JNTU-GV
Course Structure and Syllabus For
M.Tech
(VLSI (57), VLSI Design(72), VLSI System Design(61)

I – Semester

S. No.	Course Code	Course Title	L	T	P	C
1	M255701	CMOS Analog Integrated Circuit Design	3	1	0	4
2	M255702	CMOS Digital Integrated Circuit Design	3	1	0	4
3	M255703	Advanced Digital System Design	3	1	0	4
	M255704	Micro Chip Fabrication Technique				
4	M255705	Nano Electronic Material Devices	3	1	0	4
	M255706	Semiconductor Memories/ Digital Design Through HDL				
	M255707	Hardware Description Language				
5	M255708	VLSI Architecture	3	1	0	4
	M255709	Low Power VLSI				
	M255710	CAD for VLSI				
	M255711	System Design Using Embedded Processors				
6	M255712	Analog Integrated Circuit Design Lab	0	1	2	2
7	M255713	Digital Integrated Circuit Design Lab	0	1	2	2
8	M255714	Seminar-I	0	0	2	1
		TOTAL	**15**	**7**	**6**	**25**

II – Semester

S. No.	Course Code	Course Title	L	T	P	C
1	N255701	CMOS Mixed Signal Design	3	1	0	4
2	N255702	Physical Design verification	3	1	0	4
3	N255703	VLSI TESTING & TESTABILITY	3	1	0	4
4	N255704	VLSI Design Verification	3	1	0	4
	N255705	MEMS and Microsystems				
	N255706	FPGA Based System Design				
	N255707	VLSI Signal Processing				
5	N255708	VLSI Interconnects	3	1	0	4
	N255709	CMOS RF Integrated Circuit Design				
	N255710	Quantum Computing				
	N255711	Hardware Software Co-design				
6	N255712	CMOS Mixed Signal Circuit Design Lab	0	1	2	2
7	N 255713	Physical Design Verification Lab	0	1	2	2
8	N 255714	Seminar-II	0	0	2	1
		TOTAL	**15**	**7**	**6**	**25**

III Semester

S. No.	Course Code	Course Title	L	T	P	C
1	P255701	Research Methodology and IPR / Swayam 12 week MOOC course – RM&IPR	3	0	0	2
2	P255702	Summer Internship/ Industrial Training (8-10 weeks)	-	-	-	2
3	P255703	Dissertation Part – A	-	-	20	10
		TOTAL	**3**	**-**	**20**	**14**

IV Semester

S. No.	Course Code	Course Title	L	T	P	C
1	O255701	Dissertation Part – B	-	-	32	16
		TOTAL	**-**	**-**	**32**	**16**

CMOS ANALOG INTEGRATED CIRCUIT DESIGN

Course Overview: This course provides a detailed understanding of MOS devices, CMOS analog sub-circuits, and amplifier design. Topics include MOS transistor modelling, current mirrors, and amplifiers, with a focus on noise analysis and CMOS operational amplifiers. Students will learn about design techniques, compensation methods, and measurement techniques for building efficient and reliable analog circuits.

Course Objective:

- To understand the operation and modelling of MOS transistors in CMOS circuits.
- To design and analyze analog CMOS sub-circuits, such as current mirrors and voltage references.
- To explore single-stage and multi-stage amplifier designs, including gain boosting and cascode techniques.
- To study noise behavior in CMOS amplifiers and mitigate its effects.

Course Outcomes:

- Design basic building blocks of CMOS Analog ICs.
- Carry out the design of single and two stage operational amplifiers and voltage references.
- Determine the device dimensions of each MOSFETs involved.
- Design various amplifiers like differential, current and operational amplifiers.

UNIT- I

MOS Devices and Modeling: The MOS Transistor, Passive Components - Capacitor & Resistor, Integrated Circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT- II

Analog CMOS Sub-Circuits: MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors - Current Mirror with Beta Helper, Degeneration,Cascode Current

Mirror and Wilson Current Mirror, Current and Voltage References, Bandgap Reference.

UNIT- III

Single Stage Amplifier: Common Source Stage with Resistive Load, Diode Connected Load, Triode Load, CS Stage with Source Degeneration, Source Follower, CG Stage, Gain Boosting Techniques, Cascode, Folded Cascode, Choice of Device Models.

UNIT- IV

CMOS Amplifiers and Noise: Inverters, Differential Amplifiers, Cascode Amplifiers. Noise - Statistical Characteristics, Types, Noise in Single-Stage Amplifiers, Noise in Differential Pairs, Noise Bandwidth.

UNIT- V

CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of Op Amps.

Text Books:

1. CMOS Analog Circuit Design -Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.

Reference Books:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R.G. Meyer, Wiley India, Fifth Edition, 2010.

e-Reference:

1. NPTEL Courses (**https://nptel.ac.in/courses/117101105**)

CMOS DIGITAL INTEGRATED CIRCUIT DESIGN

Course Overview:

This course aims to provide a comprehensive understanding of CMOS VLSI design, covering MOS transistor principles, inverter characteristics, logic circuit design, sequential elements, arithmetic blocks, and memory architectures. Students will gain insight into both static and dynamic behaviors, layout techniques, and performance trade-offs in digital integrated circuit design.

Course Objective:

- To understand MOSFET operation under static and dynamic conditions for digital design.
- To analyze CMOS inverter characteristics including power, delay, and energy efficiency.
- To design combinational and sequential logic using various CMOS logic styles.
- To explore arithmetic building blocks focusing on speed and area trade-offs.

Course Outcomes:

- Analyze and design MOSFET-based circuits, focusing on static, dynamic, and power characteristics.
- Design combinationallogic circuits using static CMOS and dynamic logic with optimization techniques.
- Implement and analyze sequential circuits, including latches, registers, pipelines, and timing considerations.
- Design efficient arithmetic building blocks and memory architectures, focusing on speed and area tradeoffs.

UNIT- I

MOS Transistor Principles and CMOS Inverter: MOSFET characteristics under Static and Dynamic Conditions, MOS Transistor Secondary Effects, CMOS Inverter – Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay Parameters, Stick Diagram and Layout Diagrams.

UNIT- II

Combinational Logic Circuits: Static CMOS Design, Different Styles of Logic Circuits, Logical Effort of Complex Gates, Static and Dynamic Properties of Complex Gates, Interconnect Delay, Dynamic Logic Gates.

UNIT- III

Sequential Logic Circuits: Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Non-Bistable Sequential Circuits.

UNIT- IV

Arithmetic Building Blocks: Data Path Circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs.

UNIT- V

Memory Architectures: Memory Architectures and Memory Control Circuits: Read-Only Memories, ROM Cells, Read-Write Memories (RAM), Dynamic Memory Design, 6- Transistor SRAM Cell, Sense Amplifiers.

Text Books:

1. Jan Rabaey, Anantha Chandrakasan, BNikolic, "Digital Integrated Circuits: A Design Perspective", Prentice Hall of India, 2nd Edition, Feb 2003
2. N. Weste, K. Eshraghian,"Principles of CMOS VLSI Design",Addision Wesley,2nd Edition, 1993.

Reference Books:

1. MJSmith ,"Application Specific Integrated Circuits",Addisson Wesley,1997
2. Sung-MoKang & Yusuf Leblebici ,"CMOS Digital Integrated Circuits Analysis and Design", McGraw-Hill,1998.

e -References:

1. NPTELCourses(https://onlinecourses.nptel.ac.in/noc21_ee09/

ADVANCED DIGITAL SYSTEM DESIGN

Course Overview:

This course introduces front-end VLSI design and verification, focusing on reusable test environments, efficient verification of complex digital designs, and practical application of industry-standard EDA tools like Cadence and Mentor Graphics.

Course Objective:

- To demonstrate familiarity with front-end design methodologies and verification techniques, a0d develop reusable test environments.
- To verify increasingly complex digital designs with improved efficiency and effectiveness.
- To apply industry-standard EDA tools such as Cadence and Mentor Graphics for front-end design and verification.

Course Outcomes:

- Design and analyze digital systems using combinational, sequential circuits, FSMs, and basic modules.
- Develop and simulate Verilog/VHDL codes for hardware modules with IP integration techniques.
- Apply System Verilog for verification using assertions, OOP, and testbench development techniques.
- Identify and address challenges in physical design like IR drop, crosstalk, and delays.

UNIT- I

Revision of basic Digital systems: Combinational Circuits, Sequential Circuits, Logic families. Synchronous FSM and asynchronous design, Meta-stability, Clock distribution and issues, basic building blocks like PWM module, pre- fetch unit, programmable counter, FIFO, Booth's multiplier, ALU, Barrel shifter etc.

UNIT-II:

Verilog/VHDL Comparisons and Guidelines, Verilog:HDL fundamentals, simulation, and testbench design, Examples of Verilog codes for combinational and sequential logic, Verilog AMS. IP and Prototyping: IP in various forms: RTL Source code, Encrypted Source code, Soft IP, Netlist, Physical IP, and Use of external hard IP during prototyping, Case studies, and Speed issues.

UNIT-III:

System Verilog and Verification: Verification guidelines, Data types, procedural statements and routines, connecting the test bench and design, Assertions, Basic OOP concepts, Randomization. Testing of logic circuits: Fault models, BIST, JTAG interface Introduction to basic scripting language: Perl, Tcl/Tk.

UNIT-IV:

Current challenges in physical design: Roots of challenges, Delays: Wire load models Generic PD flow, Challenges in PD flow at different steps, SI Challenge - Noise & Crosstalk, IR Drop, Process effects: Process Antenna Effect &Electro migration.

UNIT-V:

Programmable Logic Devices: Introduction, Evolution: PROM, PLA, PAL, Architecture of Pal's, Applications, Programming PLD's, FPGA with technology: Anti-fuse, SRAM, EPROM, MUX, FPGA structures, and ASIC Design Flows, Programmable Interconnections, Coarse grained reconfigurable devices.

Text Books:

1. Douglas Smith, "HDL Chip Design: A Practical Guide for Designing, Synthesizing & Simulating ASICs & FPGAs Using VHDL or Verilog", Doone publications, 1998.
2. Samir Palnitkar, "Verilog HDL: A guide to Digital Design and Synthesis", Prentice Hall,2nd Edition, 2003.

Reference Books:

1. Doug Amos, Austin Lesea, Rene Richter, "FPGA based Prototyping Methodology Manual", Synopsys Press, 2011.
2. Janick Bergeron, "Writing Testbenches: Functional Verification of HDL Models", Second Edition, Springer, 2003.

e-Resources:

1. NPTEL Courses www.youtube.com/watch?v=4PMiRUPCj88&list=PLUSiNOu9YYdSWFKB8-887gcV1KZL5E8rA

2. NPTEL Courses https://archive.nptel.ac.in/courses/108/105/108105188/

MICROCHIP FABRICATION TECHNIQUE

Course Overview:
This course introduces the fundamentals of semiconductor device fabrication, covering crystal growth, wafer processing, oxidation, photolithography, etching, doping, deposition, and metallization. It also emphasizes process flows for MOS/CMOS technologies, yield analysis, design rules, stick diagrams, layouts, and packaging to provide a complete understanding of VLSI fabrication.

Course Objective:

- To explain the unit fabrication process
- To analyse process, yield and yield measurement for a process
- To propose the process flow for MOS devices
- To construct the circuit stick diagrams and circuit layout using the design rules

Course Outcomes:

- Apply and analyze the fabrication Process.
- Analyze process yield and yield measurement for a process.
- Analyze to understand flow process for MOS devices.
- Analyze to understand different concepts of circuit stick diagrams and circuit layout using the design rules .

UNIT- I
Overview of Semiconductor Industry: Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Contamination sources, clean room construction; Oxidation: dry oxidation, wet oxidation; Photolithography: Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect.
UNIT-II:
Etching Process Flow: Dry etching, Wet etching, resist stripping; Doping: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2; Deposition: CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapor phase epitaxy, molecular beam epitaxy; Chemical mechanical polishing; Metallization.
UNIT-III:
Process flow for CMOS design: Process flow for NMOS, PMOS, CMOS, BICMOS ICs, Novel MOS and GaN based devices,
Advanced isolation techniques: STI, LOCOS alternatives, High-k/metal gate process integration, Process control and monitoring during CMOS fabrication..

UNIT-IV:

Design rules: Design rules, stick diagrams and layout, Routing strategies and interconnect design rules, Layout parasitic extraction and impact on circuit performance, Reliability-aware design rules, Effect of contamination and defects on yield and reliability.

UNIT-V:

Packaging:

Overview of chip packaging types: wire bonding, flip-chip, wafer-level packagingChip characteristics, package functions, package operations Yield Measurement: Types of Yields, Models, Effect of Contamination on Yield.

Text Books:

1. Peter Van Zant, Microchip Fabrication, McGraw Hill, 2014, 6th Edition.
2. S.M. Sze, VLSI Technology, McGraw-Hill, 2017, 2nd Edition (Indian).
3. Sorab K Gandhi, VLSI Fabrication Principles: Silicon and Germanium Arsenide, Wiley, 1994, 2nd Edition.

Reference Books:

1. James D Plummer, Peter B Griffin and Michael D Deal, Silicon VLSI Technology: Fundamentals, Practice and Modeling, Pearson, 2009, 1st Edition.
2. C.Y. Chang and S.M. Sze, ULSI Technology, McGraw Hill, 2000, 2nd Edition.

e-Resources:

1. NPTEL Courses https://archive.nptel.ac.in/courses/108/108/108108113/

NANO-ELECTRONIC MATERIALS AND DEVICES

Course Overview:

The course on Nano-electronic Materials and Devices explores quantum transport, novel materials (graphene, CNTs, 2D semiconductors), and advanced device architectures (Fin FETs, TFETs, SETs). It also covers emerging memories, quantum, and neuromorphic applications, preparing students for cutting-edge research in nanoelectronics.

Course Objective:

- To understand the physics and materials for Nanoelectronics
- To understand the scaling issues
- To explain the need for non-classical and non-silicon-based devices
- To analyse the performance of novel devices

Course Outcome:

- Understand the physics and materials for Nanoelectronics.
- Understand the scaling issues.
- Explain the need for non-classical and non-silicon-based devices.
- Analyze the performance of novel devices.

UNIT- I

Overview of Nano devices: Nano devices, Nano materials, Nano device characterization, Definition of Technology node, MOS capacitor, MOS Scaling theory, Moore's Law and Koomey's law.

UNIT-II:

Issues in scaling MOS transistors: Short channel effects, Description of a typical 65 nm CMOS technology, Role of interface quality and related process techniques, Gate oxide thickness, scaling trend, SiO2 vs High-k gate dielectrics, Integration issues of high-k, Interface states, bulk charge, band offset, stability, reliability – Q bd high field, possible candidates, CV and IV techniques, Transport in Nano MOSFET, velocity saturation, ballistic transport, injection velocity, velocity overshoot, Metal gate transistor : Motivation, requirements, Integration Issues.

UNIT-III:

Non-classical MOS transistor: Requirements, and Novel devices, SOI - PDSOI and FDSOI, Ultrathin body SOI - double gate transistors, integration issues. Vertical transistors – Fin FET and Cylindrical gate FET.

UNIT-IV:

Novel devices: Tunnel FET, Negative-Capacitance (NC) FET. Metal source/drain junctions - Properties of Schottky junctions on Silicon, Germanium and compound semiconductors -Work function pinning.

Unit-V:

Emerging Nano MOSFETs: Strain, quantization, Advantages of Germanium over Silicon, PMOS versus NMOS. Compound semiconductors MOSFETs in the context of channel

quantization and strain, Hetero structure MOSFETs, exploiting novel materials, strain, quantization. CNT, Graphene, Nanotubes, nanorods and other nano-structures.

Text Books:

1. Y. Taur and T. Ning, "Fundamentals of Modern VLSI devices" Cambridge University Press, 2022, 3rd Edition.
2. Nicollian and J. R. Brews "MOS (Metal Oxide Semiconductor) Physics and Technology" Wiley, 2002, 1st Edition
3. Brundle, C. Richard, Evans, Charles A. Jr., Wilson, Shaun "Encyclopedia of Materials Characterization", Butterworth-Heinemann Manning Publications Co., 1992.

Reference Books:

1. Supriyo Datta, Lessons from Nanoelectronics A new Prospective on transport – Part A: Basic Concepts, World Scientific, 2017. 2nd Edtiton.
2. J. P. Colinge, "FinFETs and Other Multi-Gate Transistors," Springer. 2009.

e-Resources:

1. NPTEL Courses https://archive.nptel.ac.in/courses/117/108/117108047/

SEMICONDUCTOR MEMORIES

Course Overview:

This course provides a comprehensive study of semiconductor memories, covering volatile (SRAM, DRAM, CAMs) and non-volatile (ROM, Flash, RRAM, MRAM, 3D memories) technologies. It also addresses memory fault models, testing, and reliability issues to prepare students for advanced memory design challenges.

Course Objective:

- To explain the concepts and working principles of volatile memories (SRAM, DRAM, multi-ported RAMs, CAMs).
- To describe non-volatile memories (ROM, RRAM, MRAM, Flash, 3D memories).
- To understand memory fault models and testing techniques.
- To analyse reliability and design issues in semiconductor memories.

Course Outcome:

- Explain the concepts and working principles of volatile memories (SRAM, DRAM, multi-ported RAMs, CAMs).
- Describe non-volatile memories (ROM, RRAM, MRAM, Flash, 3D memories).
- Understand memory fault models and testing techniques.
- Analyze reliability and design issues in semiconductor memories.

UNIT- I

Static Random-Access Memory Technologies:

SRAM Cell Structures, MOS SRAM Architecture and Peripheral Circuit Operation, Bipolar SRAM Technologies, Silicon on Insulator (SOI) Technology, Advanced SRAM Architectures and Technologies, Application Specific SRAMs.

Unit-II:

Dynamic Random-Access Memories (DRAMs):DRAM Technology Development, CMOS DRAMs, DRAMs Cell Theory and Advanced Cell Structures, Bi- CMOS DRAMs, Soft Error Failures in DRAMs, Advanced DRAM Designs and Architecture, Application Specific DRAMs.

UNIT-III:

Non-Volatile Memories: Masked Read-Only Memories (ROMs), High Density ROMs, Programmable Read-Only Memories (PROMs), CMOS PROMs, Erasable (UV) Programmable Read-Only Memories (EPROMs), Floating Gate EPROM Cell, Onetime Programmable (OTP) EPROMs, Electrically Erasable PROMs (EEPROMs), EEPROM Technology and Architecture, Non-Volatile SRAM, Flash Memories (EPROMs or EEPROM), Advanced Flash Memory Architecture.

UNIT-IV:

Memory Fault Modelling and Testing:RAM Fault Modelling, Electrical Testing, Pseudo Random Testing, Megabit DRAM Testing, Non- volatile Memory Modelling and Testing, IDDQ Fault Modelling and Testing, Application Specific Memory Testing.

UNIT-V:

Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Non-volatile Memory Reliability, Modelling and Failure Rate Prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and Qualification, Radiation Effects, Single Event Phenomenon (SEP), Radiation Hardening Techniques and Design Issues.

Text Books:

1. Emerging Nanotechnologies (Mark Tehranipoor, 2007).
2. Practice Problems for Hardware Engineers (Nazarian, 2021).
3. Ashok K. Sharma, "Semiconductor Memories Technology, Testing and Reliability", Prentice-Hall of India Private Limited, New Delhi, 1997.

Reference Books:

1. Fernanda Lima Kastensmidt, Ricardo Reis"Fault-Tolerance Techniques for SRAM-Based FPGAs", Springer US, 2006.
2. AndreiPavlov, ManojSachdev, "CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies", Springer Germany, 2008.

e-Resources:

1. **NPTEL Courses** www.youtube.com/playlist?list=PLbMVogVj5nJRtXgdjQkYfYOHfsc-7Ar7Q

HARDWARE DESCRIPTION LANGUAGES

Course Overview:

This course introduces Verilog, System Verilog, and Verilog-AMS for digital and mixed-signal design, covering fundamentals, combinational and sequential logic modeling, state machines, and advanced verification features. It equips students with the skills to design, model, and verify modern electronic systems effectively.

Course Objective:

- To differentiate sequential language and concurrent language.
- To design combinational logic circuits using VHDL.
- To design sequential logic circuits using VHDL.
- To model Analog circuits using Verilog AMS.

Course Outcome:

- Differentiate sequential language and concurrent language.
- Design combinational logic circuits using VHDL.
- Design sequential logic circuits using VHDL.
- Model analog circuits using Verilog AMS.

UNIT- II

Introduction to Verilog

Overview of Verilog, Design Flows & EDA Tools, Code Structure, Data types, Operators and Attributes: Operators, Attributes, User-Defined Attributes, Operator, overloading.

UNIT-II:

Concurrent Code:Concurrent versus Sequential, Using Operators, WHEN, Generate and Block, Sequential Code:

Process, Signals and Variables, IF, WAIT, CASE, Using Sequential Code to Design Combinational Circuits.

UNIT-III:

State Machines: Introduction, Design Style #1, Design Style #2 (Stored Output), Encoding Style: From Binary to One Hot.

UNIT-IV:

System Verilog: Verilog +, Coverage, Randomization, Assertion, functional coverage, Object oriented programming, define parameter.

UNIT-V:

Verilog-AMS: Verilog Family of Languages, Mixed Signal Simulators, Applications of Verilog-AMS, Analog Modelling. Language Reference: Basics, Data Types, Signals, Expressions, Analog Behaviour.

Text Books:

1. Samir Palnitkar, Verilog HDL, 2nd Edition, Pearson Education, 2003, 2nd Edition.
2. Chris Spear, System Verilog for Verification: A Guide to Learning the Testbench Language Features, Springer, 2012, 3rd Edition.

Reference Books:

1. Joseph Cavanagh, Verilog HDL Design Examples, CRC Press, 2018, 1st Edition
2. Blaine Readler, Verilog by Example: A Concise Introduction for FPGA Design, Full ARC Press, 2011.

e-Resources:

1. NPTEL Courses https://nptel.ac.in/courses/106105165

VLSI ARCHITECTURES

Course Overview:

This course covers the design and analysis of VLSI architectures, focusing on RISC processors and DSP systems. It includes RISC design with pipelining, mapping DSP algorithms to efficient hardware, and applying optimization techniques like folding, unfolding, and retiming for performance improvement.

Course Objective:

- To design of RISC architecture and controller for a specific instruction set.
- To improve the performance of RISC processor by employing pipelining.
- To translate DSP algorithm into an efficient architecture and study the design of different building blocks of DSP architectures.
- To translate DSP algorithm into an efficient architecture and study the design of different building blocks of DSP architectures.

Course Outcome:

- Design RISC architecture and controller for a specific instruction set.
- Improve the performance of a RISC processor by employing pipelining.
- Translate DSP algorithms into efficient architectures and study the design of DSP building blocks.
- Estimate the effect of folding, unfolding, and retiming techniques on the performance of DSP architectures.

UNIT- I

Overview of the architectures: Overview of the features of Instruction set architectures of CISC, RISC and DSP processors. CPU performance and its factors, evaluating the performance. Design of RISC processor: Building data path and Control, multicycle implementation.

UNIT- II

Enhancing the performance with pipelining: An overview of pipelining, pipelined data path, Pipelined Control unit, various hazards of pipelining, Hazard free pipelined RISC implementation.

UNIT-III:

Multiprocessors:

Introduction, Multiprocessors connected by a single bus, Multiprocessors connected by a network, Network Topologies, Evolution versus revolution in Computer Architecture.

UNIT-IV:

Representation of DSP Algorithms, data flow graph representations, loop bound and iterative bound, algorithms for computing iteration bound.

UNIT-V:

Pipe lining and parallel processing: Introduction, pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power. Different techniques to improve the performance VLSI Architectures: Retiming, Unfolding and Folding techniques.

Text Books:

1. D.A, Patterson and J.L. Hennessy, Computer Organization and Design: Hardware / Software Interface, Elsevier, 2011, 4th Edition
2. Wayne Wolf, *Modern VLSI Design: System-on-Chip Design*, Pearson, 4th Edition, 2009.

Reference Books:

1. John L. Hennessy and David A. Patterson, *Computer Architecture: A Quantitative Approach*, Morgan Kaufmann, 6th Edition, 2019.

Keshab K. Parhi, *VLSI Digital Signal Processing Systems: Design and Implementation*, Wiley, 1999.

e-Resources:

1. NPTEL Courses www.youtube.com/watch?v=9SnR3M3CIm4&list=PL018645397D9487AF

LOW POWER VLSI

Course Overview:

This course focuses on low-power VLSI design, covering sources of power dissipation, their impact on performance and reliability, power modeling and analysis methods, leakage mechanisms, and advanced reduction techniques for energy-efficient system design.

Course Objective:

- To identify the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability.
- To characterize and model power consumption & understand the basic analysis methods.
- To understand leakage sources and reduction techniques.

Course Outcomes:

- Identify the sources of power dissipation in digital IC systems.
- understand and analyze the impact of power on system performance and reliability..
- Characterize and model power consumption and understand the basic analysis methods.
- Understand leakage sources and reduction techniques.

UNIT- I

Sources of Power Dissipation: Introduction, Short-Circuit Power Dissipation, Switching Power Dissipation, Dynamic Power for a Complex Gate, Reduced Voltage Swing, Switching Activity, Leakage Power Dissipation, p–n Junction Reverse-Biased Current, Band-to-Band Tunnelling Current, Sub threshold Leakage Current, Short-Channel Effects.

UNIT-II:

Supply Voltage Scaling for Low Power: Device Feature Size Scaling, Constant-Field Scaling, Constant-Voltage Scaling, Architectural-Level Approaches: Parallelism for Low Power, Pipelining for Low Power, Combining Parallelism with Pipelining, Voltage Scaling Using High-Level Transformations: Multilevel Voltage Scaling Challenges in MVS Voltage Scaling Interfaces, Static Timing Analysis Dynamic Voltage and Frequency Scaling.

UNIT-III:

Switched Capacitance Minimization: Probabilistic Power Analysis: Random logic signals, probability and frequency, probabilistic power analysis techniques, signal entropy, Bus Encoding: Gray Coding, One-Hot Coding, Bus-Inversion, T0 Coding, Clock Gating, Gated-Clock FSMs FSM State Encoding, FSM Partitioning, Pre-computation, Glitching Power Minimization.

UNIT-IV:

Leakage Power Minimization: Fabrication of Multiple Threshold Voltages, Multiple Channel Doping, Multiple Oxide CMOS, Multiple Channel Length, Multiple Body Bias, VTCMOS Approach, MTCMOS Approach, Power Gating, Clock Gating Versus Power Gating, Power-Gating Issues, Isolation Strategy, State Retention Strategy, Power-Gating Controller, Power Management, Combining DVFS and Power Management.

UNIT-V:

Low power clock distribution & Simulation Power Analysis: Low power clock distribution:

Power dissipation in clock distribution, single driver versus distributed buffers, zero skew versus tolerable skew, chip and package co design for clock network. Simulation Power Analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, architecture level analysis, data correlation analysis of DSP systems, Monte Carlo Simulation.

Text Books:

1. Low-Power VLSI Circuits and Systems, Ajit Pal, SPRINGER PUBLISHERS
2. Practical Low Power Digital VlsiDesign, Gary Yeap Motorola, Springer Science Business Media, LLC.

Reference Books:

1. Low Power CMOS Design – Anantha Chandrakasan, IEEE Press/Wiley International, 1998. 2
2. MassoudPedram, Jan M. Rabaey , "Low power design methodologies ", Kluwer Academic Publishers.

e-Resources:

1. NPTELCourses www.youtube.com/watch?v=TFOO1JAll2Y&list=PLBU5KursMXEMWAkoUPB5aqUPb3lKYqN6q

CAD FOR VLSI

Course Overview: This course covers VLSI physical design automation, focusing on design cycles, partitioning, floor planning, pin assignment, placement, routing, and FPGA/MCM technologies. It explores advanced algorithms, including those for global and detailed routing, as well as chip input/output circuits, protection, and clock generation.

Course Objective:

- To understand the VLSI design and physical design automation processes.
- To learn various partitioning, floor planning, placement, and routing algorithms.
- To explore FPGA and MCM technologies and their design cycles.
- To study chip input/output circuits, ESD protection, and clock distribution techniques.

Course outcome:

- Understand the VLSI design flow and the stages of physical design automation.
- Apply algorithms for partitioning, floor planning, pin assignment, and placement.
- Analyze and implement routing algorithms for global and detailed routing.
- Explore physical design techniques for FPGAs and MCMs and Design robust I/O circuits and understand ESD.

UNIT- I

VLSI Physical Design Automation: VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.

UNIT- II

Partitioning, Floor Planning, Pin Assignment and Placement: Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing. Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint-based floor planning, Rectangular Dualization. Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel pin assignments. Placement – Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms.

UNIT- III

Global Routing and Detailed Routing: Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms. Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms.

UNIT- IV

Physical Design Automation of FPGAs and MCMs: FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model. Introduction to MCM Technologies, MCM Physical Design Cycle.

UNIT- V

Chip Input and Output Circuits: ESD Protection, Input Circuits, Output Circuits and L(di/dt) noise, On-chip clock Generation and Distribution, Latch-up and its prevention.

Text Books:

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani, 3rd Edition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

Reference Books:

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.

e-Reference:

1. NPTEL Courses (https://nptel.ac.in/courses/106106088**)**

System Design Using Embedded Processors

UNIT-1:

Embedded Concepts Introduction to embedded systems, Application Areas, Categories of embedded systems, Overview of embedded system architecture, Specialties of embedded systems, recent trends in embedded systems, Architecture of embedded systems, Hardware architecture, Software architecture, Application Software, Communication Software, Development and debugging Tools.

ARM Architecture Background of ARM Architecture, Architecture Versions, Processor Naming, Instruction Set Development, Thumb-2 and Instruction Set Architecture.

UNIT-II

Overview of Cortex-M3 Cortex-M3 Basics: Registers, General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Registers, Operation Mode, Exceptions and Interrupts, Vector Tables, Stack Memory Operations, Reset Sequence.

Instruction Sets: Assembly Basics, Instruction List, Instruction Descriptions.

UNIT-III

Cortex-M3 Implementation Overview: Pipeline, Block Diagram, Bus Interfaces on Cortex-M3, I-Code Bus, D-Code Bus, System Bus, External PPB and DAP Bus.

Exceptions: Exception Types, Priority, Vector Tables, Interrupt Inputs and Pending Behavior, Fault Exceptions, Supervisor Call and Pendable Service Call.

NVIC: Nested Vectored Interrupt Controller Overview, Basic Interrupt Configuration, Software Interrupts and SYSTICK Timer.

Interrupt Behavior: Interrupt/Exception Sequences, Exception Exits, Nested Interrupts, Tail-Chaining Interrupts, Late Arrivals and Interrupt Latency

UNIT-IV

Cortex-M3/M4 Programming: Cortex-M3/M4 Programming: Overview, Typical Development Flow, Using C, CMSIS (Cortex Microcontroller Software Interface Standard), Using Assembly.

Exception Programming: Using Interrupts, Exception/Interrupt Handlers, Software Interrupts, Vector Table Relocation.

Memory Protection Unit and other Cortex-M3 features: MPU Registers, Setting Up the MPU, Power Management, Multiprocessor Communication.

UNIT-V

Cortex-M3/M4 Microcontroller STM32L15xxx ARM Cortex M3/M4 Microcontroller: Memory and Bus Architecture, Power Control, Reset and Clock Control.

STM32L15xxx Peripherals: GPIOs, System Configuration Controller, NVIC, ADC, Comparators, GP Timers, USART.

Development & Debugging Tools: Software and Hardware tools like Cross Assembler, Compiler, Debugger, Simulator, InCircuit Emulator (ICE), Logic Analyzer etc.

TEXT BOOKS:

1. The Definitive Guide to the ARM Cortex-M3, Joseph Yiu, Second Edition, Elsevier Inc. 2010.
2. Embedded/Real Time Systems Concepts, Design and Programming Black Book, Prasad, KVK.
3. David Seal "ARM Architecture Reference Manual", 2001 Addison Wesley, England; Morgan Kaufmann Publishers
4. Andrew N Sloss, Dominic Symes, Chris Wright, "ARM System Developer's Guide - Designing and Optimizing System Software", 2006, Elsevier.

REFERENCES:

1. Steve Furber, "ARM System-on-Chip Architecture", 2nd Edition, Pearson Education
2. Cortex-M series-ARM Reference Manual
3. Cortex-M3 Technical Reference Manual (TRM)
4. STM32L152xx ARM Cortex M3 Microcontroller Reference Manual
5. ARM Company Ltd. "ARM Architecture Reference Manual– ARM DDI 0100E"
6. ARM v7-M Architecture Reference Manual (ARM v7-M ARM).
7. Ajay Deshmukh, "Microcontroller - Theory & Applications", Tata McGraw Hill
8. Arnold. S. Berger, "Embedded Systems Design - An introduction to Processes, Tools and Techniques", Easwer Press

CMOS ANALOG INTEGRATED CIRCUIT DESIGN LAB

Course Overview: This lab course focuses on designing and simulating analog CMOS circuits using industry-standard EDA tools. Students gain hands-on experience in schematic design, layout, simulation, and verification, enhancing their understanding of VLSI design methodologies and analog integrated circuit performance optimization.

Course Objective:

- To understand CMOS analog design using EDA tools and techniques.
- To develop schematics and layouts for optimized analog circuit performance.
- To perform simulations verifying functionality of pre-layout and post-layout designs.
- To apply physical verification ensuring correctness and manufacturability of layouts.

Course Outcomes:

- Apply VLSI design methodologies using Mentor Graphics tools to design and verify IC circuits.
- Analyze CMOS analog circuits' role in full- custom IC design flows for performance optimization.
- Apply physical verification techniques in layout design to ensure design correctness and manufacturability.
- Create pre-layout and post-layout simulations to validate and optimize VLSI designs for functionality.

1. List of Experiments:
2. Experiment Name
3. MOS Device Characterization and parametric analysis.
4. Common Source Amplifier.
5. Common Source Amplifier with source degeneration.
6. Cascode amplifier.
7. Simple current mirror.
8. Cascode current mirror.

9. Wilson current mirror.
10. Differential Amplifier.
11. Operational Amplifier.
12. Sample and Hold Circuit.
13. Direct-conversion ADC.
14. R-2R Ladder Type DAC.

Lab Requirements:

Software:

Mentor Graphics – Pyxis Schematic, IC Station, Calibre, ELDO Simulator/ Industry Equivalent Standard Software.

Hardware:

Personal Computer with necessary peripherals, configuration and operating System..

CMOS DIGITAL INTEGRATED CIRCUIT DESIGN LAB

Course Overview: The Digital CMOS Circuit Design Lab provides hands-on experience with CMOS digital circuit design using industry-standard software tools like Mentor Graphics, Cadence, or Synopsys. Students will design, analyze, and verify various logic circuits, including multiplexers, flip-flops, counters, and memory cells, while learning physical verification and layout extraction techniques.

Course Objective:

- To apply VLSI design methodologies using standard industry EDA tools.
- To design and analyze CMOS logic circuits for digital applications.
- To perform layout extraction and physical verification for CMOS designs.
- To analyze digital CMOS circuits including sequential and combinational components.

Course Outcomes:

- Apply VLSI Design Methodologies using industry-standard tools like Mentor Graphics.
- Analyze and design basic CMOS logic circuits for full-custom IC design.
- Perform physical verification and layout extraction for CMOS circuits.
- Analyze CMOS digital circuits, including sequential and combinational logic components.

List of Experiments:

- Inverter Characteristics.
- NAND and NOR Gate.
- XOR and XNOR Gate.
- 2:1 Multiplexer.
- Full Adder.
- RS-Latch.
- Clock Divider.
- JK-Flip Flop.
- Synchronous Counter.

- Asynchronous Counter
- Static RAM Cell.
- Dynamic Logic Circuits.
- Linear Feedback Shift Register.

Lab Requirements:

Software:

Industry Standard Software (Mentor Graphics Tool/Cadence/ Synopsys/Equivalent)

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

CMOS MIXED SIGNAL DESIGN

Course Overview: This course covers advanced topics in analog CMOS design, including two-stage op-amp design, switched capacitor circuits, sample-and-hold circuits, comparators, data converters, and phase-locked loops (PLLs). Emphasis is placed on circuit analysis, noise reduction, parasitic effects, and performance limitations. Students will learn practical design strategies for high-performance analog circuits.

Course Objective:

- To design and analyze two-stage operational amplifiers, focusing on parasitic effects and biasing.
- To explore switched capacitor circuits and their applications in filter design and integrators.
- To understand the principles and design of comparators, including issues like propagation delay and slew rate.
- To study data converters and PLLs, emphasizing performance limitations, noise, and circuit optimization.

Course Outcomes:

- Understand the necessity of mixed signal systems.
- Analyze Op-Amp to meet the mixed signal specifications.
- Design CMOS comparators to meet the high- speed requirements of digital circuitry.
- Develop efficient data converter circuits for mixed signal systems.

UNIT- I

Two-Stage OP-AMP Design: Parasitic Effects on Design of Two-Stage OP-AMP, Wide Swing Cascode Current Mirrors, Design of Rugged Biasing Circuit with Temperature Independent Compensation, Challenges in Mixed-Signal Circuit Design.

Switched Capacitor Circuits: Constituents: Op-Amp, Capacitors, Switches, Non- overlapping Clocks; Basic Operation and Analysis, Resistor Equivalence of a Switched Capacitor, Parasitic-Sensitive Integrator, Parasitic-Insensitive Integrators, Signal-Flow- Graph Analysis, Design of Filters Based on Switched Capacitor Circuits.

UNIT- II

Sample-and-Hold Circuit: Testing Sample and Holds, MOS Sample-and-Hold Basics, Examples of CMOS S/H Circuits, Charge-Injection Errors, Making Charge-Injection Signal Independent, Minimizing Errors Due to Charge-Injection, Effect of Offset and Application of Switched Capacitor Circuits to Minimize Offset Errors, Parasitic Effects.

UNIT- III

Comparators: Ideal Comparator, Practical Model of Comparator, Resolving Capability, Propagation Delay, Small Signal Analysis, Conditions for Slewing, Evaluation of Propagation Delay for Single Pole and Two Pole Comparators, Design of Linear Response Comparators, Slew-Rate Limited Comparators, Comparators with Positive Feedback, Analysis of Latched Comparators, Architecture of High-Speed Comparators, Self-Biased Comparators, Push Pull Comparators.

UNIT- IV

Data Converters: Classification, Ideal D/A Converter, Ideal A/D Converter, Quantization Noise: Deterministic and Stochastic Approach, Signed Codes, Performance Limitations: Resolution, Offset and Gain Error, Accuracy and Linearity, Integrating Converters, Design of Successive-Approximation Converters, DAC-Based and Charge-Redistribution SAR, Interleaved, Pipelined, Flash, Principles of Sigma-Delta ADC, Testing of Data Converters.

UNIT- V

PLL and Oscillators: Basic PLL Architecture, VCO, Divider, Phase Detector, Loop Filter, PLL in Lock, Linearized Small-Signal Analysis, Second-Order PLL Model, Limitations, PLL Characterization and Design Example, Jitter and Phase Noise: Period Jitter, Cycle Jitter, Adjacent Period Jitter, Spectral Representations and PDF of Jitter, Ring and LC Oscillators, Phase Noise in Oscillators and PLLs.

Text Books:

1. David Johns, Tony Chan Carusone and Kenneth Martin, Analog Integrated Circuit Design, Wiley, 2012, 2nd Edition.
2. Behzad Razavi, Design of Analog CMOS Integrated Circuits"McGraw Hill Education, 2017, 2nd Edition.

Reference Books:

1. Roubik Gregorian and Gabor C. Temes, Analog MOS integrated circuits for signal processing, Wiley, 1986.
2. Roubik Gregorian, Introduction to CMOS Op-Amps and Comparators, Wiley, 2008.

e-Reference:

1. NPTEL Courses https://onlinecourses.nptel.ac.in/noc22_ee34/preview

PHYSICAL DESIGN VERIFICATION

Course Overview: This course covers VLSI physical design, focusing on design cycles, fabrication processes, and layout techniques. Topics include design styles, interconnect delay, complexity issues, graph algorithms, and data structures for layout editors. It also explores partitioning, floor planning, pin assignment, and routing algorithms, equipping students with tools for efficient VLSI design.

Course Objective:

- To understand the VLSI design and physical design cycles, including fabrication and layout processes.
- To explore design styles and interconnect issues, focusing on noise, crosstalk, and yield.
- To study graph algorithms and data structures for solving physical design problems.
- To learn partitioning, floor planning, and routing algorithms for efficient VLSI design.

Course Outcomes:

- Understand the relationship between design automation algorithms and Various constraints posed by VLSI fabrication and design technology.
- Adapt the design algorithms to meet the critical design parameters.
- Identify layout optimization techniques and map them to the algorithms.
- Develop proto-type EDA tool and test its efficacy.

UNIT- I

VLSI Design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication. Design styles: Full Custom, Standard Cell, Gate Arrays, Field Programmable Gate Arrays, Sea of Gates and Comparison, System Packaging Styles, Multi- Chip Modules. Design Rules, Layout of Basic Devices, Fabrication Process and Its Impact on Physical Design, Interconnect Delay, Noise and Crosstalk, Yield and Fabrication Cost.

UNIT- II

Factors, Complexity Issues and NP-hard Problems. Basic Algorithms (Graph and Computational Geometry): Graph Search Algorithms, Spanning Tree Algorithms, Shortest Path Algorithms, Matching Algorithms, Min-Cut and Max-Cut Algorithms, Steiner Tree Algorithms.

UNIT- III

Basic Data Structures: Atomic Operations for Layout Editors, Linked List of Blocks, Bin Based Methods, Neighbour Pointers, Corner Stitching, Multi-Layer Operations.

UNIT- IV

Graph Algorithms for Physical Design: Classes of Graphs, Graphs Related to a Set of Lines, Graphs Related to a Set of Rectangles, Graph Problems in Physical Design, Maximum Clique and Minimum Coloring, Maximum k-Independent Set Algorithm, Algorithms for Circle Graphs.

UNIT- V

Partitioning Algorithms: Design Style Specific Partitioning Problems, Group Migrated Algorithms, Simulated Annealing and Evolution. Floor Planning and Pin Assignment, Routing and Placement Algorithms.

Text Books:

1. Naveed Shervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.
2. Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008.

Reference Books:

1. "CMOS VLSI Design: A Circuits and Systems Perspective" by Neil H. E. Weste and David Harris
2. "VLSI Physical Design: From Graph Partitioning to Timing Closure" by K. D. Meade and L. F. D. DeMicheli.

e-Reference:

1. NPTEL Courses **https://nptel.ac.in/courses/106103016**

VLSI TESTING & TESTABILITY

Course Overview: This course focuses on VLSI testing, covering fault modelling, simulation, and test generation techniques. Topics include structural and functional testing, ATPG, scan chain-based methods, D-Algorithm, and Design for Testability (DFT). Students will also explore built-in self-test (BIST) and testable memory design for efficient VLSI testing.

Course Objective:

- To understand fault modelling, error diagnosis, and yield improvement in VLSI design testing.
- To learn fault simulation techniques and algorithms, including serial, parallel, and deductive methods.
- To explore test generation methods for combinational and sequential circuits, including ATPG and scan-based testing.
- To study Design for Testability (DFT) techniques and testable memory design, including BIST architectures.

Course Outcomes:

- Identify the significance of testable design.
- Specify fabrication defects, errors, and faults.
- Implement combinational and sequential circuit test generation algorithms.
- Identify techniques to improve fault coverage.

UNIT- I

Role of Testing in VLSI Design Flow, Testing at Different Levels of Abstraction, Fault, Error, Defect, Diagnosis, Yield. Types of Testing, Rule of Ten, Defects in VLSI Chip. Modelling Basic Concepts, Functional Modelling at Logic Level and Register Level, Structure Models, Logic Simulation, Delay Models. Various Types of Faults, Fault Equivalence and Fault Dominance in Combinational and Sequential Circuits.

UNIT- II

Fault Simulation Applications, General Fault Simulation Algorithms: Serial and Parallel, Deductive Fault Simulation Algorithms.

UNIT- III

Combinational Circuit Test Generation, Structural Vs Functional Test, ATPG, Path Sensitization Methods. Difference Between Combinational and Sequential Circuit Testing, Five and Eight Valued Algebra, Scan Chain-Based Testing Method.

UNIT- IV

D-Algorithm Procedure, Problems. PODEM Algorithm, Problems on PODEM Algorithm. FAN Algorithm, Problems on FAN Algorithm. Comparison of D, FAN and PODEM Algorithms. Design for Testability, Ad-Hoc Design, Generic Scan-Based Design.

UNIT- V

Classical Scan-Based Design, System Level DFT Approaches. Test Pattern Generation for BIST, Circular BIST, BIST Architectures. Testable Memory Design: Test Algorithms, Test Generation for Embedded RAMs.

TEXT BOOK:

1. M. Abramovici, M. Breuer, and A. Friedman, "Digital Systems Testing and Testable Design, IEEE Press, 1990.
2. M. Bushnell and V. Agrawal, "Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2000.

Reference Books:

1. Stroud,"A Designer's Guide to Built-in Self-Test", Kluwer AcademicPublishers,2002.
2. V.Agrawal and S.C.Seth, Test Generation for VLSI Chips, Computer Society Press. 1989.

e-Reference:

1. NPTEL Courses https://archive.nptel.ac.in/courses/117/105/117105137/

VLSI DESIGN VERIFICATION

Course Overview:

This course introduces the principles and methodologies of verifying complex VLSI designs before fabrication. It emphasizes functional correctness, performance validation, and ensuring reliability of digital systems. Students will learn simulation-based and formal verification approaches, testbench creation, coverage-driven verification, and industry-standard verification languages and tools.

Course Objective:

- Understand the need for design verification and verification methodologies in the VLSI design cycle.
- Develop skills in HDL-based modeling and writing effective testbenches.
- Apply simulation, debugging, and coverage analysis for functional verification.
- Explore advanced techniques like constrained random verification and assertion-based verification.
- Gain exposure to industry practices using SystemVerilog, UVM, and formal verification tools.

Course Outcomes:

- Understand the importance of design verification and methodologies in the VLSI design cycle.
- Develop HDL-based models and write effective testbenches for digital circuits.
- Apply simulation, debugging, and coverage-driven techniques for functional verification.
- Explore advanced verification techniques such as constrained random and assertion- based verification using System Verilog/UVM

UNIT- I

Design: Introduction to Digital VLSI Design Flow, High Level Design Representation, Transformations for High Level Synthesis.

Scheduling, Allocation and Binding: Introduction to HLS: Scheduling, Allocation and Binding Problem, Scheduling Algorithms, Binding and Allocation Algorithms.

UNIT-II:

Logic Optimization and Synthesis, Two level Boolean Logic Synthesis Lecture IV: Heuristic Minimization of Two-Level Circuits, Finite State Machine Synthesis Lecture VI: Multilevel Implementation.

Binary Decision Diagram, Binary Decision Diagram: Introduction and construction, Ordered Binary Decision Diagram, Operations on Ordered Binary Decision Diagram, Ordered Binary Decision Diagram for Sequential Circuits.

UNIT-III:

Temporal Logic: Introduction and Basic Operations on Temporal Logic, Syntax and Semantics of CLT, Equivalence between CTL Formulas.

Model Checking: Verification Techniques Lecture-II, III and IV: Model Checking Algorithm Symbolic Model Checking.

UNIT-IV:

Introduction to Digital Testing: Introduction to Digital VLSI Testing, Functional and Structural Testing, Fault Equivalence.

Fault Simulation and Testability Measures: Fault Simulation, Testability Measures (SCOAP).

UNIT-V:

Combinational Circuit Test Pattern Generation: Introduction to Automatic Test Pattern Generation (ATPG) and ATPG Algebras, D-Algorithm.

Sequential Circuit Testing and Scan Chains, ATPG for Synchronous Sequential Circuits, Scan Chain based Sequential Circuit Testing.

Built in Self-test (BIST): Built in Self-Test, Memory Testing.

Text Books:

1. D. D. Gajski, N. D.Dutt,A.C.-H. Wu and S.Y.-L. Lin, HighLevel Synthesis: Introduction to Chip and System Design, Springer, 1st edition, 1992.
2. 2. S.Palnitkar,Verilog HDL:A Guide to Digital Design and Synthesis,Prentice Hall, 2nd edition, 2003.

Reference Books:

1. G. De Micheli.Synthesis and optimization of digital circuits, 1st edition, 1994.
2. 2. M. Huth and M. Ryan, Logic in Computer Science modeling and reasoning about systems, Cambridge University Press, 2nd Edition, 2004.

e-Resource:

1. VLSI Design Verification and test: https://nptel.ac.in/courses/106103016.

MEMS AND MICROSYSTEMS

Course Overview:

The course on **MEMS (Micro-Electro-Mechanical Systems) and Microsystems** introduces students to the interdisciplinary field that integrates mechanical elements, sensors, actuators, and electronics on a common silicon substrate through microfabrication technology. It explores the principles, design, fabrication techniques, and applications of microscale devices that are widely used in consumer electronics, automotive systems, healthcare, aerospace, and industrial automation.

Course Objective:

- The course will provide adequate understanding of the physics behind the MEMS and Microsystems.
- To make students familiar with different types microsystems useful in Industries.
- To discuss MEMS device fabrication technique.
- To discuss different MEMS Device theories and their Characterization.

Course Outcomes:

- Understand the fundamental principles and working mechanisms of various MEMS and Microsystems.
- Develop the knowledge of MEMS device operation, fabrication processes, and characterization techniques.
- Identify MEMS materials and analyze their physical properties that enable their use in microsystem applications.
- Apply concepts of MEMS sensors and actuators in designing solutions for real- world engineering applications.

UNIT- I

Introduction to MEMS

Brief overview of: MEMS, Microsystems & Microelectronics Introduction to Micro fabrication, Micro sensors, Micro actuation, Micro accelerometers, Micro fluidics. MEMS & microsystem application in Electrical, Electronics, Mechanical and Bio-Medical fields.

UNIT-II:

MEMS Materials and Their Properties

Most popular Materials used in MEMS & Microsystems, and their properties: Young modulus, Poisson's ratio, density, Piezo-resistive coefficients, Temperature Coefficient of Resistance, Thermal Conductivity. Selection criterion of MEMS materials based on filed applications.

UNIT-III:

MEMS Fabrication Processes

Understanding MEMS Fabrication Processes & parameters for: Cleaning, Growth & Deposition, Ion Implantation & Diffusion, Annealing, Lithography, Etching, Bulk & Surface Micromachining, Surface Micromachining, The LIGA Process. Selection of MEMS Fabrication processes based on Applications.

UNIT-IV:

MEMS Devices

Understanding the Architecture, working and basic principle of: Micro-heaters, Accelerometers, Pressure Sensors, Digital Micrometre Device. Understanding steps involved in Design and fabrication of the above devices.

UNIT-V:

MEMS Device Characterization

Piezo-resistance, TCR, Stiffness, Adhesion, Vibration, Resonant frequency, & importance of these measurements in studying device behaviour, MEMS Reliability.

Text Books:

1. Analysis and Design Principles of MEMS Devices - Minhang Bao; Publisher: Elsevier Science.
2. An Introduction to Microelectromechanical Systems Engineering; 2nd Ed - by N. Maluf, K Williams; Publisher: Artech House Inc.

Reference Books:

1. Micro Electro Mechanical System Design - by J. Allen; Publisher: CRC Press.
2. Fundamentals of Microfabrication - by M. Madou; Publisher: CRC Press; 2nd Ed.

e-Resource:

1. MEMS and Microsystems: https://nptel.ac.in/courses/117105082

FPGA BASED SYSTEM DESIGN

Course Objectives:

- To learn the different types of programming elements, programmable logic blocks, programmable input-output blocks and programmable interconnects of various types of FPGAs.
- To understand the steps involved in synthesis, simulation, and testing of systems.
- To design and implement circuits, subsystem and system using FPGA and I/O boards.

Course Outcomes:

- Understand the basic concepts of FPGA and its structures.
- Understand the steps involved in synthesis, simulation, and testing of systems.
- Design combinational and arithmetic circuits using FPGA board.
- Design memories and DCTQ processor.
- Design real time applications using FPGA board.

UNIT I:

FPGA ARCHITECTURES

FPGA-Based Systems: Basic Concepts: Digital Design and FPGAs, The Role of FPGAs, FPGA Types, FPGAs vs. Custom VLSI, FPGA-Based System Design, Goals and Techniques, Hierarchical Design, Design Abstraction, Methodologies. FPGA Basics: Components of an FPGA, Programming Technology, Antifuse Technology, Logic Circuit Representation of FPGA. FPGA Structure: Logic Block, Logic Cluster, Adaptive LUT, Routing Part, Switch Block, Connection Block , I/O Block, DSP Block, Hard Macros, Embedded Memory, Configuration Chain – PLL and DLL.

UNIT -II

FPGA DESIGN FLOW

Design Flow and Design Tools: Design Flow, Design Flow by HDL, HLS Design, IP-Based Design, Design with Processor. Design Methodology: FPGA Design Flow, Technology Mapping, Clustering, Place and Route, Low Power Design Tools. Simulation and Synthesis Concepts,

Place and Route, Technology Mapping.

UNIT- III

FPGA BASED SUBSYSTEM DESIGN

Combinational Circuits: Basic Gates,Majority Logic and Concatenation,Shift Operations, Multiplexers, Demultiplexer,Full Adder, Magnitude Comparator. Sequential Circuits: D Flip-flop, Registers, Shift Registers, Counters. Finite State Machines – Pattern Sequence Detector. Arithmetic Circuit Designs: Digital Pipelining, Partitioning of a Design, Signed Adder Design, Multiplier Design.

UNIT -IV

FPGA BASED SYSTEM DESIGN

Design of Memories: On-chip Dual Address ROM Design, Single Address ROM Design, OnChip Dual RAM Design,External Memory Controller Design. System Designs: Discrete Cosine Transform and Quantization Processor, FOSS Motion Estimation Processor, DCTQ Processor

UNIT -V

FPGA BASED PROJECT DESIGN

Project Designs: Traffic Light Controller, Real Time Clock, Digital Signal Processor, PCI Bus Arbiter, DCTQ Processor, Electrostatic Precipitator Controller, JPEG/H.263/MPEG 1/ MPEG 2

Text Books And References:

1. Wayne Wolf, “FPGA-Based System Design”, PTR Prentice Hall, 2004.
2. Hideharu Amano, “Principles and Structures of FPGAs”, Springer, 2018.
3. S. Ramachandran, “Digital VLSI Systems Design: A Design Manual for Implementation of Projects on FPGAs and ASICs Using Verilog”, Springer, 2007.
4. Peter R. Wilson, “Design Recipes for FPGAs”, Springer, 2008.
5. Sanjay Churiwala, “Designing with Xilinx FPGAs Using Vivado”, Springer, 2017.

VLSI SIGNAL PROCESSING

Course Overview:

This course focuses on the efficient implementation of digital signal processing (DSP) algorithms using VLSI architectures. It covers concepts such as pipelining, parallelism, retiming, folding, unfolding, and systolic architectures. Emphasis is given to algorithm-to- architecture mapping, optimization of speed, area, and power, and real-time DSP applications in communications, image, and multimedia systems.

Course Objective:

- Introduce students to the basics of VLSI signal processing and the designing of VLSI architectures.
- This course is directed towards the understanding of important techniques for designing efficient VLSI architectures for DSP.
- What are the challenges in the implementation of DSP systems and how to overcome these challenges.
- How to design a system with high throughput demanded by the real-time applications and also with less power and less chip area.

Course Outcomes:

- Understand and explain the basic concepts of VLSI signal processing and its various components.
- Design efficient hardware architectures for implementing DSP techniques and algorithms.
- Analyse methods to reduce area, power, and delay in DSP-based circuits, and enhance throughput and operating frequency.
- Gain insight into real-time operating systems and their role in DSP systems.

Unit- I:

Overview of VLSI Architectures, Typical Signal Processing Algorithms, representation of DSP algorithms; Iterative bound: data-flow graph representation, loop bound and iterative bound.

Unit-II:

Pipelining and parallel processing: pipelining of FIR filters, pipelining and parallel processing for low power; Retiming: definition and properties, retiming techniques; Unfolding: properties of unfolding, critical path, unfolding and retiming; Folding: folding transformations, register minimization techniques.

Unit-III:

Systolic architecture design methodology, FIR systolic arrays; Fast convolution: Cook-Toom algorithm, Winograd algorithm, cyclic convolution; Algorithm strength reduction in filters and transforms: parallel FIR filters, DCT and IDCT, rank-order filters.

Unit-IV:

Pipelined and parallel recursive and adaptive filters: pipeline inverting in digital filters, pipelining in first-order IIR filter, parallel processing for IIR filter.

Unit-V:

DSP Processors for Mobile and Wireless Communications, Processors for Multidimensional Signal Processing.

Text Books:

1. Wiley-Inter science**,** VLSI Digital Signal Processing Systems: Design and Implementation, 2nd Edition, 2025.
2. S.Y.Kung, “VLSI Array Processors”, Prentice-Hall, 1988.

Reference Books:

1. Terri Fiez & Mohammed Ismail “Analog VLSI: Signal and Information Processing” McGraw-Hill, 1994.
2. Durgesh Nandan et al., VLSI Architecture for Signal, Speech, and Image Processing, 2nd Edition, Apple Academic Press, 2023.

e-Resourse:

1. NoC: VLSI Signal Processing: https://nptel.ac.in/courses/108105157

VLSI INTERCONNECTS

Course Overview:

This course covers the analysis, modeling, and design of interconnects in VLSI circuits. Topics include equivalent circuit models, crosstalk and noise effects, techniques for noise reduction, and emerging low-noise interconnect technologies. Emphasis is on optimizing signal integrity, performance, and reliability in modern VLSI designs.

Course Objective:

- To impart knowledge about the importance of electrical on-chip interconnects in modern VLSI circuits.
- To introduce the various equivalent circuit models of interconnects and their comparison.
- To understand the Crosstalk effects in the circuits and its analysis.
- To enable the students to understand the advanced techniques to reduce interconnect noise.

Course Outcomes:

- Develop the ability to analyze and design electrical interconnects using equivalent circuit models.
- Understand crosstalk effects in VLSI circuits and analyze their impact on signal integrity.
- Learn techniques to reduce interconnect noise and improve circuit performance.
- Understand emerging interconnect technologies that exhibit very low interconnect noise.

UNIT- I

Introduction to VLSI interconnects classification, Cu Interconnect, Technological trends, Interconnect scaling, Typical interconnect structure, Electromigration phenomenon, Signal transmission on interconnects, On-chip Interconnects, Package level interconnections.

UNIT-II:

Extraction of interconnect parameters, Physics of interconnects in VLSI, physical foundations for circuit models of VLSI interconnects, Interconnect resistance, capacitance, inductance modelling, Extended Miller effect, Alternatives for extraction. Modelling interconnect drivers. Loss and Lossless transmission line model, Switch-level RC model. T and π network inter connect model. Effective capacitance modelling. Modelling interconnect wires. General interconnect network. An RC tree. The transfer function. Convolution of input and impulse response. Moments of the transfer function. Impulse and step response of RC tree. Elmore delay. Response of single RC. Elmore delay of 2-stage RC. RCtree. Step response of lumped vs. distributed RC line. Sample RLC network. Modified node analysis equations.

UNIT-III:

Active and Passive interconnections, multi-level and multi-layer interconnections, Propagation delays, Crosstalk effects in digital circuits, spurious signals, crosstalk induced delay, energy dissipation due to cross talk, crosstalk effects in VLSI circuits.

UNIT-IV:

Techniques for avoiding interconnection noise, noise detection problem, brief introduction to the testing of logic circuits, Crosstalk configuration, DC noise margins, Crosstalk-induced spurious signal detection, Reasons for high delay uncertainty, switch factor modelling of delay uncertainty.

UNIT-V:

Buffer insertion for noise; Routing topology generation for speed optimization, Width optimization based on separability/monotonicity properties. Introduction to emerging interconnects (CNT, Graphene, optical interconnects and soon).

Text Books:

1. Grabinski, Hartmut, Interconnects in VLSI Design, 1st Edition, Springer, 2000.
2. C-K.Cheng, J. Lillis, S.Lin, N. H. Chang. Interconnect Analysis and Synthesis J. Wiley, 2000.

Reference Books:

1. M.Celik, L.Pillegi, A.Odabasioglu. IC Interconnect Analysis. Kluwer, 2002.
2. A.B.Kahng, G.Robins. On Optimal Interconnections for VLSI. Kluwer, 1995.

e-Resourse:

1. NOC: VLSI Interconnects: **https://nptel.ac.in/courses/108105187**

CMOS RF CIRCUIT DESIGN

Course Objectives:

- To impart knowledge about the RF circuit design and Wireless Technology
- To introduce the fundamental concepts of RF modulation along with RF testing.
- To enable the students to understand th e behavior of BJT and MOSFET at RF frequencies.

Course Outcomes:

- Upon successful completion of the course, the students will be able to
- Understand the basic concepts of RF design, behavior of passive components and RF modulation.
- Realize the behavior of BJT and MOSFET parameters at RF range.
- Design high frequency amplifiers.
- Explain the biasing and referencing in devices at RF range.
- Design RF circuits and explain RF synthesizers.

UNIT-I:

Fundamentals of RF Design and Wireless Technology, Design and applications of RF & wireless systems' Complexity and choice of technology, Basic concepts in RF, design, Nonlinearity and time variance in RF circuits, Inter-symbol interference (ISI),Random processes and noise, Sensitivity and dynamic range, Conversion gains and distortion.

UNIT-II:

RF Modulation and Communication Techniques, RF modulation: Analog and digital modulation of RF circuits, Comparison of modulation techniques for power efficiency, Coherent and non-coherent detection methods, Mobile RF communication basics, Multiple Access techniques: TDMA, FDMA, CDMA, OFDMA, Receiver and Transmitter, architectures, Direct conversion and two-step transmitters.

UNIT-III:

RF Devices and Testing, RF testing: Heterodyne, Homodyne, Image-reject, Direct IF and Sub-sampled receivers, BJT and MOSFE T behavior at RF frequencies, Modeling of transistors and SPICE models, Noise performance and limitations of RF devices, Integrated parasitic elements at high frequencies, Monolithic implementation techniques.

UNIT-IV:

RF Circuit Design and Implementation, Overview of RF filter design, Active RF components &

modeling, Matching and biasing networks, Basic blocks in RF systems and their VLSI implementation, Low-noise amplifier (LNA) design in various technologies, Mixers at GHz frequencies: design and implementations, Oscillators: Basic topologies, Voltage-controlled oscillators (VCOs),Definition of phase noise, Noise power and trade-offs.

UNIT-V:

Advanced RF Systems and Power Amplifier Design, Resonator-based VCO designs, Quadrature and single sideband (SSB) generators, RF synthesizers: PLLs, RF, synthesizer architectures, Frequency dividers, Power amplifier, design, Linearization, techniques for power amplifiers, Design issues in integrated RF filters.

Books and References:

1. Design of CMOS RF Integrated Circuits by Thomas H. Lee, Cambridge University press.
2. RF Microelectronics by Razavi, PHI.
3. CMOS Circuit Design, layout and Simulation by R. Jacob Baker, H.W. Li, D.E. Boyce, PHI.
4. Mixed Analog and Digital Devices and Technology by Y.P. Tsividis, TMH.

QUANTUM COMPUTING

Course Overview:

This course introduces the principles of quantum computation, focusing on the role of qubits and their operations. It covers the analysis of multi-qubit systems, quantum measurement, and entanglement. Students will explore fundamental protocols and develop skills to design quantum algorithms. Hands-on implementation of quantum circuits using suitable platforms is also emphasized**.**

Course Objective:

- Understand the principles of quantum computation qubit.
- Analyze multi-qubit systems and protocols.
- Apply quantum measurement and entanglement concepts.
- Design and implement quantum algorithms and circuits.

Course Outcomes:

- Understand the fundamental principles of quantum computation and qubits.
- Analyze multi-qubit systems, quantum gates, and communication protocols.
- Apply quantum measurement postulates and entanglement concepts for problem-solving.
- Design and implement basic quantum algorithms and circuits using appropriate quantum computing frameworks.

UNIT- I

Review of Quantum Mechanics: Motivation for Quantum Computation Qubit: The qubit state - matrix and Bloch sphere representation - computational basis unitary evolution.

UNIT-II:

Multi-qubit states

No-cloning theorem - Superdense coding - Pure states to Bell states – Bell inequalities. Protocols with multi-qubits: Swapping - Teleportation - gates: CNOT - Toffoli gate - NAND - FANOUT - Walsh Hadamard.

UNIT-III:

Measurement: Projective operators - General, Projective and POVM measure, Ensemble: Density operators - pure and mixed ensemble - time evolution – post measurement density operator. Composite systems: Partial trace - Reduced density operator - Schmidt decomposition, Purification bipartite entanglement.

UNIT-IV:

Quantum computing: Classical computing using qubits - Quantum parallelism - Deutsch's algorithm Deutsch Josza algorithm.

UNIT-V:

Quantum circuits

Basic gates - ABC decomposition - gray codes - Universal gates - Principle of deferred and implicit measurements - Quantum Fourier transform - applications: phase estimation, order finding - factoring, discrete logarithm and hidden subgroup problems - Role of prime factoring in classical cryptography - search algorithms. Quantum error correcting codes, Physical realization of qubits.

Text Books:

1. Chris Bernhardt, Quantum Computing for Everyone, The MIT Press, 2019.
2. Ray LaPierre, Introduction to Quantum Computing, Springer, 2021.

Reference Books:

1. Quantum Theory: Concepts and Methods, Asher Peres, Kluwer Academic Publishers, 1993.
2. Venkateswaran Kasirajan, Fundamentals of Quantum Computing: Theory and Practice, Springer, 2021.

e-Resources:

1. NOC:Quantum Computing: https://nptel.ac.in/courses/104104082

HARDWARE SOFTWARE CO DESIGN

Course Overview:

This course introduces the fundamentals of embedded software co-design, focusing on hardware– software partitioning, co-simulation, and verification techniques. Students will learn methodologies, tools, and languages for building efficient and reliable embedded systems through integrated hardware– software development

Course Objective:

- To introduce the fundamentals of embedded hardware-software co-design principles.
- To understand co-design methodologies, partitioning, and synthesis techniques.
- To explore prototyping, emulation, and system-level design languages.
- To study embedded compilation tools and verification methodologies.
- To gain practical experience with embedded co-design case studies and applications.

Course Outcomes:

- Apply co-design methodologies for embedded software-hardware systems.
- Analyze and partition embedded applications into hardware and software components.
- Design and evaluate co-simulation and co-synthesis techniques for embedded systems.
- Develop and verify embedded applications using co-design tools and languages.

UNIT- I

Co- Design Issues :Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co synthesis.

UNIT-II

Prototyping and Emulation

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure **Target Architectures:**Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT-III:

Compilation Techniques and Tools for Embedded Processor Architectures

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT-IV:

Design Specification and Verification

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, Interface verification.

UNIT-V:

Languages for System-Level Specification and Design-I

System-level specification, design representation for system level synthesis, system level specification languages.

Languages for System-Level Specification and Design-II

Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system..

Text Books:

1.Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers.

Reference Books:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer Publications.

e-Resources:

1.NPTEL : https://nptel.ac.in/courses/106103182

CMOS MIXED SIGNAL CIRCUIT DESIGN LAB

Course Overview: This lab course focuses on the design and implementation of CMOS mixed-signal circuits such as op-amps, comparators, and data converters. Students gain hands-on experience in layout techniques, switched-capacitor circuits, and parasitic extraction using industry-standard tools for real-world applications.

Course Objective:

- To design and implement CMOS mixed-signal circuits for real applications.
- To apply layout techniques for effective mixed-signal circuit integration.
- To develop switched-capacitor circuits for discrete-time signal processing applications.
- To analyze data converter performance and extract parasitics from circuit layouts.

Course Outcomes:

- Design and Implement discrete-time signal processing circuits.
- Apply layout methodologies and design techniques specific for mixed-signal integrated circuits.
- Design operational amplifiers optimized for operation in mixed-signal environments.
- Design high-speed comparators for time-critical mixed-signal application.

Cycle	Syllabus
Cycle 1	1.Fully compensated op-amp with resistor and Miller compensation. 2.Comparator design: a.Linear Response. b.Slew-rate limited.
Cycle 2	3.Switched capacitor circuits: a.Parasitic sensitive integrator. b.Parasitic insensitive integrator. c.Delay free integrators. d.Low Pass filter. 4.Data converters (ADC, DAC for given specifications). 5.Layouts and parasitic extraction..

Text Books:

1. David Johns, Tony Chan Carusone and Kenneth Martin, Analog Integrated Circuit Design, Wiley, 2012, 2nd Edition.
2. Roubik Gregorian and Gabor C.Temes, Analog MOS integrated circuits for signal processing, Wiley, 1986.

Reference Books:

1. Roubik Gregorian, Introduction to CMOS Op-Amp and Comparators, Wiley,1999.
2. Alan Hastings, Theart of Analog Layout, Wiley, 2005

e- Reference:

1. NPTEL Courses https://onlinecourses.nptel.ac.in/noc23_ee142/preview

PHYSICAL DESIGN VERIFICATION LAB

Course Overview: This lab course focuses on implementing and analysing algorithms used in physical design verification of VLSI systems. Students apply graph theory, computational geometry, partitioning, floor planning, and routing techniques to optimize IC layouts using programming and relevant EDA tools.

Course Objective:

To analyze and implement graph algorithms for layout optimization tasks.

To apply computational geometry solving layout challenges in VLSI systems.

To design and optimize partitioning techniques for improved VLSI performance.

To implement floor planning algorithms using modern optimization and constraint-based methods.

Course Outcomes:

Analyze and Implement graph algorithms, focusing on physical design automation applications and optimization.

Apply computational geometry techniques to solve geometric problems in VLSI layout and design.

Design, evaluate, and optimize partitioning algorithms for VLSI design using various techniques.

Implement floor planning algorithms using constraint-based, integer programming, and simulated evolution strategies for optimization.

Syllabus

Cycle 1 :

1. Graph algorithms:
2. Graph search algorithms:
3. Depth first search
4. Breadth first search
5. Spanning tree algorithm:
6. Kruskal’s algorithm
7. Shortest path algorithm:

8. Dijkstra algorithm
9. Floyd-Warshall algorithm
10. Steiner tree algorithm

Cycle 2

2.Partitioning algorithms:

a) Kernighan–Lin algorithm
b) Fiduccias–Mattheyses algorithm
c) Simulated annealing and evolution algorithms

3.Floor planning algorithms:

a) Constraint based methods
b) Integer programming-based methods
c) Rectangular dualization based methods
d) Simulated evolution algorithms

4. Routing algorithms - Two terminal algorithms:

a) Maze routing algorithms:
b) Lee's algorithm
c) Soukup's algorithm
d) Hadlock algorithm
e) Line-Probe algorithm
f) c)Shortest path-based algorithm

Software required: C/C++ Programming Language /Relevant software.

Text Books:

1. Naveed Shervani, Algorithms for Physical Design Automation, 3rd Edition, Kluwer Academic,1998.
2. Charles J Alpert, Dinesh P Mehta, Sachin S. Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press,2008.