Code No: R203104Q **R20** SET - 1

III B. Tech I Semester Regular/Supplementary Examinations, December -2023
DIGITAL LOGIC DESIGN
(Com to CSE,IT)

Time: 3 hours Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
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UNIT-I

1. a) Perform the binary subtraction using2's complement method and 1's complement method. $(1001)_2 - (1010)_2$. [7M]
   b) Convert the following i)$AB_{16}=()_{10}$ ii)$1234_8=()_{10}$ iii)$772_{10}=()_{16}$. [7M]

(OR)

2. a) Convert the given expressions in standard SOP form [7M]
   i)f(A,B,C)=A+AB+CB ii)f(P,Q,R)=PQ+R+PR
   b) State and prove the following laws of Boolean algebra. [7M]
   i)Commutative ii) associative iii)distributive

UNIT-II

3. a) Simplify the following function using K-Map:F(A,B,C,D)=Σ(0,2,3,8,10,11,12,14) [7M]
   b) Implement Carry look-a-head adder circuit and explain its operation briefly. [7M]

(OR)

4. a) Design a full adder by using two half adders. [7M]
   b) Simplify the following function using K-Map:F(A,B,C,D,E)=Π(0,1,6,7,8,9,21,22,23,29,31) [7M]

UNIT-III

5. a) Design a 4:16decoder with basic gates. [7M]
   b) Draw the pin diagram and obtain the truth table of IC7485? [7M]

(OR)

6. a) Design a combinational circuit for a 2-bit magnitude comparator. [7M]
   b) Design a 4 to 2 priority encoder. [7M]

UNIT-IV

7. a) Classify Shift Registers? Design and Explain any one of the Shift Registers. [7M]
   b) Design mod-10 counter with JK flip-flops. [7M]

(OR)

8. a) What is Race condition and explain about the operation of clocked RS flip-flop. [7M]
   b) Convert the JK Flip-flop in to RS flip-flop. [7M]

UNIT-V

9. a) Design a finite state machine which can detect the sequence 0010 by using JK flip-flop. [7M]
   b) Explain the designing steps to convert Mealy machine to Moore machine. [7M]

(OR)

10. a) Explain the differences between Mealy and Moore Machine. [7M]
    b) What is a Finite State Machine? Explain the capabilities and limitations of Finite State Machine. [7M]

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Code No: R203104Q **R20** SET - 2

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DIGITAL LOGIC DESIGN
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Time: 3 hours Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
*****

UNIT-I

1. a) Convertthefollowingnumbersi)$(53)_{10}=()_2$ii)$(231)_4=()_{10}$iii)$(1101101)_2=($ $)_8$iv)$(4D.56)_{16}=()_2$ [7M]
   b) Perform the following arithmetic operation using1's and 2's complement methods: $(1101110)_2-(10101)_2$. [7M]

(OR)

2. a) Simplify the following [7M]
   (i)$AB+BC+A^1C=AB+A^1C$ (ii)$(X+Y).(Y^1+Z)=X$
   b) Draw the pin Diagram and truth table of 7400 [7M]

UNIT-II

3. a) Simplify the following function using K-Map:$F(A,B,C,D)=\Pi(0,1,2,3,5,7,11)$ [7M]
   b) Implement a 4 bit Binary to Gray code converter. [7M]

(OR)

4. a) Simplify the following function usingK-Map:$F(A,B,C,D,E)=\Sigma(0,2,4,7,8,10,12,16,18,20,23,24,25,26,27,28)$ [7M]
   b) Design a full subtract or by using two half sub tractors. [7M]

UNIT-III

5. a) What is a decoder? Explain a 4:16 decoder with a truth table and logic diagram. [7M]
   b) Implement the following Boolean function using 4:1Mux:$F(A,B,C,D)=\Sigma(0,2,3,6,11,13,15)$ [7M]

(OR)

6. a) Design a priority encoder of 4-bit. [7M]
   b) Draw the pin diagram and obtain the truth table of IC74154. [7M]

UNIT-IV

7. a) Design a 4bit shift left register using flip flops. [7M]
   b) Discuss in detail about sequential circuits with examples. [7M]

(OR)

8. a) Explain universal shift registers with truth tables. [7M]
   b) Design a Mod-10 counter with T flip-flops. [7M]

UNIT-V

9. a) Define Finite State Machine. Explain the State diagram representation in Mealy and Moore Models with suitable example. [7M]
   b) Explain the capabilities and limitations of Finite State Machine. [7M]

(OR)

10. a) Explain the designing steps to convert Mealy machine to Moore machine. [7M]
    b) Design a finite state machine which can detect 0011. [7M]

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Code No: R203104Q **R20** SET - 3

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Time: 3 hours Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
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UNIT-I

1. a) Convert the following to required form i)$(163.789)_{10}=()_8$ ii)$(101101110001.00101)_2=()_{10.}$ iii)$(292)_{16}=()_{2.}$ [7M]
   b) Perform the given subtraction using1's and2's complement methods:$(10110)_2$-$(1101101)_2$. [7M]

(OR)

2. a) Reduce the following Boolean expressions. i)AB+A(B+C)+B(B+C). ii)ABEF+AB(EF)′+(AB)′EF. iii)A′B′+A′BC′+A′BCD+A′BC′D′E. [7M]
   b) Write the Postulates and theorems of Boolean Algebra. [7M]

UNIT-II

3. a) Simplify the following 6 Variable function using K-Map:F=Σ(0,5,7,8,9,12,13,23,24,25,28,29,37,40,42,44,46,55,56,57,60,61) [7M]
   b) Implement a 4 bit BCD to Binary code converter. [7M]

(OR)

4. a) Simplify the following function using Tabular method: F(A,B,C,D)=Π(2,4,5,9,12,13) [7M]
   b) Implement a 4 bit Binary to BCD code converter. [7M]

UNIT-III

5. a) Explain 16x1 multiplexer with the help of truth table and logic diagram. [7M]
   b) Draw the circuit diagram of a full subtract or using NOR gates. [7M]

(OR)

6. a) What is decoder? Construct a 4:16 decoder with two 3:8 decoders. [7M]
   b) Implement the following Boolean function using4:1Mux:F(A,B,C,D)=Σ(1,2,5,8,9,12,14) [7M]

UNIT-IV

7. a) Convert the JK flip-flop to T flip-flop. [7M]
   b) What is race around condition? Explain how is it eliminated in master-slave flip-flops with diagram? [7M]

(OR)

8. a) Draw an eat circuit diagram of an egativeedgetriggered JK flip-flop and explain its operation. [7M]
   b) Draw the circuit diagram of 4-bit Johnson counter using D flip-flop and explain [7M]

UNIT-V

9. a) What is a Finite State Machine? Explain the capabilities and limitations of Finite State Machine. [7M]
   b) Design a finite state machine which can detect 0111. [7M]

(OR)

10. a) List out the designing steps to convert Moore machine to Mealy machine? [7M]
    b) Explain the differences between Mealy and Moore Machine? [7M]

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Code No: R203104Q **R20** SET - 4

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Time: 3 hours Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
*****

UNIT-I

1.	a)	Convert the following numbers. i)$(10101100111.0101)_2$toBase10. ii)$(153.513)_{10}$to base8.	[7M]
	b)	Represent the decimal numbers 0 to 7,-7 to-1insigned magnitude, 1's complement, 2's complement forms using4-bits.	[7M]
		(OR)	
2.	a)	Obtain the canonical sum of product form of f=A'BC+B'C'(A+D) and f=A(C+D')+BC'	[7M]
	b)	Express the following function is sum of minterms and product of maxterms. F(A,B,C,D)= B'D+A'D+BD	[7M]

UNIT-II

3.	a)	Simplify the following 5 Variable function using K-Map:F=Σ(0,2,3,5,7,8,10,11,14,15,16,18,24,26,27,29,30,31)	[7M]
	b)	Design a 4 bit adder-subtract or circuit and explain its operation.	[7M]
		(OR)	
4.	a)	Simplify the following function using Tabular method: F(A,B,C,D)=Σ(0,2,3,6,7,8,10,12,13)	[7M]
	b)	Implementa4 bit Gray to Binary code converter.	[7M]

UNIT-III

5.	a)	Implementa4-bitdigitalcomparatorand explainitsoperation.	[7M]
	b)	Distinguish between PROM, PLA and PAL.	[7M]
		(OR)	
6.	a)	Implement aseven segment decoderandexplain its operation.	[7M]
	b)	What is ade-multiplexer? Constructa1:8de-multiplexerwithtwo1:4 de-multiplexers.	[7M]

UNIT-IV

7.	a)	Distinguish between combinational logic and sequential logic.	[7M]
	b)	Design a 4-bitripplecounter using T-flip-flop. Explain using waveforms.	[7M]
		(OR)	
8.	a)	Explain the working of a 4-bitregister which uses parallel load with alogic diagram.	[7M]
	b)	Design a 4-bit Johnson counter using T-flop flops and draw the circuit diagram and timing diagrams.	[7M]

UNIT-V

9.	a)	What is a Finite State Machine? Explain the capabilities and limitations of Finite State Machine.	[7M]
	b)	Design a finite state machine which can detect 0011	[7M]
		(OR)	
10.	a)	Differentiate the mealy machine and Moore machine.	[7M]
	b)	Discuss the process to convert Moore machine to Mealy machine?	[7M]

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