Code No: R2032042 **R20** SET -1

III B. Tech II Semester Supplementary Examinations, December -2023
VLSI DESIGN
(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
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UNIT-I

1. a) Draw the VLSI design flow diagram and explain. [7M]
   b) Determine the pull up to pull down ratio for NMOS inverter driven by one or more pass transistor inverter. [7M]

(OR)

2. a) With neat diagrams, explain the different steps in p-well fabrication of CMOS transistors. [7M]
   b) Draw the circuit diagram of CMOS inverter and explain its operation. [7M]

UNIT-II

3. a) What is meant by sheet resistance R_s? Explain the concept of R_s applied to MOS transistors. [7M]
   b) Calculate on resistance of an inverter from V_{DD} to GND. If n- channel sheet resistance R_{sn}=104 Ω per square and P-channel sheet resistance $R_{sp} = 3.5 \times 10^4$ Ω per square. (Z_{pu}=4:4 and Z_{pd}=2:2). [7M]

(OR)

4. a) What is inverter delay? How delay is calculated for multiple stages? Explain. [7M]
   b) Two nMOS inverters are cascaded to drive a capacitive load $C_L=16C_g$. Calculate pair delay V_{in} to V_{out} in terms of τ. [7M]

UNIT-III

5. a) Draw a standard Cascode current sink circuit and explain its operation and output characteristics. [7M]
   b) Write a short note on following: (i) Body bias effect (ii) Source degeneration of common source amplifier. [7M]

(OR)

6. a) Derive the expressions for input impedance, voltage gain and output impedance of common drain amplifier. [7M]
   b) Explain about single stage amplifiers with resistive load. [7M]

UNIT-IV

7. a) Model the static CMOS layout for the expression F= (A+B)'. [7M]
   b) Develop a 2-input XOR gate using pass transistor logic. [7M]

(OR)

8. a) Explain the following: (i) Static power dissipation (ii) Dynamic power dissipation. [7M]
   b) Briefly discuss about Master-Slave based edge triggered register with a neat diagram. [7M]

UNIT-V

9. a) Draw and explain the FPGA design flow. [7M]
   b) Discuss different types of programming technologies used in an FPGA design. [7M]

(OR)

10. a) Explain about High – k metal technology. [7M]
    b) Write a short note on Giga scale dilemma. [7M]

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