**Code No: 138EW** **R16**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**
**B. Tech IV Year II Semester Examinations, July - 2021**
**SYSTEM DESIGN USING FPGAS**
**(Electronics and Communication Engineering)**

**Time: 3 hours** **Max. Marks: 75**

**Answer any Five Questions**
**All Questions Carry Equal Marks**
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1.a) Design a T-flip flop using D-flip flop and implement the same in VHDL. Also draw the Schematic.
b) Discuss the design of four, two input NAND gate using different VHDL statement. Also obtain the synthesized schematic for NAND gate. [8+7]

2.a) Write the VHDL code for octal to binary encoder using RTL3 architecture. Also Synthesize the VHDL code.
b) Synthesize equal VHDL code for all architectures N => 16. Compare the synthesis results. [8+7]

3.a) Design a 4-bit bidirectional shift register using RTL3 architecture. Also synthesize the VHDL code.
b) Implement a 40-bit DMA starting word address register using VHDL. [8+7]

4.a) Implement the design of divided-by-3 clock divider circuit using VHDL code.
b) Write the VHDL code for a counter controlled by enable signal and the flip flops do not have a gated clock input. List out the disadvantages of not having the gated clock. [8+7]

5.a) If the place and route tool has the clock synthesis capability, What are the changes that need to be done to VHDL code take advantage of it?
b) In FIRCHIP plot I/O pads are placed on the boundary. The position of these I/O pads are certain to relate to the position of the package pins. What factors are to be considered for selecting a package for the design. [7+8]

6.a) Obtain the VHDL code for 4×1 Multiplexer using AND-OR gates along with schematic.
b) Define a design directory structure for a design by two or more designers. State the assumptions, guidelines, usages, advantages and purposes. [8+7]

7.a) Design a 4-bit magnitude comparator using RTL4 architecture. Also draw the synthesized schematic for RTL4.
b) A zero detector is similar to equality checker except that the constant has every bit '0'. Write VHDL code for zero detector and also synthesize the code. [8+7]

8.a) How can the data be transferred in an Universal Synchronous Transmitter and Receiver. Write the VHDL code and also draw the synthesized schematic. Also analyze the timing path required for each input.
b) The functional vector for the fabrication vendor are required to test after fabrication. Develop a process to incorporate that format in to design environment. [8+7]

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