Code No: 138AQ **R16**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech IV Year II Semester Examinations, July - 2021
ANALOG CMOS IC DESIGN
(Electronics and Communication Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any Five Questions
All Questions Carry Equal Marks
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1.a) Deduce the small signal model for an n-channel MOSFET taking into account the body effect.
b) Derive an expression for g_m of an N-channel MOS FET operating in linear and saturation regions. [7+8]

2.a) Explain how to realize Resistor using Active devices.
b) Consider a source follower which is biased by a current mirror. The dimensions of all the transistors are 100µm/1.6µm, $\mu_n C_{ox}$ = 90µA/V^2, $\mu_p C_{ox}$ = 30µA/V^2, I_{bias} = 100µA, $\gamma_n = 0.5V^{1/2}$, $r_{dx\text{-}n}$ = 8000L(µm)/I_D(mA). What is the gain of the stage? [7+8]

3.a) Explain how power-supply sensitivity can be reduced in bootstrap bias technique.
b) Design a second order Butterworth low pass filter with a cutoff frequency of 500 Hz and a pass band gain of -2. Assume that a 5V ± power supply and a CMOS clock are used. [7+8]

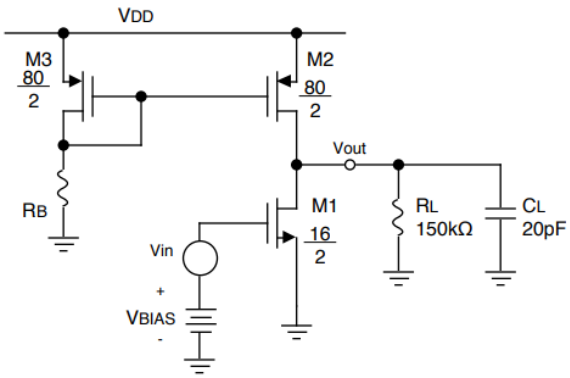
4.a) Why is emitter resistor R_E replaced by a constant current bias circuit in differential amplifier stage of an op-AMP? Explain.
b) Design the dual input balanced output differential amplifier with the current mirror bias according to the following specifications:
i) Supply voltage Vs = ±12V
ii) Maximum output voltage swing – 7Vpp. [7+8]

5. Discuss in detail the compensation of OP amp that makes it completely independent of process and temperature variations. [15]

6.a) With neat sketch and necessary equations explain the design aspect of a two-stage open loop comparator for slewing response.
b) Give an account of charge injection errors in connection with comparators and suggest a method to minimize the same. [7+8]

7.a) Explain about the Bipolar simple current mirror with degeneration helper with necessary equations.

b) Determine the DC gain and 3-dB bandwidth frequency for the circuit with the load impedance of 150kΩ || 20pF added to the output. [7+8]



8. Choose values of V_{GS} = 1,2,3,4 and 5V, assume that the channel modulation parameter is zero. Sketch to scale the output characteristics of an enhancement n-channel device if V_T = 0.7V and I_D = 500μA when V_{GS} = 5 V in saturation. [15]

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