R18

Code No: 156DF

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech III Year II Semester Examinations, February/March - 2022
VLSI DESIGN
(Electronics and Communication Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
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1. Explain the following:
   a) Transconductance g_m
   b) Figure of merit w_o
   c) Pass transistor. [5+5+5]

2.a) Derive the expression for the threshold voltage of MOSFET.
   b) Derive the expression for transfer characteristics of CMOS Inverter. [8+7]

3.a) Explain steps in VLSI Design flow.
   b) Design a Stick Diagram for 2-input nMOS NAND gate. [8+7]

4.a) Explain 2µm CMOS design rules for wires.
   b) Draw the Layout Diagrams for NOR and XOR Gate. [7+8]

5.a) Explain the model for deviation of time delay.
   b) Describe three sources of wiring capacitances. Explain the effect of wiring capacitance on the performance of a VLSI circuit. [7+8]

6. Define the following and explain the significance of each term in VLSI circuits:
   a) Fan in and Fan out
   b) Choice of layers. [7+8]

7.a) Design a 4-bit Parity generator and draw its logic diagram.
   b) Explain the operation of SRAM cell with its construction. [8+7]

8.a) What is CPLD? Draw its basic structure and give its applications.
   b) Explain about system level test techniques in detail. [8+7]

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