Code No: 154AN **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year II Semester Examinations, March - 2022
DIGITAL ELECTRONICS
(Electrical and Electronics Engineering)

Time: 3 Hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
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1.a) Perform arithmetic operation using 2's complement method.
i) -70 – 85 ii) 130 – 65
b) How to interface CMOS and TTL gates.
c) What are the advantages of Tri-state logic? [7+4+4]

2.a) Simplify the Boolean expression using K-map and draw the logic diagram.
$F(A,B,C,D) = \sum M(0,1,5,12,1,3,15)+d(1,3,6)$
b) Realise a full adder using the 3×8 decoder. [8+7]

3.a) Develop the logic circuit diagram and table for 4-bit ring counter and explain the working.
b) What is a glitch? Design and show the timing diagram for a Mod 6 asynchronous counter showing the glitches in the diagram. [6+9]

4.a) With a neat block schematic, describe the working of a successive approximation ADC and illustrate it with a suitable example.
b) Explain the working of Flash type ADC. [10+5]

5.a) Bring out the differences between a PAL and PLA.
b) Implement $F = \sum m(2,3,4,5,7)$ using PAL.
c) Compare CPLDs and FPGAs. [5+5+5]

6.a) Distinguish between Sequential and combinational circuits.
b) Design a mod-11 asynchronous counter using T flip flops and discuss its disadvantages. [5+10]

7.a) What are fast adders? Design a 4 bit, carry look ahead adder, showing the logical diagram.
b) Design a BCD to decimal decoder. [8+7]

8.a) Compare the characteristics of TTL and CMOS logic families.
b) Minimize the Boolean expression $F=AB'C'+C'D+BD'+A'C$ using K-map and implement the logic circuit using NAND gates only. [6+9]

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