

Code No: 153AT

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech II Year I Semester Examinations, March - 2022

ELECTRONIC DEVICES AND CIRCUITS

(Common to ECE, EIE, MCT)

Time: 3 Hours

Max. Marks: 75

Answer any five questions

All questions carry equal marks

- 1.a) With a neat circuit diagram, Explain the operation of Full Wave Rectifier with Capacitor filter.
- b) A Half Wave Rectifier circuit supplies 100 mA DC current to a $250\ \Omega$ load. Find the DC output voltage, PIV rating of the diode and rms voltage for the transformer supplying the rectifier. [9+6]
- 2.a) State and prove Clamping Circuit Theorem.
- b) An unsymmetrical square wave with $T_1 = 1\text{ msec}$ and $T_2 = 1\ \mu\text{sec}$ has an amplitude of 10 V. This signal is applied to the restorer circuit of figure 1, in which $R_f = 50\ \Omega$, $R = 50\ \text{K}\Omega$. Assume that the capacitor C is arbitrarily large, so that the output is a square wave without tilt. Find where, on the waveform, the zero level is located. [8+7]

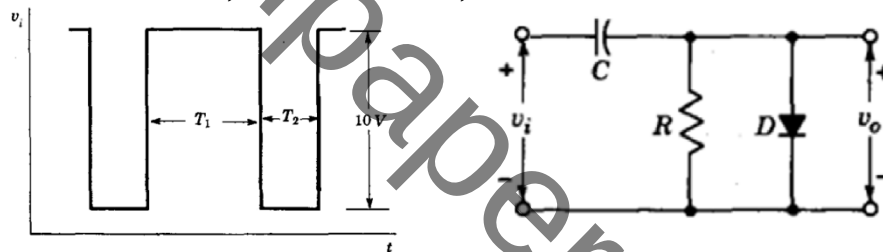


Figure: 1

- 3.a) Draw and explain the input and output characteristics of BJT in CE configuration.
- b) In the circuit shown in figure 2, with $\beta = 100$. Determine I_{CQ} , V_{CEQ} and draw the DC load line. [8+7]

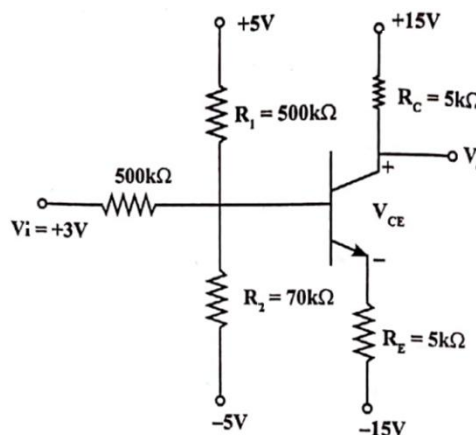


Figure: 2

- 4.a) Explain the working of the transistor as a switch.
- b) In a silicon transistor with a fixed bias, $V_{CC} = 9\text{ V}$, $R_C = 3\text{ k}\Omega$, $R_B = 8\text{ k}\Omega$, $\beta = 50$, $V_{BE} = 0.7\text{ V}$. Find the operating point and stability factor S . [7+8]
- 5.a) Illustrate the construction and principle of operation of JFET with necessary diagrams.
- b) A FET follows the relation $I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$. What are the values of I_D and g_m for $V_{GS} = -1.5\text{ V}$ if I_{DSS} and V_P are given as 8.4 mA and -3 V respectively?
- c) State any three differences between JFET and BJT. [7+4+4]
- 6.a) Explain the construction of SCR with neat diagram. Draw its V-I characteristics.
- b) Determine the value of R_L that will establish maximum power conditions for the zener diode shown in circuit shown in figure 3. [8+7]

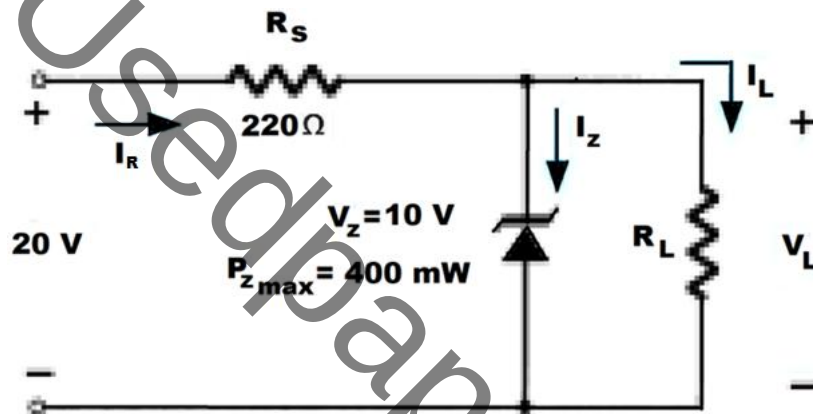


Figure: 3

- 7.a) Draw the h-parameter equivalent circuit for a typical common base amplifier and derive expression for A_i , A_v , R_i and R_o .
- b) In the CE amplifier calculate the mid frequency voltage gain and lower 3-dB point. The transistor has h-parameters $h_{fe} = 400$ and $h_{ie} = 10\text{ k}\Omega$, the circuit details are $R_s = 600\text{ }\Omega$, $R_L = 5\text{ k}\Omega$, $R_e = 1\text{ k}\Omega$, $V_{CC} = 12\text{ V}$, $R_1 = 15\text{ k}\Omega$, $R_2 = 2.2\text{ k}\Omega$ and $C_e = 50\text{ }\mu\text{F}$. [8+7]
- 8.a) Draw the transfer and drain characteristics of MOSFET and explain the three regions of operation of a MOSFET.
- b) Derive an expression for voltage gain, input impedance and output impedance of CG amplifier at low frequencies. [7+8]

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