Code No: 153AN

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year I Semester Examinations, March - 2022
DIGITAL SYSTEM DESIGN
(Electronics and Communication Engineering)

Time: 3 Hours   **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
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1.a)   Solve for x
   i) $(257)_8 = (x)_2$ ii) $(21.625)_{10} = (x)_8$ iii) $(BC.2)_{16} = (x)_8$ iv) $(33)_{10} = (201)_x$
  b)   Obtain dual of the following Boolean expressions
   (i) $AB+A(B+C)+B'(B+D)$ (ii) $A+B+A'B'C$.   [8+7]

2.a)   Express the Decimal Digits 0-9 in BCD, 2421, 84-2-1 and Excess-3.
  b)   Using the tabular method, obtain the minimal expression for
   $F = \sum m(6, 7, 8, 9) + \sum d(10, 11, 12, 13, 14. 15)$.   [7+8]

3.a)   Minimize the following expression using K-map and realize using NAND Gates.
   $F(A,B,C,D) = \sum m(1,3,7,11,15) + \sum d(0,2,5)$.
  b)   Construct a full adder using only two half adders and one OR gate.   [8+7]

4.a)   With the aid of external logic, convert D type flip-flop to a JK flip-flop.
  b)   Design a synchronous modulo-12 counter using JK flip-flop.   [5+10]

5.a)   Find the characteristic equation for:
   i) T flip-flop   ii) D flip-flop
  b)   Draw and explain the operations of 4-bit universal shift register.   [8+7]

6.a)   Draw and explain the modulo N –counters.
  b)   Explain concept of minimal cover table.   [10+5]

7.a)   Discuss about the approaches of designing synchronous sequential finite state machines.
  b)   Design a 1101 sequence detector and draw its logic diagram.   [5+10]

8.   Write a short note on followings:
   a) CMOS transmission gate
   b) Tristate TTL
   c) AND, OR gates using DTL.   [5+5+5]

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