Code No: R193202E **R19** **SET - 1**

III B. Tech II Semester Regular Examinations, June-2022

VLSI DESIGN

(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
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UNIT-I

1. a) Outline the DC transfer characteristics of CMOS inverter. [8M]
   b) An nMOSFET is operating in saturation region with the following parameters: [7M]
   V_{GS} = 5 V, V_{tn} = 1.1 V, W/L = 120, $\mu_n C_{ox}$ = 120 µA/V
   Find the Drain resistance of the device.

(OR)

2. a) Describe the operation of enhancement mode NMOS transistor using its characteristics. [8M]
   b) Realize CMOS inverter and describe its operation. [7M]

UNIT-II

3. a) Summarize the fabrication steps of N Well process with neat diagram. [8M]
   b) What is the need of oxidation process in MOS transistor fabrication and list the types of oxidations. [7M]

(OR)

4. a) List the typical fabrication steps involved in MOS transistor fabrication. [8M]
   b) Compare diffusion and ion implantation. [7M]

UNIT-III

5. a) Model the static CMOS layout for the expression F= (A+B)'. [8M]
   b) Develop a 2-input XOR gate using pass transistor logic. [7M]

(OR)

6. a) Construct the stick diagram for NMOS NAND gate. [8M]
   b) Design two bit comparator using Pass transistor or Transmission gate. [7M]

UNIT-IV

7. a) Develop the SR Latch with true single phase clock systems. [8M]
   b) Design DFF using Transmission gate. [7M]

(OR)

8. a) Demonstrate the sources of clock skew with neat diagrams. [8M]
   b) Illustrate the operation of single transistor DRAM cell. [7M]

UNIT-V

9. a) Define simulation and list the possible types of simulations in ASIC design. [8M]
   b) Describe Floor planning using diagram of ASIC design sequence. [7M]

(OR)

10. a) Draw the ASIC design flow and describe the backend design process. [8M]
    b) Define circuit extraction, in which stage of the ASIC design flow circuit extraction is the best. [7M]

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