Code No: R1932042 **R19** **SET - 1**

III B. Tech II Semester Regular Examinations, June-2022

VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions **ONE** Question from **Each unit**

All Questions Carry Equal Marks

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UNIT-I

1. a) Derive an expression for transconductance of an n-channel enhancement MOSFET operating in active region. [8M]
   b) Derive I_d-V_{ds} relationship of MOS in Resistive region. [7M]

(OR)

2. a) Draw the VLSI design flow diagram and explain. [8M]
   b) Explain about 2μm CMOS design rules and discuss with layout examples. [7M]

UNIT-II

3. a) Design a 2-input Ex-OR using CMOS Transmission gate. [8M]
   b) Describe about methods for driving large capacitive loads. [7M]

(OR)

4. a) Describe the following: [8M]
   (i) Pseudo NMOS logic (ii) Domino CMOS Logic
   b) Discuss about choice of fan-in and fan-out selection in gate level design. [7M]

UNIT-III

5. a) What is current mirror? Explain the general properties of current mirror with block diagram. [8M]
   b) Explain the operation of single stage amplifier with resistive load. [7M]

(OR)

6. a) What is the common-drain amplifier? How do you find the voltage gain of a common-drain amplifier? [8M]
   b) Elaborate the principle of operation of an n-channel enhancement MOSFET and discuss the conditions for different regions of operation of MOSFET. [7M]

UNIT-IV

7. a) Write a short notes on: [8M]
   (i) Ratioed Circuits (ii) Dynamic Circuits
   b) Describe pass transistor briefly with example. [7M]

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(OR)

8. a) Explain the following: [8M]
(i) Static power dissipation (ii) Dynamic power dissipation
b) Briefly discuss about Master-Slave based edge triggered register with a neat diagram. [7M]

UNIT-V

9. Illustrate with a neat architecture diagram about various functional blocks of FPGAs. [15M]

(OR)

10. a) Draw the FPGA design flow and explain. [8M]
b) Explain about FinFET technology. [7M]

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Code No: R1932042 **R19** **SET - 2**

III B. Tech II Semester Regular Examinations, June-2022

VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
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UNIT-I

1. a) Draw and Explain about BiCOMS inverter. [8M]
   b) Draw the schematic diagram, stick diagram and layout of 2-input CMOS NAND gate. [7M]

(OR)

2. a) Determine the pull up to pull down ratio for NMOS inverter driven by another NMOS inverter. [8M]
   b) Analyze CMOS inverter with its transfer characteristics. [7M]

UNIT-II

3. a) Describe the following: [8M]
   (i) Dynamic CMOS logic (ii) np CMOS Logic
   b) Explain following: [7M]
   (i) Fan-in (ii) Fan-out (iii) Choice of layers

(OR)

4. a) What are the alternate gate circuits available? Explain any one of them with suitable sketch by taking NAND gate as an example. [8M]
   b) Explain different wiring capacitances used in gate level design with an example. [7M]

UNIT-III

5. a) Write a short note on Current sources and sinks. [8M]
   b) Explain the operation of single stage amplifier with diode connected load. [7M]

(OR)

6. a) Derive the expressions for input impedance, voltage gain and output impedance of common source amplifier with source resistor. [10M]
   b) Explain about body bias effect. [5M]

UNIT-IV

7. a) Write and explain about the sources of power dissipation in VLSI design. [8M]
   b) How switch logic can be implemented using pass transistors? Explain? [7M]

(OR)

8. a) Explain about deep submicron processes with suitable schematic diagrams. [8M]
   b) Explain about Master-Slave Edge-Triggered Register. [7M]

UNIT-V

9. a) List out the different families of FPGAs. Explain how they are differing. [8M]
   b) Explain in detail about TFET technology. [7M]

(OR)

10. a) Explain about High – k metal technology. [8M]
    b) Draw the FPGA design flow and explain. [7M]

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Code No: R1932042 **R19** **SET - 3**

III B. Tech II Semester Regular Examinations, June-2022

VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
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UNIT-I

1. a) What are the steps involved in CMOS n-Well Fabrication? Explain with neat sketches. [8M]
   b) Explain design rules for layouts. [7M]

(OR)

2. Determine the pull up to pull down ratio for NMOS inverter driven by one or more pass transistor inverter. [15M]

UNIT-II

3. a) What is meant by sheet resistance Rs? Explain the concept of Rs applied to MOS transistors. [8M]
   b) Design a 2-input Multiplexer using CMOS Transmission gate. [7M]

(OR)

4. a) Implement Ex-OR logic gate using CMOS logic. [8M]
   b) Explain the concept of delay estimation and sizing of MOSFET. [7M]

UNIT-III

5. a) Draw a standard Cascode current sink circuit and explain its operation and output characteristics. [8M]
   b) Write a short note on following: [7M]
      (i) Body bias effect
      (ii) Source degeneration of common source amplifier.

(OR)

6. a) Derive the expressions for input impedance, voltage gain and output impedance of common drain amplifier. [10M]
   b) Explain about modelling of a transistor. [5M]

UNIT-IV

7. a) With the help of a diagram, explain SR Master-Slave register. [8M]
   b) Explain importance of Set up and hold time in the analysis of CMOS circuit. [7M]

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(OR)

8. a) Design a NOR gate using pass transistor logic. [8M]
   b) Define and explain the concept of Metastability. [7M]

UNIT-V

9. a) What is FPGA? Draw its structure and also write its advantages. [8M]
   b) With a neat sketch explain the CLB, IOB and programmable interconnects of an FPGA design. [7M]

(OR)

10. a) Write a short note on Giga scale dilemma. [8M]
    b) Explain about High–k metal technology. [7M]

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Code No: R1932042 **R19** **SET - 4**

III B. Tech II Semester Regular Examinations, June-2022

VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
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UNIT-I

1. a) Draw the circuit diagram for CMOS inverter and explain the transfer characteristics using necessary equations, and the different regions in the characteristics. [8M]
   b) What is meant by latch up? How can it be eliminated? [7M]

(OR)

2. a) Explain λ based design rules in VLSI circuit. [8M]
   b) Draw the stick diagram for 3 input NAND gate. [7M]

UNIT-II

3. a) Calculate ON resistance of an inverter from VDD to GND. If n- channel sheet resistance R_{sn} = 104 Ω per square and P-channel sheet resistance R_{sp} = 3.5 × 104 Ω per square. (Z_{pu}=4:4 and Z_{pd}=2:2). [8M]
   b) Draw circuits using CMOS, pseudo NMOS and DCVS for the given function $OUT = \overline{D + A \bullet (B + C)}$. [7M]

(OR)

4. a) Classify different types of MOS scaling. Derive their effects on various parameters of MOSFET. [8M]
   b) Design a 2-input Ex-NOR using CMOS Transmission gate. [7M]

UNIT-III

5. a) Derive the expressions for input impedance, voltage gain and output impedance of common source amplifier. [8M]
   b) Write a short note on current sources and sinks. [7M]

(OR)

6. a) Why do we use common-drain amplifier? How do you calculate voltage gain and current gain of common-drain amplifier? [8M]
   b) Tabulate the differences between common-source amplifier and common-drain amplifier. [7M]

UNIT-IV

7. a) Explain the concept of pipelining used to optimize sequential circuits. [8M]
   b) Explain about Mux based Latches with an example. [7M]

(OR)

8. a) Explain about Master slave register. [8M]
   b) With neat diagrams, explain cross coupled NAND and NOR gates. [7M]

UNIT-V

9. a) Explain the step-by-step approach of the FPGA design process in the Xilinx environment. [8M]
   b) Write a short note on Giga scale dilemma. [7M]

(OR)

10. a) Explain about TFET technology. [8M]
    b) Write notes on short channel effects. [7M]

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