

III B. Tech II Semester Supplementary Examinations, February-2022

VLSI DESIGN

(Common to ECE, EIE, E.COM.E)

Time: 3 hours

Max. Marks: 70

- Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
 2. Answer **ALL** the question in **Part-A**
 3. Answer any **FOUR** Questions from **Part-B**

PART -A**(14 Marks)**

1. a) When the channel is said to be pinched-off? [2M]
- b) Give the various color coding used in stick diagram. [3M]
- c) Give the scaling factor for current density (J) in terms of different scaling models. [3M]
- d) Explain the gate level and function level testing. [2M]
- e) What is CLB? [2M]
- f) Give the expression for dynamic power consumption. [2M]

PART -B**(56 Marks)**

2. a) Explain the process of CMOS fabrication with suitable sketch. [7M]
- b) Define threshold voltage of a MOS device and explain its significance. [7M]
3. a) What is a stick diagram? Draw the stick diagram and layout for an nMOS inverter. [7M]
- b) Explain about design rule check. Why is it employed? [7M]
4. a) Derive the expressions for rise time and fall time in the case of CMOS inverter. [7M]
- b) Why scaling is required? Write the scaling factors for different types of device parameters. [7M]
5. a) Give the Architecture of a boundary scan test and explain the same. [7M]
- b) Explain the different categories of DFT techniques. [7M]
6. a) What are FPGAs? Explain the principle and operation. [7M]
- b) List out the important features of Altera Flex 8000FPGA. [7M]
7. a) Explain the techniques used for reduction of switching capacitance. [7M]
- b) With the help of neat diagrams explain about power grid and clock design. [7M]

