Code No: R163202C **R16** SET - 1

III B. Tech II Semester Supplementary Examinations, February-2022

VLSI DESIGN

(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A **(14 Marks)**

1.	a)	Build a circuit for NAND gate using pass transistor.	[2M]
	b)	Give the various color coding used in stick diagram with examples.	[2M]
	c)	Define the term area capacitance of layers.	[2M]
	d)	What are the protections used for ESD.	[3M]
	e)	How you can increase the operating frequency of your design.	[3M]
	f)	Show some low power design techniques.	[2M]

PART –B **(56 Marks)**

2.	a)	Analyze the steps involved in a CMOS p-well process.	[7M]
	b)	With neat schematic, explain BiCMOS Fabrication Process.	[7M]
3.	a)	Design schematic, stick diagram and MOS layout of the following function using CMOS logic $f = \big((A+B)(C+D) \big)'$.	[7M]
	b)	Discuss the design rules of contact cuts for NMOS and CMOS.	[7M]
4.	a)	Analyze the sheet resistance concept applied to MOS transistor and inverters.	[7M]
	b)	Evaluate the scaling factors impact on the device parameters-Gate Area (A_g), Gate Capacitance (C_g), Parasitic Capacitance (C_x) and Gate Capacitance Per Unit Area (C_o).	[7M]
5.	a)	Discuss the On-Chip clock Generation and Distribution with examples.	[7M]
	b)	Discuss the Issues for BIST and advantages of BIST.	[7M]
6.	a)	Draw and Explain the Basic FPGA architecture with advantages.	[7M]
	b)	Explain a note on standard cell design and FPGA interconnection resources.	[7M]
7.	a)	Write short notes on need for low power design through voltage scaling.	[7M]
	b)	Discuss the methods of minimizing switching capacitance activity.	[7M]

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