Code: 15A04301 **R15**

B.Tech II Year I Semester (R15) Regular & Supplementary Examinations November/December 2018

ELECTRONIC DEVICES & CIRCUITS

(Common to EEE, ECE and EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) Explain about zener break down.
(b) Define forbidden energy gap.
(c) Compare CE, CC and CB configurations.
(d) Define ripple factor and form factor.
(e) Compare BJT and FET amplifiers.
(f) List the applications of varactor diode.
(g) Compare the rectifier and regulator.
(h) Draw the symbol for N-channel E-MOSFET.
(i) Define ripple factor.
(j) What is the need of biasing?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Compare the characteristics of PN junction diode, Zener diode and Tunnel diode.
(b) For a Ge diode, the $I_0 = 2\mu A$ and the voltage of 0.26 V is applied. Calculate the forward and reverse dynamic resistance values at room temperature.

OR

3 Explain semi-conductors, insulators and metals classification using energy band diagrams.

UNIT – II

4 (a) Derive the expression for ripple factor for full wave rectifier with L-section filter.
(b) Compare FWR and Bridge rectifier.

OR

5 (a) With the help of a neat diagram, explain about the half wave and full wave rectifiers. Also derive the ripple factor and rectification efficiency.
(b) Determine the rating of a transformer to deliver 125 watts of dc power to a load for the following:
(i) Half wave rectifier. (ii) Full wave rectifier. (iii) Bridge rectifier.

UNIT – III

6 (a) Compare CB and CC amplifiers.
(b) Analyze CS-FET amplifier.

OR

7 (a) Explain the operation of CC configuration of BJT and its input and output characteristics briefly.
(b) Explain about Punch through and Base width modulation.

UNIT – IV

8 (a) Obtain stability factor.
(b) Distinguish thermal runaway and thermal stability.

OR

9 (a) What is meant by thermal run-away? Briefly explain.
(b) Draw the circuit diagram of a collector to base bias circuit of CE amplifier and derive an expression for S.

UNIT – V

10 (a) A CB amplifier is driven by a voltage source of internal resistance R_S = 1 kΩ. The load impedance is R_L = 1 kΩ. The transistor parameters are h_{ib} = 22 Ω, h_{fb} = -0.98, $h_{rb} = 2.9 \times 10^{-4}$, h_{ob} = 0.5μA/v. Compute current gain, Voltage gain, input and output Impedance of the amplifier.
(b) Explain the method of evaluating h-parameters for a transistor in CC configuration.

OR

11 Compare FET amplifiers in detail.

*****

Code: 19A04302T **R19**

B.Tech II Year I Semester (R19) Supplementary Examinations August 2021

ELECTRONIC DEVICES & CIRCUITS

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) What is cut in voltage of a diode?
(b) Draw piecewise V-I characteristics of p-n junction diode.
(c) What is zener breakdown?
(d) Explain the working principle of LED.
(e) Compare full wave and bridge rectifier.
(f) What is the need of filters?
(g) Draw the symbol of PNP and NPN transistor.
(h) Explain the need for biasing.
(i) Compare FET and BJT.
(j) Write short notes on CMOS.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Explain the forward and reverse characteristics of PN junction diode using suitable circuit diagram and relevant wave forms.

OR

3 Derive the expressions for drift and diffusion current densities.

UNIT – II

4 Explain the V-I characteristics of zener diode using suitable circuit diagram and wave forms.

OR

5 Explain the construction, working and V-I characteristics of UJT.

UNIT – III

6 Explain the conversion of AC to DC using bridge rectifier using suitable circuit diagram and wave forms.

OR

7 (a) Explain the working of a half wave rectifier with π-filter.
(b) Explain the circuit and wave form of a clipper circuit.

UNIT – IV

8 Explain the common base configuration of PNP transistor and also its input and output characteristics.

OR

9 Derive the stability factor for fixed and self biasing circuit.

UNIT – V

10 Explain the structure and V-I characteristics of n-channel enhancement mode of MOSFET.

OR

11 Explain the DC analysis on p-channel enhancement mode JFET.

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Code: 13A04301 **R13**

B.Tech II Year I Semester (R13) Supplementary Examinations November/December 2018

ELECTRONIC DEVICES & CIRCUITS

(Common to EEE, ECE & EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) State the mass action law.

(b) A silicon PN junction at a temperature of 20°C has a reverse saturation current of 10 picoampere. What is the reverse saturation current approximately at 40°C for the same bias?

(c) Draw the diode connected transistor.

(d) Why BIT is called as a current control device?

(e) Define diffusion capacitance.

(f) What is meant by base width modulation?

(g) What is tunneling phenomenon?

(h) Write the equation for drain current of JFET.

(i) Give the biasing arrangement for an NPN transistor to operate in the active region.

(j) What is working principle of photo diode?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Define the following with respect to a diode: (i) Cut in voltage. (ii) Reverse breakdown voltage. (iii) Transition capacitance. (iv) Intrinsic and extrinsic semiconductors.

(b) Distinguish between zener breakdown and avalanche breakdown.

OR

3 Discuss the effect of temperature upon the characteristics of PN junction diode.

UNIT – II

4 (a) Draw and explain the characteristics of PNP transistor in CE configuration.

(b) Compare CB, CE and CC transistor configurations.

OR

5 Explain the working of p-channel enhancement MOSFET with VI characteristics.

UNIT – III

6 An NPN transistor with beta = 50 is used in a common-emitter circuit with V_{CC} = 10 V and R_C = 2K. The bias is obtained by connecting a 100 K resistance from collector to base. Assume V_{BE} = 0. Find: (i) The quiescent point. (ii) The stability factor S.

OR

7 Derive the stability factor S for fixed bias and self bias.

UNIT – IV

8 (a) Draw the equivalent circuit for the CE and CC configurations subject to the restriction that R_L = 0. Show that the input impedances of the two circuits are identical.

(b) Draw the equivalent circuit for the CE and CC configurations subject to the restriction that the input is open circuited. Show that the output impedances of the two circuits are identical.

OR

9 Find A_V, A_{VS}, A_I, R_I and R_O for common drain FET amplifier.

UNIT – V

10 Draw the VI-characteristics of SCR and explain its operation. Explain the terms holding current and latching current.

OR

11 What is the basic property of a photoconductive cell? With the help of sketches, explain its construction, symbol and operation.

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Code: 15A04301 **R15**

B.Tech II Year I Semester (R15) Regular & Supplementary Examinations November/December 2017

ELECTRONIC DEVICES & CIRCUITS

(Common to EEE, ECE and EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) Define static and dynamic resistance of diode.
(b) List the applications of zener diode.
(c) What is rectifier?
(d) List out different filters used in association with rectifiers.
(e) Define alpha and beta DC amplification factors of BJT.
(f) Compare BJT and FET.
(g) What is the need of biasing?
(h) What is thermal runaway?
(i) Draw BJT transistor small signal low frequency hybrid model.
(j) Draw JFET transistor small signal low frequency hybrid model.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) With neat diagrams, explain the operation of p-n junction diode considering different biasing conditions.
(b) Illustrate V-I characteristics of p-n junction diode.

OR

3 Discuss the operation and characteristics of the following:
(a) SCR.
(b) UJT.

UNIT – II

4 (a) With the help of a neat circuit diagram, input and output waveforms, describe the operation of Half-wave rectifier.
(b) Derive the expressions for ripple factor and maximum efficiency of HWR.

OR

5 (a) Design a Full-wave center-tap rectifier with capacitor filter and then explain its operation.
(b) Derive the expression for ripple factor of a Full-wave center-tap rectifier with capacitor filter and then comment on the result.

UNIT – III

6 Illustrate the input and output characteristics of all three configurations of a BJT transistor. Also give the important equations related to those configurations.

OR

7 (a) Explain the construction and operation of n-channel JFET.
(b) Draw and explain the drain and transfer characteristics of n-channel JFET.

UNIT – IV

8 (a) Design a common emitter BJT circuit with self bias and then explain its operation.
(b) Derive the expression for stability factor S of self bias circuit.

OR

9 List out different FET biasing methods and then explain the same.

UNIT – V

10 By performing generalized analysis of transistor amplifier, derive the expression for different gains and impedances.

OR

11 (a) Design and analyze common source JFET amplifier for its gains and impedances.
(b) Compare CE, CB and CC amplifiers.

*****

Code: 13A04301 **R13**

B.Tech II Year I Semester (R13) Supplementary Examinations November/December 2017

ELECTRONIC DEVICES & CIRCUITS

(Common to EEE, ECE & EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) Define Mass action law.
(b) What is the need of filters in power supplies?
(c) State the differences between enhancement and depletion mode MOSFET.
(d) For a common emitter configuration if α is 0.975, then determine the value of β.
(e) Why thermal runaway occur in transistor?
(f) What is the need for biasing?
(g) State Miller's theorem.
(h) Draw the h parameter equivalent circuit of CE configuration.
(i) Mention the principle of operation of LED.
(j) Draw the symbol diagram and VI characteristics of Diac and Triac.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 For the P-type semiconductor silicon at 300 K if its conductivity is $1(\Omega\ cm)^{-1}$ given that mobility of holes in silicon is 500 cm^2/Vs. Find the concentration of electrons. Also determine the ratio of holes to the free electrons. It is given that the intrinsic concentration of silicon is 1.5×10^{10}.

OR

3 Discuss in detail about the working of bridge rectifier and derive all the parameters.

UNIT – II

4 Illustrate the working characteristics of CB configuration with neat circuit diagram.

OR

5 Draw and explain the construction and principle of operation of JFET and derive the relationship between pinch-off voltage and drain current.

UNIT – III

6 How to stabilize the Q-point using bias compensation techniques? Explain.

OR

7 State the reasons for biasing for zero current drift and derive the condition for zero drift. Also if the n-channel FET is biased at I_D = 0.8mA, calculate the value of $g_{m.}$ Given I_{DSS} = 1.65 mA , V_P = -2.0 V and g_{m0} = 1.60 mA/V.

UNIT – IV

8 A common collector circuit has the following components $R_1 = R_2 = 27\ k\Omega$, $R_E = 5.6\ k\Omega$, $R_L = 47\ k\Omega$, $R_S = 600\ \Omega$. The transistor parameters are $h_{ie} = 1\ k\Omega$, $h_{fe} = 85$ and $h_{oe} = 2\ \mu A/V$. Calculate A_i, R_i, A_v, R_0 using simplified hybrid model circuit.

OR

9 Draw the low frequency equivalent circuit of common source configuration of JFET with fixed bias and derive its performance parameters.

UNIT – V

10 Elaborate on the tunneling mechanism of Tunnel diode along with its VI characteristics.

OR

11 With the help of relevant schematic diagram, briefly describe the operational principle of UJT with its VI characteristics.

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Code: 15A04301 **R15**

B.Tech II Year I Semester (R15) Regular Examinations November/December 2016

ELECTRONIC DEVICES & CIRCUITS

(Common to EEE, ECE and EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) Briefly write about diode resistance.
(b) Write major differences between zener breakdown and avalanche breakdown.
(c) Define TUF & PIV.
(d) Define & Classify filters.
(e) Briefly explain reach through effect.
(f) Draw the symbols for NPN (BJT), PNP (BJT), N-channel JFET and P-channel JFET.
(g) What is the importance of biasing?
(h) Write short notes on thermal runaway.
(i) Sketch the transistor hybrid model.
(j) Draw small signal model for FET.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Derive diode current equation.
(b) A silicon diode has a saturation current of 7.5 μA at room temperature 300 K. Calculate the saturation current at 400 K.

OR

3 Explain construction and operation of UJT & SCR with necessary diagrams.

UNIT – II

4 Explain construction and operation of a bridge rectifier and derive its expressions.

OR

5 (a) Discuss full wave rectifier with L-section filter.
(b) Design a filter for full wave rectifier circuit with LC filter to provide an output voltage of 10 V with a load of 200 mA and the ripple is limited to 2%.

UNIT – III

6 Draw and explain characteristics of Common Collector configurations.

OR

7 Explain construction and operation of N-channel Enhancement & Depletion mode MOSFET.

UNIT – IV

8 Why self bias technique is so popular? And derive its three stability factors.

OR

9 What is the difference between bias stabilization & bias compensation? And also explain any two methods of bias compensation.

UNIT – V

10 Discuss generalized analysis of transistor amplifier model using h-parameters.

OR

11 Discuss generalized analysis of FET amplifier model using small signal model.

*****

Code: 13A04301 **R13**

B.Tech II Year I Semester (R13) Supplementary Examinations November/December 2016

ELECTRONIC DEVICES & CIRCUITS

(Common to EEE, ECE & EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) Compare Avalanche with Zener effect.
(b) Draw the outputs of half wave and full wave rectifiers.
(c) Among CB, CC and CE configurations, which one is more popular and why?
(d) Mention the advantages of FET compared with BJT.
(e) List two important parameters which affect the stability of the Q-point.
(f) Discuss the importance of selecting an operating point in a transistor.
(g) Draw the equivalent circuit or h-model for a two port device.
(h) Write about two types of MOSFETs.
(i) Give the expression of intrinsic stand-off ratio of UJT? Specify typical range of it.
(j) List various applications of an SCR.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 With a neat diagram, explain the working of a PN junction diode in forward bias and reverse bias. Also show the effect of temperature on its V-I characteristics

OR

3 With a circuit diagram, explain the working of full wave bridge rectifier and derive the expression for average output current and rectification efficiency

UNIT – II

4 (a) Explain how the transconductance of a JFET varies with drain current and gate voltage characteristics
(b) A JFET has the following parameters IDSS = 10 mA, Pinch off voltage = -4 V, VGS = -1.0 Volts. Find the values of drain current.

OR

5 (a) Compare BJT with FET.
(b) Explain the use of MOSFET as a switch.

UNIT – III

6 What is a load line and how is it used in the calculation of current and voltage gains for a single stage amplifier?

OR

7 (a) Write the conditions for thermal stability in CE configuration.
(b) Write the importance of biasing and draw a CE amplifier using a fixed-bias circuit.

UNIT – IV

8 Draw the hybrid model of transistor in CE and CB configurations. Explain how h-parameters can be determined from the transistor characteristics.

OR

9 Draw the high frequency equivalent model of FET with a neat sketch, explain the construction and characteristics of depletion MOSFET.

UNIT – V

10 Draw the symbol of a Silicon Controlled rectifier and explain its V-I characteristics

OR

11 Write a short note on:

(a) Light Emitting Diode.
(b) Photo Diode.
(c) Liquid Crystal Display.

*****

Code: 9A04301

R09

B.Tech II Year I Semester (R09) Supplementary Examinations November/December 2016

ELECTRONIC DEVICES & CIRCUITS

(Common to EIE, E.Con.E, ECE, ECC, CSS, IT, CSE, EEE & MCT)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Explain the temperature dependence on VI characteristics of PN junction diode.

(b) A PN-junction diode has a reverse saturation current of 30 μA at a temperature of 125^0C. At the same temperature find the dynamic resistance for 0.2 V bias in forward and reverse direction.

2 (a) Discuss how full wave rectification differs from half wave rectification.

(b) Compare the performance features of center tapped full wave rectifier and a bridge rectifier circuit using the same type of transformers.

3 (a) Why does the CE configuration provide large current amplification while CB does not?

(b) Define ICBO and ICEO. How are they different? How are they related? Are they typically close in magnitude?

4 (a) Design a voltage divider bias network using a supply of 24 V, β = 110 and I_{CQ} = 4μA, V_{ceQ} = 8 V choose $V_e = V_{cc}/8$.

(b) What is thermal runaway?

5 (a) Explain the common drain configuration of JFET with its low frequency AC equivalent circuit.

(b) If two JFET's are connected in parallel with r_{d1} = 20 kΩ, r_{d2} = 30 kΩ, g_{m1} = 2mV and g_{m2} = 4mV. Find effective g_m and r_d.

6 (a) Compare CS, CD and CG JFET amplifiers in all respects.

(b) Draw the voltage divider biasing circuit for FET and explain.

7 State and prove Millers theorem and explain how it is useful in analyzing the amplifier circuits.

8 (a) Explain the construction and principle of operation of varactor diode.

(b) What are the advantages and disadvantages of Tunnel diode?

*****

Code: 9A04301

R09

B.Tech II Year I Semester (R09) Supplementary Examinations June 2016

ELECTRONIC DEVICES & CIRCUITS

(Common to EIE, E.Con.E, ECE, ECC, CSS, IT CSE, EEE & MCT)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Explain how does the reverse saturation current of diode varies with temperature.

(b) Draw the energy band diagram of p-n diode for no bias, forward bias and reverse bias and explain.

2 (a) Discuss the importance of PIV in rectifier circuits.

(b) Derive the ripple factor expression for FWR with inductor filter.

3 (a) With neat diagram explain the various current components in a pnp transistor.

(b) Discuss in brief about the different configurations of BJT.

4 (a) Explain the simpler way of drawing dc load line.

(b) Prove that stability factor S″ = $\frac{(I_{C1} - I_{C01})S_2}{\beta_1(\beta_2 + 1)}$

Where S_2 is the value of stabilizing factor S when β = β2.

5 (a) Briefly explain the operation of n-channel enhancement MOSFET and draw its characteristics.

(b) For n-channel JFET, V_{DS} = 10 V and V_{GS} is changed from 2V to 3V and drain current changed from -4 mA to 2.0 nA. Find r_d and μ if V_{DS} changes from 8 to 12V and I_D changes from 3.0 to 3.2 mA at V_{GS}=2.5V

6 (a) Explain the small signal equivalent circuit of common gate amplifier.

(b) In CG amplifier, R_D= 4 kΩ, R_S= 1 kΩ, r_d= 35 kΩ and g_m= 1.43 x 10^{-3} mho. Find the voltage gain, impedance and output impedance.

7 (a) Draw the small signal hybrid model of CB amplifier and derive the expressions for its A_i, A_v, R_i and R_o.

(b) What are the hybrid or h parameters? Why are they so called?

8 (a) Define gate power dissipations and explain its importance in SCR.

(b) Draw and explain the equivalent circuit of UJT.

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Code: 13A04301 **R13**

B.Tech II Year I Semester (R13) Supplementary Examinations June 2016

ELECTRONIC DEVICES & CIRCUITS

(Common to EEE, ECE & EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) Define intrinsic semi conductor, write example.

(b) What are the basic applications of conventional and Zener diode?

(c) Write the formula for β in terms of α, and in terms of γ of a NPN transistor.

(d) For a transistor α is 0.99, what is β?

(e) List out the types of biasing techniques.

(f) Define thermal runaway.

(g) Draw the h-parameter model of CE mode.

(h) Write the typical values of h_{ie}, h_{fe}, h_{re} & h_{oe}.

(i) Define thyristor family.

(j) Draw the symbols of UJT and Tunnel diode.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) The leakage current through Germanium diode is Io = 25 μA, if the forward bias of V_f = 0.2 V, Calculate the static resistance.

(b) What are the various breakdown mechanisms? Explain one in detail.

OR

3 The Half wave rectifier circuit is supplied with a 230 V AC through 3:1 step down transformer with a resistive load of 10 KΩ, the diode forward resistance is 75 Ω and transformer secondary winding resistance 10 Ω. Calculate $V_{m,}$ I_m, I_{av}, V_{av} and P_{DC}.

UNIT – II

4 (a) Write the current components of PNP transistor and explain.

(b) For a transistor the leakage current is 0.1 μA in CB configuration, while it is 19 μA when it is connected in CE configuration. Calculate α and β of the same transistor.

OR

5 Draw and explain construction and operation of Enhancement mode MOSFET with its characteristics.

UNIT – III

6 Draw the BJT self bias circuit and derive equations for I_B, I_C and V_{CE}.

OR

7 (a) In a fixed bias circuit a Si transistor with β = 100 is used, V_{CC} = 6 V, R_C = 3 KΩ, R_B = 530 KΩ. Draw the DC load line, determine the Q point, What is the stability factor?

(b) What are the advantages of self bias over other biasing techniques?

UNIT – IV

8 For a CE amplifier circuit R_S = 1 KΩ, R_1 = 50 KΩ, R_2 = 2 KΩ, R_C = 1 KΩ, R_L = 1.2 KΩ. Construct small signal equivalent model and Calculate A_I, A_V, R_I and R_I'.

OR

9 (a) State and explain Millers theorem.

(b) A Common Emitter amplifier with collector to Base bias having R_S = 10 KΩ, R_f = 200 KΩ and R_C = 10 KΩ. Calculate A_I, $R_{I,}$ A_V. and R_I'.

UNIT – V

10 With neat diagrams, explain the construction and operation of SCR with its characteristics

OR

11 Draw and explain the construction and operation of UJT

*****

Code: 13A04301 **R13**

B.Tech II Year I Semester (R13) Regular & Supplementary Examinations December 2015

ELECTRONIC DEVICES & CIRCUITS

(Common to EEE, ECE and EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) Differentiate between intrinsic and extrinsic semiconductors.

(b) A HWR is used to supply 24 V dc to a resistive load of 500 Ω and the diode has a forward resistance of 50 Ω. Calculate the maximum value of the ac voltage required at the input.

(c) Specify the relation between α and β factors with respect to a transistor.

(d) Write any two differences between N-channel JFET to a P-channel JFET.

(e) What is the need for biasing a transistor?

(f) Define: (i) Thermal resistance. (ii) Thermal runaway.

(g) Compare CB, CE and CC configurations of a transistor.

(h) Sketch a simplified CE Hybrid model of a transistor.

(i) Why Schottky diode is also called as hot carrier diodes?

(j) Define Latching current and holding currents of a SCR.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT - I

2 What is Fermi Level? By indicating the position of Fermi level in intrinsic, N-type and P-type semiconductor, explain its significance in semiconductors.

OR

3 (a) Compare the performance of Inductive, L-section and π-section filters used with rectifiers.

(b) In a FWR using an LC filter, L = 10 H, C = 100 µF, and R_L = 500 Ω. Calculate I_{dc}, V_{dc}, and ripple factor for an input of V_i = 30 Sin (100 πt) V.

UNIT - II

4 With reference to a BJT, explain the following terms in detail.
(i) Emitter efficiency. (ii) Base transportation factor. (iii) Large signal current gain.

OR

5 Detail the construction of an n-channel MOSFET of depletion type. Draw and explain its characteristics.

UNIT - III

6 (a) Explain how biasing is provided to a transistor through potential divider bias.

(b) An NPN transistor with $\beta = 50$ is used in Common Emitter configuration with V_{CC} = 10 V and R_C = 2.2 kΩ. Biasing is done through a 100 kΩ resistance from collector-to-base. Assuming V_{BE} to be zero volts. Find: (i) The quiescent point. (ii) The stability factor S.

OR

7 Describe the significance of operating point, DC and AC load lines to ensure active region operation of a BJT in CE configuration

UNIT - IV

8 (a) List out the typical values of h-parameters in the three BJT configurations (CE, CB and CC).

(b) Describe how h_{ie} and h_{fe} can be determined from BJT characteristics.

OR

9 Draw the basic circuit and small-signal model of Common drain FET amplifier. Derive the expressions for voltage gain and output resistance.

UNIT - V

10 Draw the basic structure and equivalent circuit of UJT, explain how the UJT can be used as negative-resistance device with the aid of static characteristics.

OR

11 Describe the following briefly:

(a) Principle of operation of a Photodiode

(b) Energy band structure and V-I characteristics of a Tunnel diode.

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Code: 13A04301

R13

B.Tech II Year I Semester (R13) Regular Examinations December 2014

ELECTRONIC DEVICES & CIRCUITS

(Common to EEE, ECE and EIE)

Time: 3 hours Max. Marks: 70

PART - A

(Compulsory Question)

*****

1 Answer the following: (10 X 02 = 20 Marks)

(a) Define forbidden energy gap.
(b) Define peak inverse voltage of diode.
(c) When does a transistor act as a switch?
(d) Define transconductance.
(e) What is operating point?
(f) Which is the most commonly used transistor configuration. Why?
(g) Write the voltage and current equation for hybrid parameters.
(h) What is the significance of h-parameters?
(i) What are the limitations of LCD?
(j) Define radiant intensity for LED.

PART - B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT - I

2 (a) Derive the diode current equation?
(b) Describe the physical mechanism for avalanche breakdown.

OR

3 Derive the ripple factor and efficiency for full wave rectifier with input capacitance.

UNIT - II

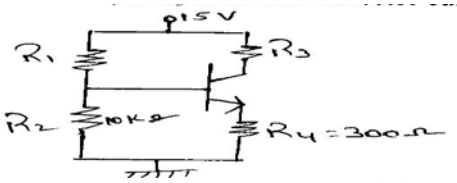
4 With the help of a neat diagram show different current components in a transistor.

OR

5 Draw and explain the drain characteristics of N-channel Enhancement type MOSFET.

UNIT - III

6 In the circuit show in figure transistor has β = 100 and $V_{BE\ (active)}$ = 0.6 V. Calculate the values of R_1 & R_3 Such that collector current of 1 mA and V_{CE} = 2.5 V.



OR

7 For the improvement of stability of the operating point what suggestions you would like to give for self-bias. Discuss with the help of stability factors.

UNIT - IV

8 (a) State Miller's theorem with the aid of a circuit diagram.
(b) Explain the dual of Miller's theorem.

OR

9 Given I_E = 2.5 mA, h_{fe} = 140, h_{oe} = 20 μs and h_{ob} = 0.5 μs determine:

(a) The common- emitter hybrid equivalent circuit.
(b) The common base r_e model.

UNIT - V

10 Sketch and explain the volt-ampere characteristics of a tunnel diode. Indicate the negative resistance portion.

OR

11 (a) Explain the construction and working of photo diode.
(b) Explain Schottky diode with necessary sketches.

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Code: 9A04301

1

B.Tech II Year I Semester (R09) Regular & Supplementary Examinations December/January 2013/14

ELECTRONIC DEVICES AND CIRCUITS

(Common to EIE, E.Con.E, ECE, ECC, CSS, IT, CSE, EEE and MCT)

Time: 3 hours Max Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Explain the V-I characteristics of a P-N Junction diode.

(b) Calculate the dynamic forward and reverse resistance of a p-n junction diode when the applied voltage is 0.24 V. Assume Germanium diode. I_0 =2 µA and T = 300 K.

2 Explain the operation of half wave and full wave rectifiers with and without capacitor filter.

3 (a) Write about the phenomena of reach through in a transistor.

(b) Draw the circuit and explain the output characteristics of CB transistor configuration.

4 If the various parameters of a CE amplifier which uses the self bias method are V_{CC}= 12 V, R_1 = 10 K, R_2 = 5 K, R_C = 1 K, R_e = 2 K and β = 100, find:

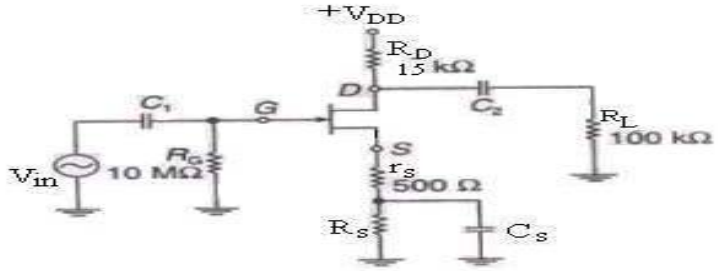
(a) The coordinates of the operating point, and

(b) The stability factor, assuming the transistor to be of silicon.

5 (a) Explain the salient features of voltage controlled device.

(b) Give the classification of FET and write down its merits and demerits when it is compared with BJT.

6 (a) The figure shown below is a swamped FET amplifier. Determine the voltage gain when R_L = 100 K. Neglect the FET output resistance (r_d). Take g_m = 4 mS.



(b) How should the gate-source junction of a JFET be biased? Explain how the potential applied to this junction controls the drain current.

7 (a) Draw CC transistor hybrid model and derive h-parameters of CC transistor using hybrid model.

(b) If a load resistance R_L = 1.2 KΩ is connected to a CE amplifier circuit, determine current gain, input impedance. Assume R_S = R_L and take typical values of h parameters.

8 (a) Explain the differences between tunnel diode and normal PN junction diode.

(b) Write short notes on thermistor.

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Code: 9A04301

2

B.Tech II Year I Semester (R09) Regular & Supplementary Examinations December/January 2013/14

ELECTRONIC DEVICES AND CIRCUITS

(Common to EIE, E.Con.E, ECE, ECC, CSS, IT, CSE, EEE and MCT)

Time: 3 hours Max Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Derive the expressions for diffusion capacitance of PN junction diode.

(b) An ideal Ge p-n junction diode has a reverse saturation current of 30 μA at a temperature of 125^0C. Find the dynamic resistance for a 0.2 V bias (i) in the forward direction. (ii) in the reverse direction.

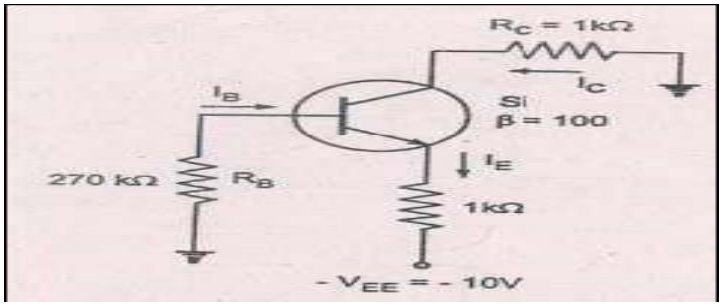
2 (a) With a neat sketch, explain the operation of a single phase full-wave bridge rectifier.

(b) Explain the necessity of filter circuit in rectifiers and give the list of filters used in this section.

3 (a) Sketch the profiles of majority and minority carrier currents in the base of an NPN transistor. Explain the transistor action with the help of these profiles.

(b) The reverse saturation current of the Ge transistor is 2 μA at room temperature of 25^0C and increases by a factor of 2 for each temperature increase of 10^0C. Find the reverse saturation current of the transistor at a temperature of 75^0C.

4 (a) For the circuit shown below, calculate I_B, V_C and V_{CE}.



(b) Differentiate bias stabilization and compensation techniques.

5 (a) Explain the working principle of MOSFET in enhancement and depletion modes.

(b) Define the different parameters of FET.

6 (a) Explain the voltage divider biasing circuit of FET.

(b) Determine the values of R_d and R_S for a self biased p-channel JFET having the following parameters V_P = 5 V, I_{DSS} = 12 mA, V_{DD} = 12 V, I_D = 5 mA, V_{DS} = 6 V.

7 (a) Explain the analysis of CE amplifier using the approximate model.

(b) For CB amplifier is drawn by a voltage source of internal resistance r_s = 1000 Ω. The h-parameters are h_{ie} = 1 KΩ, h_{re} = 2 x 10^{-4}, h_{fe} = 50, h_{oe} = 25 μA/V. Calculate the current gain, voltage gain and output resistance using exact analysis.

8 (a) Explain V-I characteristics of SCR.

(b) Design a UJT relaxation oscillator to generate a sawtooth waveform at frequency of 500 Hz. Assume the supply voltage V_{BB} = 20 V, V_P = 2.9 V, V_V = 1.118 V, I_P = 1.6 mA, I_V = 3.5 mA.

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Code: 9A04301

3

B.Tech II Year I Semester (R09) Regular & Supplementary Examinations December/January 2013/14

ELECTRONIC DEVICES AND CIRCUITS

(Common to EIE, E.Con.E, ECE, ECC, CSS, IT, CSE, EEE and MCT)

Time: 3 hours Max Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Distinguish between zener and avalanche breakdown mechanisms.

(b) Explain about forward bias and reverse bias in the case of a p-n junction diode.

2 (a) What is the cause of surge rectifier circuits using capacitor filter? How is the current limited?

(b) In a full wave rectifier the required dc voltage is 9 V and the diode drop is 0.8 V. Calculate ac rms input voltage required in case of bridge rectifier circuit and centre tapped full wave rectifier circuit.

3 (a) Explain the operation of a NPN bipolar junction transistor in CB configuration.

(b) Compare CB, CE, CC configurations with respect to current gain, voltage gain, input resistance and output resistance.

4 (a) Draw the transistor biasing circuit using fixed bias arrangement and explain its principle with suitable analysis.

(b) Calculate the quiescent current and voltage of collector to base bias arrangement using the following data: V_{cc} = 10 V, R_b = 100 K, R_c = 2 K, β = 50 and also specify a value of R_b so that V_{ce} = 7 V.

5 (a) Compare BJT, JFET and MOSFET in all respects.

(b) For the FET self biased circuit shown (figure 2), calculate the values of R_D and R_S to obtain the bias condition. The maximum drain current is 10 mA and V_{GS} = -2.2 V at I_D = 5 mA.

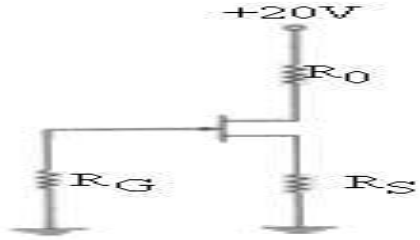
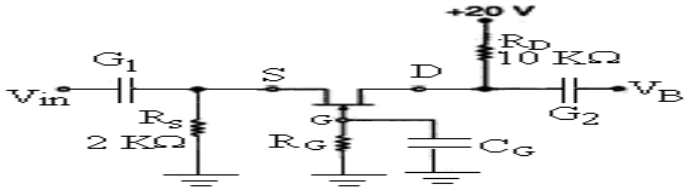


Figure. 2

6 (a) The following figure shows the circuit of a common gate JFET amplifier. The JFET has g_m = 2500 μS. Determine the voltage gain and input resistance.



(b) Sketch the circuit of a CD amplifier. Derive the expression for the voltage gain at low frequencies and what is the order of magnitude of the output impedance.

7 Derive the equations of current gain A_I, voltage gain A_V, input impedance Z_i, output impedance Y_0, voltage gain with R_s (A_{VS}), current gain with R_s (A_{IS}) using a general two port active network.

8 (a) Explain the V-I characteristics of tunnel diode.

(b) Write short notes on opto-isolator and light dependent resistor.

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Code: 9A04301

4

B.Tech II Year I Semester (R09) Regular & Supplementary Examinations December/January 2013/14

ELECTRONIC DEVICES AND CIRCUITS

(Common to EIE, E.Con.E, ECE, ECC, CSS, IT, CSE, EEE and MCT)

Time: 3 hours Max Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Draw the band diagrams of PN junction under open circuit conditions and explain.

(b) The voltage across a silicon diode at room temperature (300 K) is 0.7 volts when 2 mA current flows through it. If the voltage increases to 0.75 V, calculate the diode current.

2 (a) Explain the significance of the term "ripple factor" in rectifier circuits.

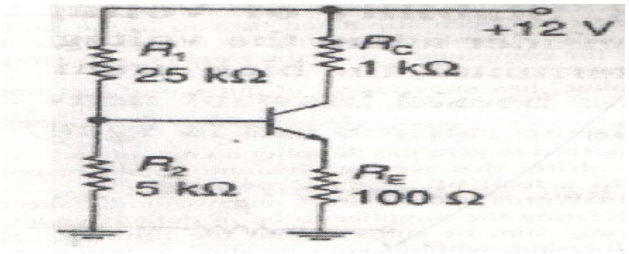
(b) Explain the working of bridge rectifier circuit.

3 (a) Explain the phenomena of reach through in a transistor.

(b) What are the different configurations of BJT? Explain.

4 (a) Explain thermal instability. What are the factors affecting the stability factor?

(b) For the CE amplifier circuit shown below, find the percentage change in collector current if the transistor with $h_{fe} = 50$ is replaced by another transistor with $h_{fe} = 150$. Assume $V_{BE} = 0.6$ V.



5 (a) Draw the drain characteristics of depletion type MOSFET. Explain clearly different operating regions in characteristics with proper reasoning.

(b) Draw the circuit symbol of P channel and N channel JFET.

6 (a) Explain the small signal model of FET.

(b) Calculate the operating point of self biased JFET having supply voltage $V_{DD} = 20$ V, maximum value of drain current $I_{DSS} = 10$ mA and $V_{GS} = -3$ V at $I_D = 4$ mA. Also determine the value of r_d to obtain this condition.

7 (a) Explain the analysis of CE amplifier with emitter resistor using approximate model.

(b) A CE amplifier uses load resistor $R_c = 2$ KΩ in the collector circuit and is given by voltage source V_S of $R_s = 1$ KΩ. The h-parameters are $h_{fe} = 55$, $h_{ie} = 1300$ Ω, $h_{oe} = 22$ μA/V and $h_{re} = 2 \times 10^{-4}$. Neglecting biasing resistors, calculate A_i, A_v, R_i and R_o using $R_E = 200$ Ω.

8 (a) Briefly explain the principle of operation of opto-isolator and light dependent resistor.

(b) List the features and applications of varactor diode.

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Code: 9A04301

1

B.Tech II Year I Semester (R09) Regular and Supplementary Examinations, November 2012

ELECTRONIC DEVICES & CIRCUITS

(Common to EIE, E.Con.E, ECE, ECC, CSS, IT, CSE, EEE and MCT)

Time: 3 hours Max Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Write the diode equation and discuss the effect of temperature on diode current.

(b) Explain about avalanche and zener breakdown.

2 (a) For a full wave rectifier with shunt capacitance filter derive expression for ripple factor using approximate analysis.

(b) Why filter circuit is necessary with rectifiers. Give the list of different filters used in rectifier and their merits and demerits.

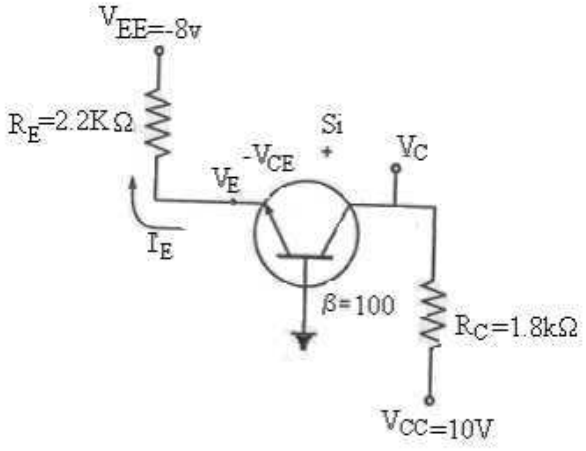
3 (a) Draw a diagram showing various currents in a PNP transistor in common collector mode.

(b) Explain the operation of a PNP bipolar junction transistor in CC configuration.

(c) Draw the common collector transistor characteristics.

4 (a) Explain in detail about thermal runaway and thermal resistance.

(b) For the circuit shown below, determine I_E, V_C and V_{CE} . Assume V_{BE} = 0.7 V



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5 (a) Explain the principle of MOSFET in depletion mode with neat sketches and o/p characteristics.

(b) Explain the different parameters of FET.

6 (a) JFET amplifier with voltage dividing biasing circuit has the following parameters. V_P = -2 V, I_{DS} = 4 mA, r_d = 910 Ω, R_S = 3 KΩ, R_1= 12 MΩ, R_2 = 8.57 MΩ, V_{DD} = 24 V. Find the value of drain current I_D at operating point.
Verify whether FET will operate in pinch-off region or not.

(b) How FET is used as a voltage variable resistor.

7 (a) A transistor with h_{ie} = 1.1 K, h_{fe} = 50, h_{re} = 2.5 X 10^{-4}, h_{oe} = 25 μA/V is connected in CE configuration as shown in figure 1. Calculate A_I, A_V, R_I, R_0.

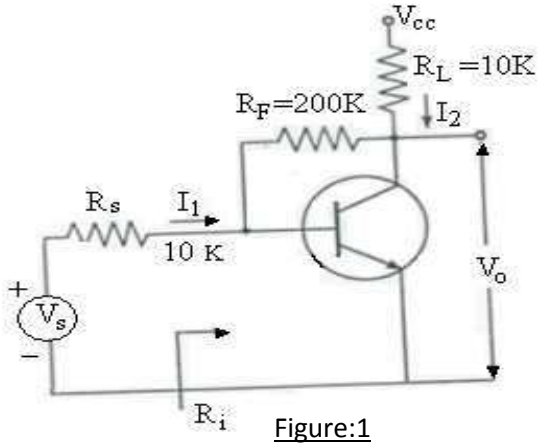

Figure:1

(b) Analyze a single stage transistor amplifier using h - parameters.

8 (a) Explain the working principle of an LED with its characteristics.

(b) What is a tunnel diode? Draw the V-I characteristics of such a diode and explain the occurrence of the negative differential resistance.

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Code: 9A04301

2

B.Tech II Year I Semester (R09) Regular and Supplementary Examinations, November 2012

ELECTRONIC DEVICES & CIRCUITS

(Common to EIE, E.Con.E, ECE, ECC, CSS, IT, CSE, EEE and MCT)

Time: 3 hours Max Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Draw the energy band diagram of p-n diode for no bias, forward bias and reverse bias.

(b) What are general specifications of p-n junction diode?

2 (a) Draw the circuit diagram of full-wave rectifier with inductor filter.

(b) A full-wave rectified voltage of 18 V peak is applied across a 500 µF filter capacitor. Calculate the ripple and d.c. voltages if the load takes a current of 100 mA.

3 (a) Define α_{dc} and β_{dc} of a transistor.

(b) Explain the input and output characteristics of a transistor in CB configuration.

4 (a) Prove that stability factor $S^{11}= \dfrac{(I_C - I_{C01})S}{\beta(\beta+1))}$

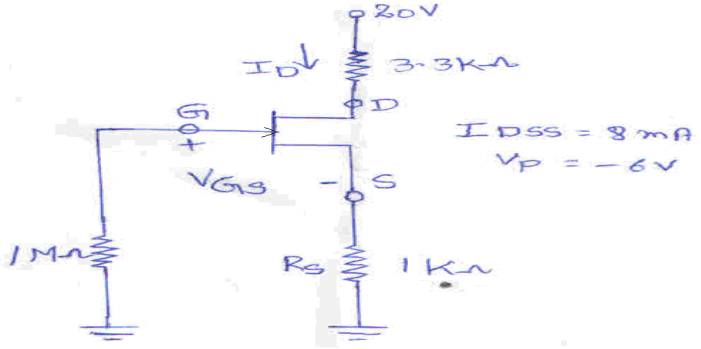
(b) Why biasing is necessary for a transistor circuit in a given configuration? Mention the three different types of biasing a Bipolar Junction Transistor.

5 (a) Why we call FET as a voltage controlled device?

(b) Draw the drain characteristics of depletion type MOSFET. Explain clearly different operating regions in characteristics with proper reasoning.

6 (a) Draw the small signal model of FET amplifier in CS connection and derive the equation for voltage gain, input impedance and output impedance.

(b) Determine the following for the circuit shown below: (i) V_{GSQ} (ii) I_{DQ} (iii) V_{DS} (iv) V_S



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7 (a) A transistor used in CE amplifier connection has the following set of h parameters, h_{ie} = 1KΩ, h_{fe} = 100, h_{re} = 5×10^{-4}, h_{oe} = $2\times10^{-5}\Omega^{-1}$, R_s = 15 KΩ, R_L= 5 KΩ. Determine input impedance, output impedance, current gain and voltage gain.

(b) Draw the hybrid parameter equivalent circuit for an n-p-n common emitter transistor and briefly explain.

8 (a) With a neat circuit diagram explain two transistor analogy of an SCR and explain its working with the help of V-I Characteristics.

(b) Describe the construction of a light-emitting diode and explain its operational mechanism.

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Code: 9A04301

3

B.Tech II Year I Semester (R09) Regular and Supplementary Examinations, November 2012

ELECTRONIC DEVICES & CIRCUITS

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Time: 3 hours Max Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Explain about various current components in a forward biased p-n junction diode.

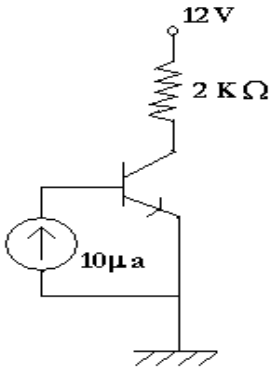
(b) Find the value of D.C. resistance and A.C resistance of a Germanium junction diode at 25^0 C with I_0 = 25 μ*A* and at an applied voltage of 0.2 V across the diode.

2 (a) Discuss a full wave rectifier with π-filter.

(b) Compare the performance of L-section and π-filters.

3 (a) Discuss qualitatively the conditions of flow of currents through a NPN Transistor contributing to the fact that Emitter current is the sum of Collector and Base currents.

(b) A silicon transistor with V_{BE} = 0.7 V, α = 0.98 and collector cut-off current of 10 μA is connected as shown below. Find (i) β *and* I_{CO} (ii) I_C and I_E



4 (a) Draw a BJT fixed bias circuit and derive the expression for the stability factor 'S'.

(b) An NPN transistor with β = 50 is used in a common emitter circuit with V_{CC} = 10 V, R_C = 2 KΩ. The bias is obtained by connecting a 100 KΩ resistance from collector to base. Assume V_{BE} = 0.7 V. Find (i) the quiescent point and (ii) the stability factor, S

Contd. in Page 2

5 (a) What are the differences between BJT and FET?
(b) Draw the small signal model of common source MOSFET amplifier and define all parameters.

6 (a) Draw two biasing circuits for an enhancement type MOSFET and explain.
(b) Calculate the value of R_S required to self bias an n-channel JFET with I_{DSS} = 40 mA, V_P = -10 V, V_{GSQ} = -5 V.

7 (a) The figure 2 shows a CE amplifier with collector to base bias. Calculate A_I , A_V , R_I . The transistor parameters are h_{ie} = 1.1 K, h_{fe} = 50, h_{oe} = 25 x 10^{-6} A/V, h_{re} = 2.5 x 10^{-4}.

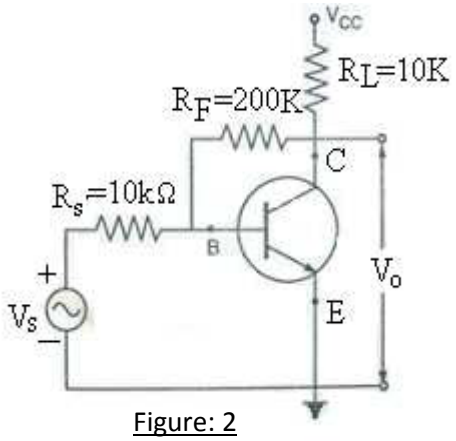


Figure: 2

(b) Draw the circuit diagram of CE amplifier with emitter resistance and obtain its equivalent hybrid model and derive expressions for A_I, R_I, and A_V. Use approximate analysis.

8 (a) Explain the V-I characteristics and the features of Tunnel diode.
(b) If V*E*<V*P* and V*E*>V*P*, explain how UJT works for these conditions.

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Code: 9A04301

4

B.Tech II Year I Semester (R09) Regular and Supplementary Examinations, November 2012

ELECTRONIC DEVICES & CIRCUITS

(Common to EIE, E.Con.E, ECE, ECC, CSS, IT, CSE, EEE and MCT)

Time: 3 hours Max Marks: 70

Answer any FIVE questions

All questions carry equal marks

*****

1 (a) Explain about Forward bias and Reverse bias in the case of a p-n junction diode.

(b) Draw the band diagram of PN junction under open circuit conditions and explain.

2 (a) Calculate the value of capacitance to use in a capacitor filter connected to a full wave rectifier operating at a standard aircraft power frequency of 400 Hz, if the ripple factor is 10% for a load of 500 Ω.

(b) Explain the working of the Half wave rectifier circuit using signal waveforms at various points in the circuit.

3 (a) Explain the input and output characteristics of a transistor in CB configuration.

(b) Calculate the collector current and emitter current for a transistor with α_{dc} = 0.99 and I_{CBO} = 50 μA when the base current is 20 μA.

4 (a) Explain the criteria for fixing operating point.

(b) List out the different types of biasing methods.

5 (a) Discuss FET small signal low frequency model.

(b) Sketch the cross section of an NMOS enhancement transistor and briefly explain.

6 (a) Draw the circuit diagram of common source JFET amplifier and derive the expressions for input resistance and output resistance.

(b) How should the gate-source junction of a JFET be biased? Explain how the potential applied to this junction controls the drain current.

7 (a) Derive the input impedance, output impedance, voltage gain, current gain in CC configuration using approximate model.

(b) A CE amplifier is drawn by a voltage source of internal resistance r_s = 1000 Ω. The h-parameters are h_{ie} = 1 KΩ, h_{re} = 2 x 10^{-4} , h_{fe} = 50, h_{oe} = 25 μA/V. Calculate the current gain, voltage gain and output resistance using exact analysis.

8 (a) Draw the two transistor version of an SCR and explain its firing characteristics with this circuit.

(b) Write a brief note on light dependent resistor.

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