Code: 19A05301 **R19**

B.Tech II Year I Semester (R19) Regular Examinations March 2021

DIGITAL LOGIC DESIGN

(Common to CSE & IT)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Explain $(r-1)'$s complement with example in detail.

(b) Perform subtraction $(1010)_2$ - $(0110)_2$ using 2′ complement method.

(c) Simplify $AB + (AC)' + AB'C\ (AB + C)$.

(d) What are universal logic gates, realize AND, OR gates using universal gates?

(e) Compare a decoder with a demultiplexer.

(f) Define full subtractor.

(g) Classify the register with respect to serial and parallel input-output.

(h) Write about bidirectional shift register.

(i) Differentiate PLA and PAL.

(j) Draw the circuit diagram of TTL.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Convert the octal number 367412 to binary, decimal and hexadecimal.

(b) Find the complement of the following and show that $A.A' = 0$ and $A + A' = 1$.

(i) $A = xy' + x'y$.

(ii) $A = (x + y' + z)(x' + z')(x + y)$.

OR

3 (a) Reduce the following Boolean Expressions to the indicated number of literals:

(i) $A'C' + ABC + AC' + AB'$ to two literals.

(ii) $(X'Y' + Z') + Z + XY + WZ$ to three literals.

(iii) $A'B\ (D' + CD) + B(A + A'CD)$ to one literal.

(b) Convert the following to Decimal and then to octal:

(i) $(125F)_{16}$. (ii) $(10111111)_2$. (iii) $(4234)_{10}$.

UNIT – II

4 (a) Reduce the following expression to the simplest possible POS and SOP forms:

F = Σm(6, 8, 13, 18, 19, 25, 27, 29, 31) + d(2, 3, 11, 15, 17, 24, 28)

(b) Simplify the following expression into sum of products using Karnaugh map:

F(A, B, C, D) = Σ(1, 3, 4, 5, 6, 7, 9, 12, 13)

OR

5 (a) Simplify: (i) $A'B + A'BC' + A'BCD + A'BC'D'E$.

(ii) $(P + Q + R)\ (P' + Q' + R')\ P$.

(b) Explain design procedure for combinational circuit. Differentiate between Combinational circuit & Sequential circuit.

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UNIT – III

6 (a) Construct 4*16 Decoder with help of 2*4 Decoder

(b) Design of full adder by using two half adders.

OR

7 (a) Implement and odd parity generator for 3-bit using a decoder.

(b) Define a multiplexer? Draw a 4:1 multiplexer for the function:

f(a, b, c, d) = Σ(0, 4,5,10,11,12,15)

UNIT – IV

8 (a) Draw the schematic circuit of an edge-triggered JK flip flop with active low preset and active low clear using NAND gates and explain its operation.

(b) Design and draw the logic diagram for MOD-6 ripple counter.

OR

9 (a) Design a 3-bit counter using T flip flops.

(b) Define the following terms with relation to flip flop:

(i) Set-up time. (ii) Hold time. (iii) Propagation delay time. (iv) Preset. (v) Clear.

UNIT – V

10 (a) Explain about MOS and CMOS logic.

(b) Explain about ROM and its different types.

OR

11 (a) Write about the following:

(i) Transistor-transistor logic (TTL).

(ii) Emitter-coupled Logic (ECL).

(iii) CMOS logic.

(b) Compare PLA with PROM.

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