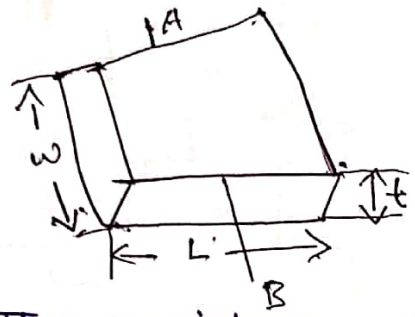
Sheet Resistance (R_s):-

To understand the concept of sheet resistance, Here Let us consider a uniform slab which is having a length of 'L' a width of 'w' and thickness of 't'. as follows.



$\Rightarrow$ The resistance b/w the terminals A & B can be given by R_{AB}.

$$R_{AB} = \frac{\rho l}{A}$$

where ρ – resistivity constant

l – length of the material

A – Crosectional Area.

$$R_{AB} = \frac{\rho l}{w \times t}$$

For a uniform slab, length = width ($L = w$) then

$$R_{AB} = \frac{\rho l}{w \times t}$$

$$R_{AB} = \frac{\rho}{t}$$

$\therefore$ The sheet resistance R_s is a dependent factor on thickness 't' and is independent on crosectional area 'A'.

$$R_S = \frac{\rho}{t} \quad \frac{\Omega}{sq}$$

Some of the typical values of sheet resistance for different technologies are tabulated below.

Layer	Rs ohm Per scauence		
	5μm	2μm (orbit)	1.2μm
Metal	0.03	0.04	0.04
diffussion (active)	10→50	20→45	20→45
silicide	2→4	—	—
Polysilicon	15→100	15→30	15→30
n-transistor -channel	1×10^4	2×10^4	2×10^4
P-transistor channel	2.5×10^4	4.5×10^4	4.5×10^4

Sheet resistance concept applied to MOS transistors & inverters:-

⇒ The sheet resistance concept can be applied to n-type Pass transistors for the figures shown below.

5μm

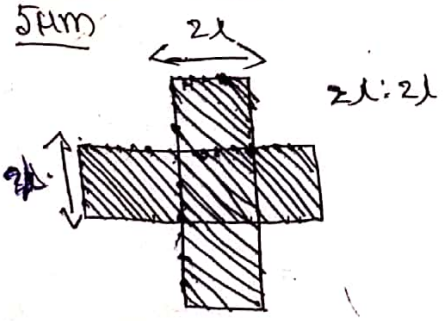


Fig (a)

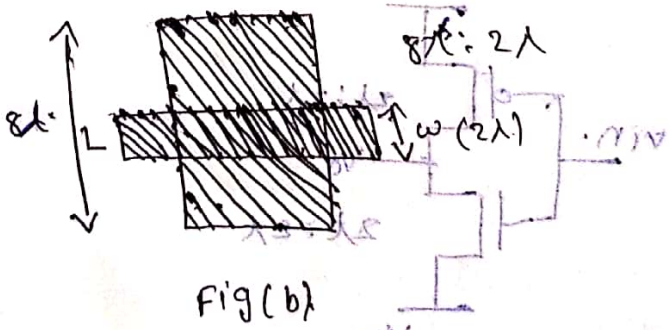


Fig (b)

⇒ In Fig(a) its having a length of 2λ and width of 2λ and fig(b) is carriedout with a length of 8λ & width of 2λ.

⇒ The channel resistance 'R' can be given as

$R = Z R_s$

R_s values can be taken from tabular form i.e 5µm technology.

⇒ For fig(a) the channel Resistance 'R' can be given as w.k.t $Z = \frac{L}{W}$

$\Rightarrow \frac{2\lambda}{2\lambda} = 1$

$R = Z R_s$

$= 1(R_s)$

$R = 1 \times 10^4$

$R = 10k\Omega$

⇒ For Fig(b) the channel resistance 'R' can be given as

$Z = \frac{L}{W}$

$= \frac{8\lambda}{2\lambda} = 4$

$R = Z R_s$

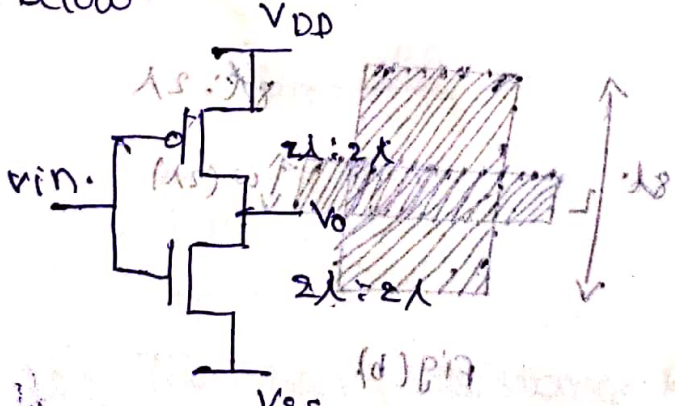
$= 4(R_s)$

$= 4(10^4)$

$R = 40k\Omega$

For Inverters

⇒ Here Letus consider a CMOS inverter as shown below.



⇒ The channel resistance for PMOS device can be given as

$R_{PS} = Z_{pu} R_s$

$Z_{pu} = \frac{L}{W}$

$= \frac{2\lambda}{2\lambda} = 1$

$R_{PS} = 1 \times 2.5 \times 10^4$

$\boxed{R_{PS} = 25\,k\Omega}$

$\Rightarrow$ The channel resistance for n-MOS device can be given as

$R_{ns} = Z_{pd} R_s$

$Z_{pd} = \frac{2\lambda}{2\lambda} = 1$

$R_{ns} = 1 \times 10^4$

$\boxed{R_{ns} = 10k\Omega}$

$\therefore$ The total resistance for nMOS inverter can be given as

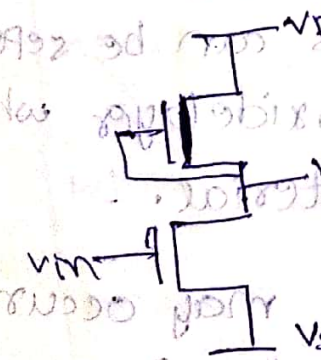
$R_{ON} = R_{PS} + R_{ns}$

$= 25k\Omega + 10k\Omega$

$\boxed{R_{ON} = 35k\Omega}$

For NMOS inverter:-

$\Rightarrow$ Here let us consider an NMOS inverter as shown in fig below.



$\Rightarrow$ The resistance of pullup depletion mode NMOS can be calculated as

$R_{npus} = Z \cdot R_s$

$Z = L/W = 8l/2l$

$Z = 4$

$\therefore R_{npus} = 4 \times 10^4$

$\boxed{R_{npus} = 40k\Omega}$

$\Rightarrow$ The resistance of pulldown enhancement mode nmos can be given as

$R_{npds} = ZR_s$

$Z = \frac{L}{W} = \frac{2l}{2l} = 1$ [R_s values are taken from Spum tech]

$R_{npds} = 1 \times 10^4 = 10k\Omega$

$\boxed{R_{npds} = 10k\Omega}$

$\therefore$ The total resistance for an Nmos inverter can be given as

$R_{ON} = R_{npus} + R_{npds}$

$= 40k\Omega + 10k\Omega$

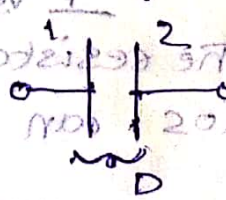
$\boxed{R_{ON} = 50k\Omega}$

Area capacitances of layers:

$\Rightarrow$ Based on the fabrication process, it is apperend that the Mos layers can be seperated from one an other by a oxide layer which is acting as insulating material.

$\therefore$ Parallel plate capacitances may occur.

$\Rightarrow$ Here the oxidelayer acts as dielectric material b/w plate1 and plate2.



⟹ w.k.t the capacitance 'C' can be given as

$$C = \frac{\epsilon A}{D}$$

where $\epsilon = \epsilon_0 \epsilon_{ins}$

ϵ_0 – absolute permitivity (or) permitivity of free space = 8.854×10^{-12} faraday/m.

ϵ_{ins} – relative permitivity = 4 for si.

A – Area of the plates

D – thickness of oxide layer.

⟹ some of the typical values of area capacitance are tabulated below for 5 µm, 2 µm, 1.2 µm technology.

capacitance	value in PF x 10^{-4} µm^2 (relative values in brackets)		
	5µm	2µm	1.2µm
Gate to channel	4 (1.0)	8 (1.0)	16 (1.0)
diffussion (active)	1 (0.25)	1.75 (0.22)	3.75 (0.23)
Polysilicon to substrate	0.4 (0.1)	0.6 (0.075)	0.6 (0.038)
Metal1 to substrate	0.3 (0.075)	0.33 (0.04)	0.33 (0.02)
Metal2 to substrate	0.2 (0.05)	0.17 (0.02)	0.17 (0.01)
Metal2 to Metal1	0.4 (0.1)	0.5 (0.06)	0.5 (0.03)
Metal2 to Polysilicon	0.3 (0.075)	0.3 (0.038)	0.3 (0.018)

Standard unit of capacitance:- ($\square_{cg}$).

⇒ The standard unit of gate capacitance can be defined for gate to channel capacitance and it can be represented with '$\square_{cg}$'.

For 5μm technology:-

⇒ The area/standard square for 5μm technology

$= 5\mu m \times 5\mu m = 25\mu m^2$ [$\because L = W = 5$]

⇒ w.k.t the standard unit of capacitance ($\square_{cg}$) can be given as,

$\square_{cg}$ = (Area/standard square) × capacitance ← from table

⇒ for 5μm capacitance is $= 4 \times 10^{-4} pf/\mu m^2$

$\square_{cg} = 25\mu m^2 \times 4 \times 10^{-4} pf/\mu m^2 = 100 \times 10^{-4} pf$

$= 0.01 pf$

For 2μm technology:-

⇒ The area/standard square for 2μm technology

$= 2\mu m \times 2\mu m = 4\mu m^2$

⇒ w.k.t the standard unit of capacitance can be given as

$\square_{cg}$ = Area/standard square × capacitance

⇒ for 2μm capacitance is $= 8 \times 10^{-4} pf/\mu m^2$

$\square_{cg} = 4\mu m^2 \times 8 \times 10^{-4} pf/\mu m^2 = 32 \times 10^{-4} pf$

$= 0.0032 pf$.

for 1.2μm technology:-

⇒ The area/standard square for 1.2μm technology

$= 1.2\mu m \times 1.2\mu m = 1.44\mu m^2$

⇒ w.k.T the standard unit of capacitance can be given as

$\square_g$ = Area/standard square × capacitance

⇒ for 1.2μm capacitance is = $16 \times 10^{-4} pF/\mu m^2$

$\square_{cg} = 1.44\mu m^2 \times 16 \times 10^{-4} pF/\mu m^2$

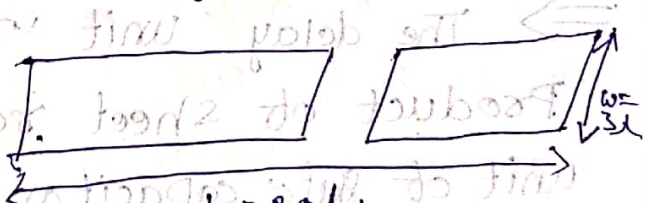
$\square_{cg} = 0.0023 pF$

Some area capacitance calculations:-

⇒ In this calculation of capacitance we use all relative values of capacitance and all values are defined in 'λ' based rules.

⇒ For Ex here let us consider a metal as shown in fig below.

⇒ The relative area for the given metal can be defined as the ratio of Area of interest to the standard Area.



$\therefore$ relative area = $\frac{\text{Area of interest}}{\text{standard area}}$

$= \frac{20\lambda \times 3\lambda}{2\lambda \times 2\lambda} = 15$

(i) For 5μm:-
For the given metal the capacitance to the substrate can be given as

capacitance to the substance = Relative area × capacitance.

$= 15 \times 0.075 \square cg$

$= 1.125 \square cg$

∴ The capacitance to substrate is 1.125 times of $\square cg$

(ii) For diffussion:-

capacitance $= 15 \times 0.25 \square cg$

$= 3.75 \square cg$

(iii) For Polysilicon:-

capacitance $= 15 \times 0.1 \square cg$

$= 1.5 \square cg$

Time delay:- (the delay unit) (τ)

⟹ The delay unit 'τ' can be given as the Product of sheet resistance (R_s) and standard unit of gate capacitance ($\square cg$).

i.e, $\boxed{\tau = R_s \square cg}$

For 5μm technology:-

$\tau = R_s \square cg$

$= 10^4 \times 0.01 fF$

$= 10^4 \times 0.01 \times 10^{-12}$

$= 10^2 \times 10^{-12}$

$= 10^{-10}$

$= 0.1 \times 10^{-9}$

$\tau = 0.1$ ns.

For 2μm:-

$\tau = R_s \square c_g$

$= 2 \times 10^4 \times 0.0032$ PF

$= 2 \times 10^4 \times 0.0032 \times 10^{-12}$

$= 2 \times 0.0032 \times 10^{-8}$

$\tau = 0.064$ ns

For 1.2μm:-

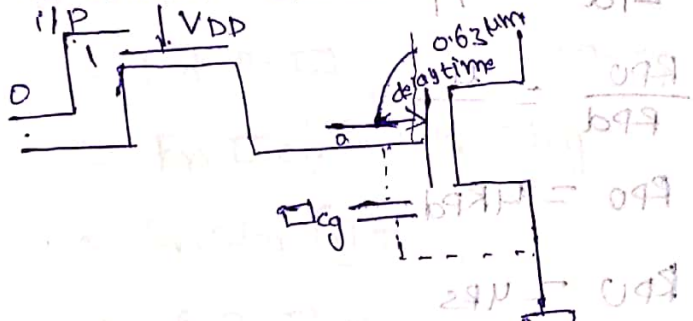
$\tau = R_s \square c_g$

$= 2 \times 10^4 \times 0.0023$ PF

$= 2 \times 0.0023 \times 10^{-8}$

$\tau = 0.046$ ns.

⇒ The simple dig that illustrates the delay -unit is shown below.



⇒ Here the i/p transitions are from 0 to V_{DD} and when it is passed through a delay ckt only 63% of VDD is available at the o/p. i.e $V_{DS} \simeq 3V$.

⇒ W.K.T the electron Transit time can be given as $\tau_{ds} = \frac{L^2}{\mu V_{ds}}$

For 5μm technology:-

$\tau_{ds} = \frac{L^2}{\mu V_{ds}}$

$= \frac{5\mu m \times 5\mu m}{650 cm^2/V\text{-sec} \times 3V}$

$$= \frac{25 \times 10^{12}\ m^2}{650 \times (0.01)\ m^2/V\text{-}sec \times 5V}$$

$$\boxed{\tau_{ds} = 0.15\ nsec}$$

NOTE:- The electron Transic time τ_{ds} is approximately equal to the delay unit τ.

Inverter delays;-

(i) NMOS inverter;-

⇒ Here let us consider an NMOS inverter of 4:1 type

∴ The Pullup to Pulldown ratio of NMOS driven by another NMOS is 4:1.

$$\frac{Z_{PU}}{Z_{Pd}} = \frac{4}{1}$$

$$\frac{R_{PU}}{R_{Pd}} = \frac{4}{1}$$

$$R_{PU} = 4R_{Pd}$$

$$R_{PU} = 4R_S$$

$$R_{PU} = 4 \times 10^4$$

$$\boxed{R_{PU} = 40k\Omega}$$

⇒ The delays associated with NMOS inverter are not dependent on the cascaded connections but depends on how many times it is being turned ON/off.

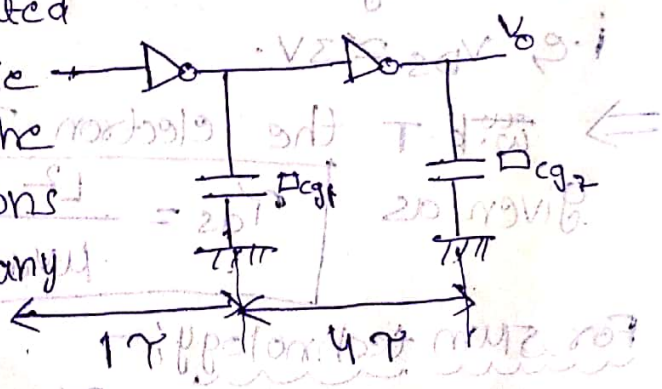


Fig (a)

⟹ For i/p logic 1 shown in fig (b) the NMOS which is pulldown in inv1 will get ON then the capacitor C_{g_1} can have a discharge path i.e, $\tau_1 = R_n C_{g_1}$

⟹ $R_n = 10k\Omega - C_{g_1}$

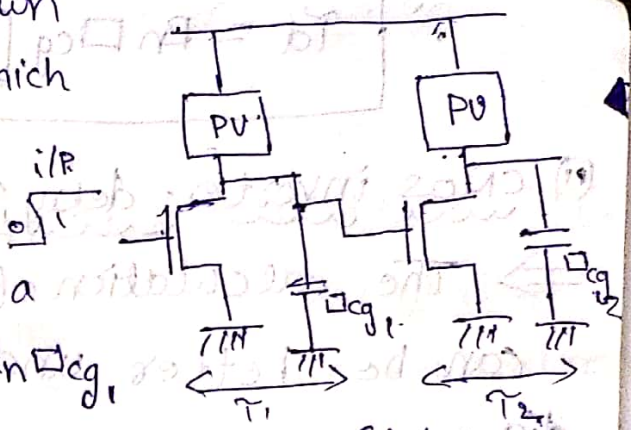


Fig (b).

⟹ when capacitor C_{g_1} discharge then the pulldown inv2 is having an i/p of '0' hence it will get off.

∴ The capacitor C_{g_2} will get charge thrgh pullup of inv2. $\tau_2 = R_{PU2} C_g = 40k\Omega - C_g$

∴ The overal delay τ_d can be given as

$$\tau_d = \tau_1 + \tau_2$$

$$= 10k\Omega \cdot C_g + 40k\Omega - C_g$$

$$= R_n C_g + 4R_n \cdot C_g$$

$$= R_n C_g [1+4]$$

$$= 5 R_n C_g$$

$$\boxed{\tau_d = 5\tau}$$

∴ The overall delay of NMOS inverter is 5τ.

⟹ From the above calculations

$$\tau_d = R_n C_g [1+4]$$

w.k.T the pullup to pulldown ratio of NMOS driven by another NMOS is 4:1

i.e, $\frac{Z_{PU}}{Z_{Pd}} = 4/1$

$$\tau_d = R_n \square c_g \left[1 + \frac{2p_v}{2p_d}\right]$$

(ii) CMOS inverter delay :-

⟹ The calculation of CMOS inverter delay can be better understood with the following dig.

⟹ due to the internal wiring capacitances the load capacitances will get doubled. i.e $2\square c_g$

⟹ For i/p logic the pulldown of Inv1 will get ON and the capacitor will get discharge throughit.

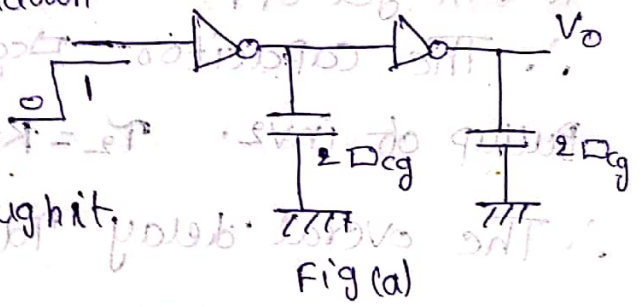


Fig (a)

$\tau_1 = R_n 2\square c_g$

$\boxed{\tau_1 = 20k\Omega \square c_g}$

⟹ when the capacitor $2\square c_{g1}$ is discharge then at the i/p of Inv2 we get 0.

So the pullup of Inv2 will get ON and the capacitor will get charge.

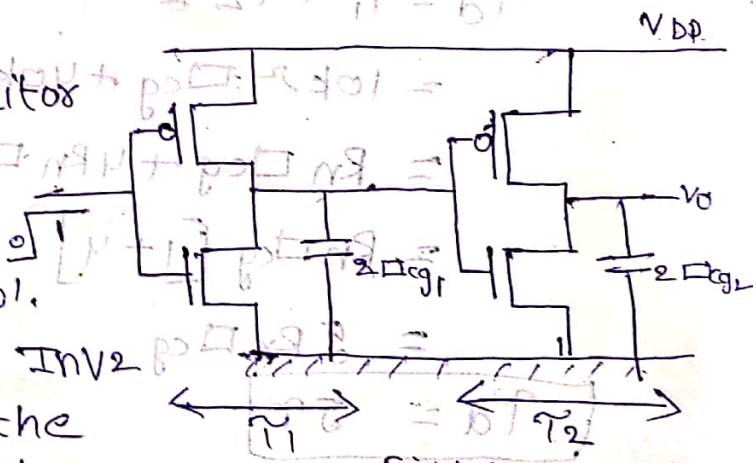


Fig (b).

$\therefore \tau_2 = R_p 2\square c_g$

$= (25k\Omega) 2\square c_g$

$\boxed{\tau_2 = 50k\Omega \square c_g}$

⟹ The overall delay τ_d can be given as

$\tau_d = \tau_1 + \tau_2$

$= 20\square c_g + 50\square c_g$

$= 2R_s \square c_g + 5R_s \square c_g$

$T_d = 7 R_s \square_g$

$\boxed{T_d = 7\tau}$

∴ The overall delay in CMOS Inverter is 7τ.

⟹ The total delay can be better calculated including the risetime & falltime estimations.

Risetime calculation :- (T_r)

⟹ The Risetime can be calculated when we apply i/p as logic '0'. then the i/p pullup of inv2 acts as constant current source as shown in fig.

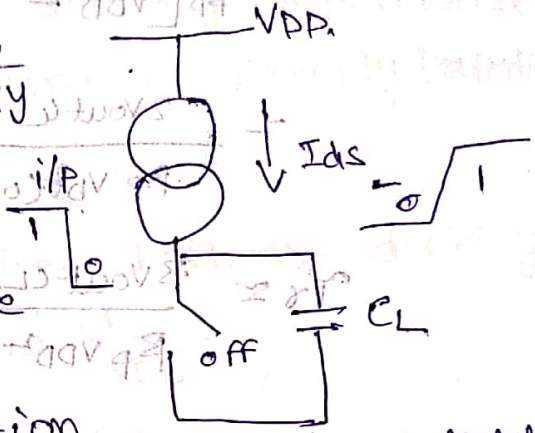


Fig:- Rise time calculation

⟹ The Ids in saturation mode can be given as

$$I_{ds} = \frac{K_W}{L} \frac{[V_{gs} - V_t]^2}{2}$$

$$I_{ds} = \beta_p \frac{[V_{gs} - V_{tp}]^2}{2}$$

$$V_{out} = I_{ds} R \quad \text{---} (1)$$

w.k.t $\tau_r = RC_L$

$$R = \frac{\tau_r}{C_L} \quad \text{---} (2)$$

sub (2) in (1)

$$V_{out} = I_{ds} \frac{\tau_r}{C_L}$$

$$\tau_r = \frac{V_{out} \cdot C_L}{I_{ds}}$$

$$\tau_r = \frac{V_{out} C_L}{I_{ds}}$$

$$\tau_r = \frac{V_{out} C_L}{\frac{\beta_p [V_{gs} - V_{tp}]^2}{2}}$$

$$= \frac{2 V_{out} C_L}{\beta_p [V_{gs} - V_{tp}]^2}$$

$$= \frac{2 V_{out} C_L}{\beta_p [V_{DD} - 0.2 V_{DD}]^2}$$

$$= \frac{2 V_{out} C_L}{\beta_p V_{DD}^2 (0.64)}$$

$V_{tp} = 0.2 V_{DD}$

$V_o = V_{DD}$

$$\tau_r \simeq \frac{3 V_{out} C_L}{\beta_p V_{DD}^2}$$

$$= \frac{3 V_{DD} C_L}{\beta_p V_{DD}^2}$$

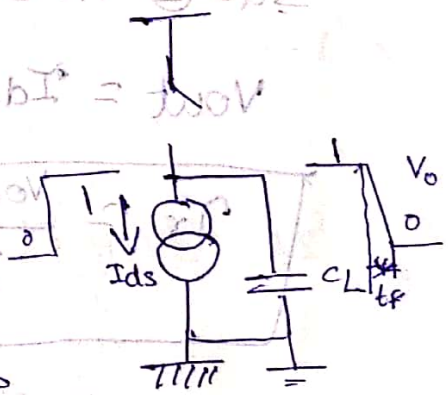
$$\boxed{\tau_r \simeq \frac{3 C_L}{\beta_p V_{DD}}}$$

Falltime calculation:-

The process of falltime calculation is almost similar to risetime calculation.

⇒ The falltime can be calculated when i/p is logic '1' then the NMOS which is pulled down will get turned 'ON'.

$$\boxed{T_f = \frac{3 C_L}{\beta_n V_{DD}}}$$ (reference from risetime calculation)



⇒ The ratio of risetime to fall time is. $\frac{\tau_r}{T_f}$.

$$\frac{T_r}{F_f} = \frac{\frac{3C_L}{\beta_p V_{DD}}}{\frac{3C_L}{\beta_n V_{DD}}}$$

$$\boxed{\frac{T_r}{T_f} = \frac{\beta_n}{\beta_p}}$$

∴ The risetime t_r is directly proportional to $\frac{1}{\beta_p}$. and Fall time is directly proportional to $\frac{1}{\beta_n}$.

⟹ The risetime & falltime both are directly proportion to C_L and $\frac{1}{V_{DD}}$.

driving large capacitive loads:-

⟹ To drive capacitors of comparitively very large, it can be done when the signals are propagated from ON chip peripherals to off chip perpherals.

⟹ Let the offchip load capacitance is C_L then it is several orders greaterthan the gate capacitance C_g i.e, $C_L > 10^4 C_g$ (assumption)

⟹ To have a reduced delay we have to get a low resistance path by increasing the channel length. i.e, area.

⟹ Methods of driving large capacitive loads:-

⟹ Basically we are having 3 classifications.

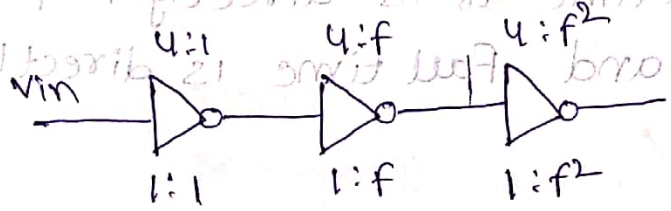
1. cascading connections of Inverters
2. super Buffers as drivers.
3. BiCMOS drivers

1. cascading connections of Inverters:-

⟹ To drive large capacitive loads we should have low resistances

⟹ The low resistances can be obtain whenever we are having low Z_{pu} & Z_{pd}'s

⟹ The arrangment for calculating cascaded connections of inverters is shown below



cascade connections of Inverters.

f- width factor.

⟹ If we increase the width factor 'f' then the load on capacitor may increase their by we can have minimum resistance.

⟹ The total delay for NMOS Inverter:-

$\therefore \tau_d = 5f\tau$ (NMOS inverter)

$= 1f\tau + 4f\tau$

Total delay for CMOS inverter

$\tau_d = 7f\tau$

$= 2f\tau + 5f\tau$

⟹ suppose if we are having 'N' no of inverters in cascaded connection then 'N' can be is a function of can can be given as

$N^f = \frac{C_L}{C_g} = y$

$N^f = y$

log on Both sides

$$f \log N = \log y$$

let $f = e$

$$\log N e^{e} = \log y.$$

$$N = \log y$$

For NMOS inverter:-

$\tau_d = 1f\tau$ For Δvin

$\tau_d = 4f\tau$ For ∇vin

For CMOS inverter:-

$\tau_d = 2f\tau$ For Δvin

$\tau_d = 5f\tau$ for ∇vin'

$\Rightarrow$ If (i) 'N' is even then

$\tau_d = \frac{N}{2}\tau_d \Rightarrow$ 2.5fτ For NMOS.

$\tau_d = \frac{N}{2}\tau_d \Rightarrow$ 3.5fτ For CMOS.

(ii) If 'N' is odd then.

$\tau = [2.5(N-1)+1]f\tau$ Δvin for NMOS

$\tau = [(3.5)(N-1)+2]f\tau$ Δvin for CMOS

$\tau = [2.5(N-1)+4]f\tau$ ∇vin for NMOS

$\tau = [3.5(N-1)+5]f\tau$ ∇vin for CMOS.

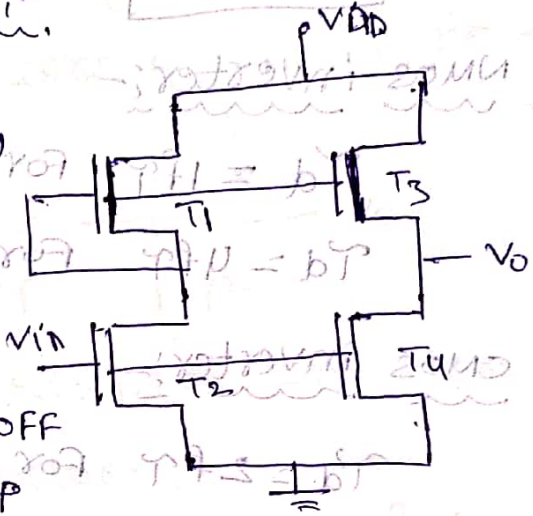
2) Super Buffers as drivers:-

⟹ Basically we are having two classifications

(i) inverting type NMOS super Buffer.

(ii) Non inverting type NMOS super Buffer.

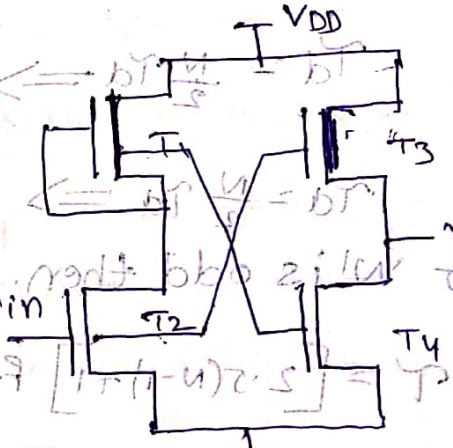
inverting type S.B:-



⟹ If Vin is 'logic'1' then T2 & T4 will get ON their by Producing o/p as logic '0'.

⟹ If Vin is logic'0' then T2 & T4 will get OFF their by Producing o/p as logic '1'.

Non inverting type S.B:-



⟹ If Vin is logic'1' then then T2 & T3 will get ON their by Producing o/p as logic'1'.

⟹ If Vin is logic'0' then T2 & T3 will get off their by Producing o/p as logic '0'.

3) BICMOS drivers:-

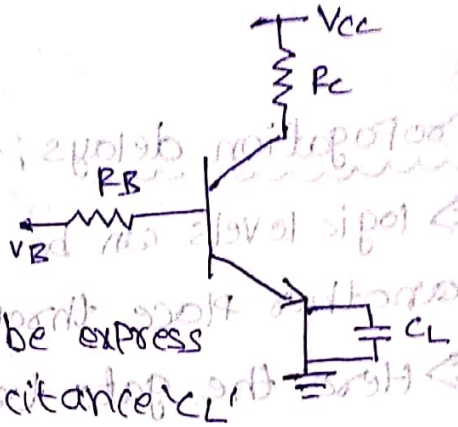
⟹ Bipolar technology having high o/p deriving current capability in a minimize silicon area.

⟹ In Bipolar the transconductance gm and silicon area that represents o/p drive current per area is more compared to MOS technology

⟹ For the application of Minimum Base voltage V_B it draws large o/p current.

⟹ The voltage V_{BE} is a depedent on base width W_B and impurity concentration.

⟹ The switching characteristics can be understood with the flwng dig.



⟹ The amount of time required to change i/p is equal to time to change o/p.

⟹ The change in time can be express as a function of load capacitance (C_L) and standard unit of gate capacitance (C_g).

i.e $\boxed{\Delta t = \frac{C_L}{C_g}}$

⟹ In Bipolar technology gate capacitance C_g is replaced with transconductance g_m.

i.e $\boxed{\Delta t = \frac{C_L}{g_m}}$

⟹ In Bipolar technology transconductance (g_m) is more their by we can have minimum delay.

⟹ The total time can be represented as

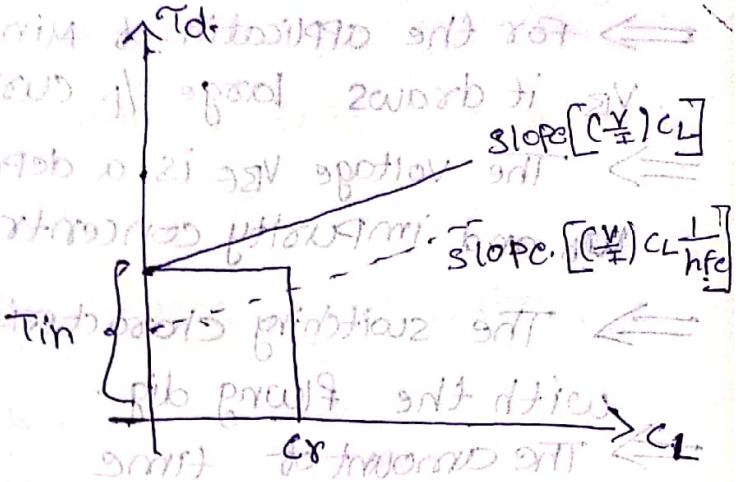
$$T = T_{in} + \left(\frac{V}{I}\right) C_L \frac{1}{h_{fe}}$$

where C_L - Load capacitance

h_{fe} - current amplification factor

T_{in} - inbuilt time.

⟹ The graphical representations of Bipolar and Mos technologies can be shown as

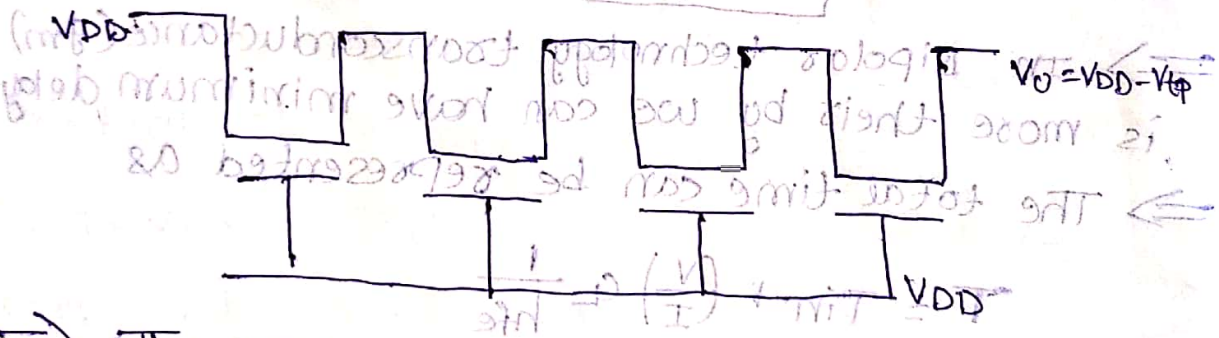


Propagation delays :-

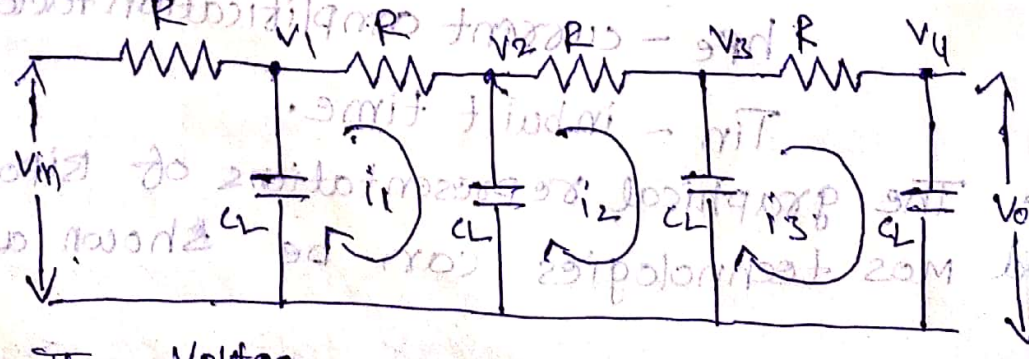
⇒ logic levels can be transfered from one place to another place through series of pass transistors.

⇒ Here the gate terminals of series of passtran-sistor are tied together and V_{DD} is been applied as we are considering NMOS pass transistor

⇒ For ex a series of 4 pass transistors can be represented as follows.



⇒ The equivalent ckt can be drawn as



⇒ The voltage

$\Rightarrow$ The amount of current 'i' at node 2 can be given as

$$C\frac{dV_2}{dt} = i_1 - i_2$$

$$= \frac{V_1 - V_2}{R} - \frac{V_2 - V_3}{R}$$

$$= \frac{V_1 - 2V_2 + V_3}{R}$$

$$RC\frac{dV_2}{dt} = \frac{d^2V_2}{dx^2}\ V_1 - 2V_2 + V_3$$

$$RC\frac{d^2V_2}{dt^2} = \frac{d^2V_2}{dx^2}$$

where, x = distance.

$\Rightarrow$ suppose if we are having 'N' no of stages then $R_{total} = N\gamma R_s$

N = No. of stages, γ = relative resistance.

R_s = sheet resistance

$\Rightarrow$ The total capacitance can be given as

$$C_{total} = NC\square_{cg}$$

N - no. of stages, C - relative capacitance

$\square_{cg}$ - standard unit of gate capacitance.

$\Rightarrow \therefore$ Total delay $t_d = R_{total} C_{total}$

$$= N\gamma R_s\ NC\square_{cg}$$

$$= N^2\gamma C R_s \square_{cg}$$

$$\boxed{t_d = N^2\gamma c\tau}$$

i.e, the total delay $\propto N^2$.

Choice of layers:-

⟹ whenever we are designing the ckt of our convinience of suitable specifications, we have to consider several no. of considerations which includes choice of layers.

1. V_{DD} & V_{SS} should be distributed on metal -layers whenever possible.
2. The length of Polysilicon should be use after carefull consideration bcz of relatively high value of sheet resistance.
3. The Polysilicon is unsuitable for routing Vdd & Vss otherthan smaller distances.
4. capacitive effects may also be considered Bcz diffussion regions relatively may have high capacitive values to the substrate.

Electrical rules:-

layer	Max length of wire		
	5μm	2μm	1.2μm
metal	chipwide	chipwide	chipwide
Silicide	200λ	Not applicable	Not applicable
Poly	200λ	400μm	250μm
diffussion	20λ	100μm	60μm

choice of layers;-

Layer	capacitance	resistance	comment
metal	low	low	good current driving capability without large voltage drop. it is used for power distributions & global
silcide	moderate	moderate	⇒ it has RC product as a moderate value. long wires are possible. This layer is useful in place of polysilicon in some cases of NMOS process.
polysilicon	moderate	high	It has RC product as a moderate value and IR-drop.
diffussion (active)	high	moderate	⇒ RC product is moderate and it has moderate IR drop. hence it is hard to drive.

wiring capacitances;-

⇒ we have area capacitances contributed in the calculation of overall capacitance. we have 3 other sources for calculation of overall capacitance

1. Interlayer capacitance
2. Pheripheral capacitance
3. fringing fields

Interslayer capacitance;-

⇒ Parallel plate effects are present one layer to another layer.

⇒ For ex, giving area metal to polysilicon

capacitance is higher than metal to substrate capacitance

Peripheral capacitance;-

⟹ The source and drain of n+ diffussion region forms junctions with P substrate at uniform depth.

⟹ //ly, P+ative regions may form junctions with N-well or N-type of substrate.

⟹ for diffussions regions each diode does form associated with peripheral capacitance which is measured in PF/unit length.

⟹ The typical values of different technologies are given by.

diffusions capacitance	Chemical values		
	5 μm	2 μm	1.2 μm
C_{area}	1.082×10^{-4} PF/μm²	1.25×10^{-4} PF/μm²	1.75×10^{-4} PF/μm²
$C_{peripheral}$	8×10^{-4} PF/μm²	Negligible	Negligible

Fringing Fields;-

⟹ capacitance due to fringing field effects can be a major component of overall capacitance of interconnected wires.

⟹ fringing field capacitance can be of the same order of area capacitance then capacitance of fringing field can be given as

$$C_{ff} = \epsilon_0 \epsilon_{ins} l \left[\frac{2\pi}{\ln\left[1+\frac{2d}{t}\left(1+\sqrt{\frac{t}{2d}}\right)\right]} + \frac{t}{4d} \right]$$

l - length of channel

t - thickness of wire

d - distance b/w wire & substrate

∴ The total wire capacitance can be given as

$$C_w = C_{area} + C_{ff}$$

C_{area} - area capacitance

C_{ff} - Fringing field capacitance

Part-2

Scaling of Mos ckts

⇒ Micro electronic technology may be characterized in interms of several indicators or figure of Merits

⇒ The commonly used are

1) Minimum feature size.
2) No. of gates on chip
3) Power disippation.
4) Maximum operational freaquency
5) die size.
6) Production cost

⇒ Many of these figure of Merits can be improved by reducing the dimensions of Transistors, interconnections and seperation b/w features and by adjusting doping level supply voltage.

Scaling Models & scaling factors :-

⇒ Basically there are 2 types of scaling models

1) constant electricfield scaling Model.
2) constant voltage Scaling Model.

⇒ In accordance of these two scaling models we are having a special type of scalingmodel called "combined vetage and dimension S.M".

⇒ The following fig indicates that the substrate doping levels which are associated with Scaling of Transistors.

⇒ In order to accomodate these 3 scaling models we use 2 scaling factors as $1/\alpha$ & $1/\beta$.

⇒ $1/\beta$ is choosen as a scaling factor for supply voltage Vdd & gate oxide thickness 'D'. and $1/\alpha$ is used for all other linear dimensions.

NOTE:-

⟶ For constant electric field Mode $\beta = \alpha$ and

For constant voltage Mode, $\beta = 1$

Scaling factors for device Parameters

1) Gate area (A_G) :-

A_G = length x width = $L \times W = 1/\alpha \times \frac{1}{\alpha} = \frac{1}{\alpha^2}$

$\therefore$ $\boxed{A_G = 1/\alpha^2}$

2) gate capacitance / unit area :- (C_o or C_{ox})

$$C_o = \frac{\epsilon_{ox}}{D}$$

where ϵ_{ox} is permitivity of gate oxide

i.e, $\epsilon_{ox} = \epsilon_o \epsilon_{ins}$ and D is gate oxide -thickness which is scaled by $1/\beta$.

$C_o = \frac{\epsilon_{ox}}{D} = \frac{1}{1/\beta} = \beta$

$\therefore$ $\boxed{C_o = \beta}$

3) Gate capacitance (C_g) :-

$C_g = C_o W L$

where C_o is absolute value i.e, $C_o = \beta$

$C_g = \beta \frac{1}{\alpha} \times 1/\alpha = \beta/\alpha^2$

$\boxed{C_g = \beta/\alpha^2}$

4) Paracetic capacitance (C_x) :-

$$C_x = \frac{A_x}{d}$$

where d - depletion region around source and drain which is scaled by $1/\alpha$ and A_x is areal of depletion region around source and drain which is scaled by $1/\alpha^2$

$$C_x = \frac{A_x}{d} = \frac{1/\alpha^2}{1/\alpha} = 1/\alpha$$

5. carrier density in the channel :- (Q_{ON})

$$Q_{ON} = C_o V_{gs}$$

$C_o - \beta$

$V_{gs} - 1/\beta$

$$Q_{ON} = \beta \times 1/\beta = 1$$

6. ON channel resistance (R_{ON}) :-

$$R_{ON} = \frac{L}{W} = \frac{1/\lambda}{1/\lambda} = 1$$

7. gate delay (T_d) :-

$$T_d = C_g R_{ON}$$

$$= \beta/\lambda^2$$

8. maximum operating freq (f_o) :-

$$f_o = \frac{W}{L} \frac{\mu C_o V_{dd}}{C_g}$$

$$= \frac{1/\lambda}{1/\lambda} \frac{\beta 1/\beta}{\beta/\lambda^2} = 1 \cdot \lambda^2/\beta$$

9. saturation current (I_{ds}) :-

$$I_{ds} = \frac{C_o \mu}{2} \frac{W}{L} [V_{gs} - V_t]^2$$

$$I_{ds} = \frac{\beta}{2} 1/\lambda/1/\lambda \left[1/\beta\right]^2 * 1/\beta^2$$

$$= \beta/2 \; 1/\beta^2$$

$$= \frac{1}{2\beta}$$

10. current density (J) :-

$$J = I_{ds}/A$$

$$J = 1/\beta/1/\lambda^2 = \lambda^2/\beta$$

11. switching energy per gate (E_g) :-

$$E_g = \frac{C_g}{2} V_{DD}^2 = \frac{\beta/\lambda^2}{2} 1/\beta^2 = \frac{1}{\lambda^2 \beta}$$

12. Power disippation per gate :- (P_g)

$$P_g = P_{gs} + P_{gd}$$

where P_{gs} - static Power $= \frac{V_{DD}^2}{R_{ON}}$

$= 1/\beta^2$

P_{gd} - dynamic Power

$$P_{gd} = \epsilon_g f_o = \frac{1}{\alpha^2 \beta} \frac{\alpha^2}{\beta} = \frac{1}{\beta^2}$$

$$P_g = 1/\beta^2 + 1/\beta^2 = 2/\beta^2 \text{ i.e, } 1/\beta^2$$

13. Power disippation per unit area (P_a) :-

$$P_a = P_g/A = \frac{1/\beta^2}{1/\alpha^2} = \alpha^2/\beta^2$$

14. Power speed Product :- (P_t)

$$P_t = F_d \times P_g$$

$$= \beta/\alpha^2 \times 1/\beta^2$$

$$= 1/\alpha^2\beta$$

Scaling effects:-

S.NO	Parameter	combined voltage & dimension	constant electric field ($B=\alpha$)	constant voltage ($B=1$)
1	supply voltage Vdd	$1/B$	$1/\alpha$	1
2.	channel length(L)	$1/\alpha$	$1/\alpha$	$1/\alpha$
3.	width of the -channel (W)	$1/\alpha$	$1/\alpha$	$1/\alpha$
4.	gate oxide thickness (D)	$1/B$	$1/\alpha$	1
5.	Gate area (AG)	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha^2$
6.	Gate capacitance -per unit area (Co)	B	α	1
7.	Gate capacitance cg	B/α^2	$1/\alpha$	$1/\alpha^2$
8.	Paracetic capaci -tance (Cx)	$1/\alpha$	$1/\alpha$	$1/\alpha$
9.	carries density in the channel (QON)	1	1	1
10	ON channel resist -ance (RON)	1	1	1
11.	gate delay (Td)	B/α^2	$1/\alpha$	$1/\alpha^2$
12.	maximum operating -frequency (fo)	α^2/B	α	α^2
13.	saturation current (Ids)	$1/B$	$1/\alpha$	1
14.	current density (J)	α^2/B	α	α^2
15.	switching energy Per gate	$\frac{1}{\alpha^2 B}$	$\frac{1}{\alpha^3}$	$\frac{1}{\alpha^2}$

16	Power dissipation per gate (Pg)	$1/\beta^2$	$1/\alpha^2$	1
17.	Power dissipation per unit area (Pa)	α^2/β^2	1	α^2
18.	Power speed product (Pt)	$1/\alpha^2\beta$	$1/\alpha^3$	$1/\alpha^2$

limitations on scaling:-

substrate doping level:-

So far we discussed about various effects we have neglected the built-in (junction) Potential V_B which interm depends on substrate doping level and this is acceptable so long V_B is small compared to Vdd.

substrate doping scaling factor:-

As the channel length of MOS transistor is reduced, the depletion region width also to be scaled down to prevent source & drain depletion region from meeting. The depletion width 'd' for a junction can be given as

$$d = \sqrt{\frac{2\epsilon V}{qN_B}}, \text{ where } \epsilon = \epsilon_0\epsilon_{ins}$$

q - charge of an electron

N_B - substrate doping level

V - max. applied voltage = Vdd

The built in Potential V_B can be given as

$$V_{B1} = \frac{kT}{q} \ln\left[\frac{N_B N_D}{n_i^2}\right]$$

where N_D – drain & source doping level.

n_i – intrinsic carrier concentration.

if N_B is increase to reduce'd', at the same time V_B is also enlarged thus for combined voltage and dimension scaling model we can write $V_a = mV_B$ where m is a real number.

then $V_a = V_a$; $V = V_a + V_B$

$V = mV_B + V_B$

$$\boxed{V_1 = V_B(1+m)}$$

Now if we scaled down 'V_a' by $1/\beta$, we have

$$V_a = \frac{mV_B}{\beta}$$

$$V_2 = V_a + V_b$$

$$= \frac{mV_B}{\beta} + V_B$$

$$= \frac{mV_B + \beta V_B}{\beta}$$

$$\boxed{V_2 = \frac{V_B(m+\beta)}{\beta}}$$

∴ The effective scaled voltage

$$V_S = \frac{V_2}{V_1} = \frac{V_B(m+\beta)/\beta}{V_B(1+m)} = \frac{(m+\beta)}{\beta(m+1)}$$

$$\boxed{V_S = \frac{m+\beta}{\beta(m+1)}}$$

limitations due to subthreshold current:-

⟹ one of the major concerns in the scaling of devices is the effect on subthreshold current 'Isub' which may be expressed as

$$I_{sub} \propto e^{\frac{(V_{gs}-V_t)}{KT/q}}$$

⟹ when a transistor is at off state, then the value of $(V_{gs}-V_t)$ is Negative and should be as large as possible to minimize 'Isub'.

⟹ As the voltages are scaled down then the ratio of $(V_{gs}-V_t)$ to $\frac{KT}{q}$ will get minimize so that subthreshold current increases.

⟹ for this reason, it may be desirable to scale both V_{gs} and V_{DD} together with V_{DD} by a factor '1/b' $\Rightarrow \frac{1}{a}$.

∴ a is generally greater than b.

⟹ The max electric field across the depletion region is given by $E_{max} = \frac{2V}{d} \propto \frac{2(V_a - V_b)}{d}$ ∵ a>b.

⟹ The Junction breakdown voltage can be given as $BV = \frac{\epsilon_0 \epsilon_{ins} E^2}{2qN_B}$

⟹ Note:-

→ extra care is therefore required in a estimating breakdown voltages for scaled devices.

→ If the electric fields are greater and breakdown voltage is greater at the corners of diffussion regions underlying SiO_2.

limitations on logic levels & supply voltage due to noise:

⇒ The major advantages in the scaling of devices are smaller gate delay time i.e, higher operating frequency & lower internal power consumption.

⇒ The lowering interface spacing and higher switching speeds increased noise in VLSI chips. so noise may also be amplified and this is a major concern.

⇒ The mean square current fluctuations in the channel can be given as

$$\boxed{i^2 = 4KT\, R_n g_m \Delta f} \quad \text{——} (1)$$

where R_n – noise resistance

Δf – bandwidth

$g_m = \beta V_p$

V_p = pinch off voltage $\beta = \frac{\mu W C_{ox}}{L}$

⇒ The equivalent noise resistance R_n can be given as:

$$R_n = \frac{\left[\frac{1}{2}\frac{V_g'}{V_p'} + \frac{1}{6}\right]}{g_m} \quad \text{——} (2)$$

where $V_g' = V_{gs} - V_t + V_B$

$V_p' = V_p + V_B$

i.e, $$R_n = \frac{\left[\frac{1}{2}\left[\frac{V_{gs} - V_t + V_B}{V_p + V_B}\right] + \frac{1}{6}\right]}{g_m}$$

// y The Thermal noise equivalent $R_n g_m$ can be give as

$$R_n g_m = \frac{1}{2}\left[\frac{V_{gs} - V_t + V_B}{V_p + V_B}\right] + \frac{1}{6}. \quad \text{——} (3)$$

⇒ observing eq (3) the value $R_n g_m$ is also dependent on V_g. but only to very small extent.

⇒ The modified expression of P_{ngm} when t_{ox} is scaled can be given as

$$P_{ngm} = \frac{1}{2}\left[\frac{V_g}{V_g - \frac{1}{2}\left(\frac{a}{C_{ox}}\right)^2\left(\frac{1+4g'C_{ox}}{a}\right)^{1/2} - 1}\right] + 1/6$$

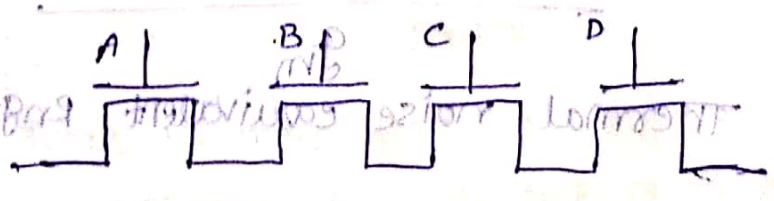
where $a = (2C_{int}.qN_B)^2$

⇒ Thus due to the increase in the value of C_{ox}, P_{ngm} decreased by a small amount which intern decreased the ratio of logic levels to thermal noise by same amount.

Switch logic :-

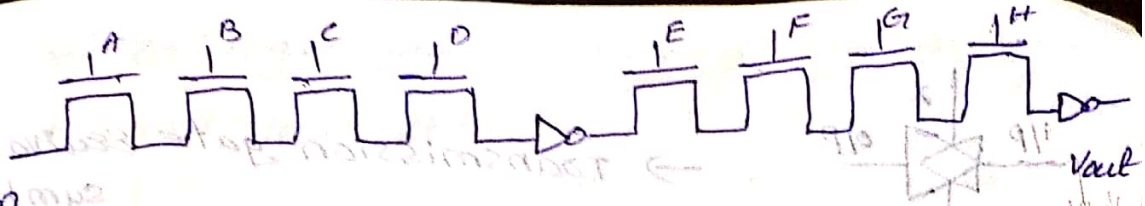
→ switch logic is based on pass transistors (or) in the transmission gates.

* this approach is fast for smaller arrays and takes no static current from supply rails hence power dissipation of such arrays is small. since, current flows only on switching.
* pass transistor logic is similar to logic arrays on relay contact.
* the basic "AND" connections are setout as shown in the fig below, but many combinations of switches are possible.



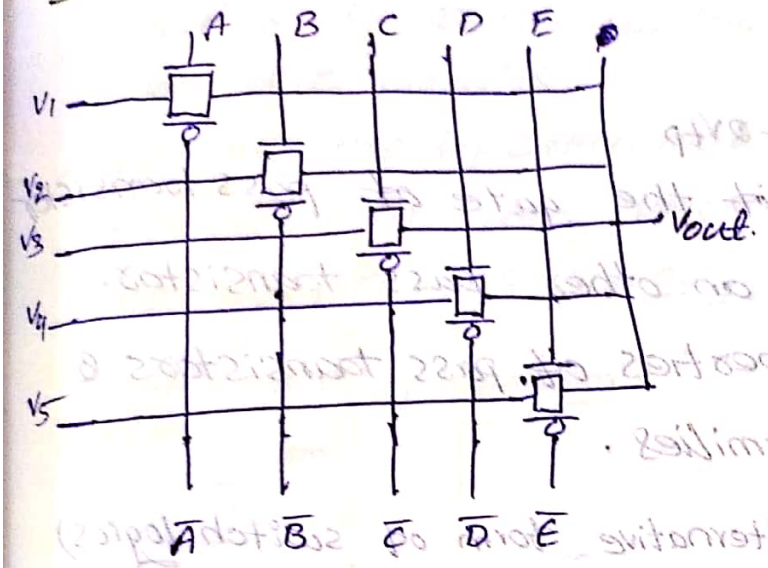
② — $V_{out} = V_{in}$ when $ABCD = 1$

* Here logic levels will be degraded by V_t effects.



$V_{out} = V_{in} - V_{tp}$ when ABCDEFGH=1

cmos 5-way selector switch:-



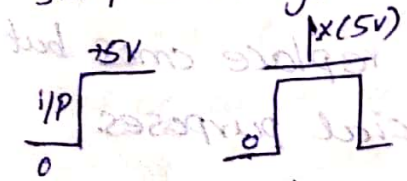
$V_0 = V_1A + V_2B + V_3C + V_4D + V_5E$

* where A, B, C, D, E are "mutually exclusive elements"

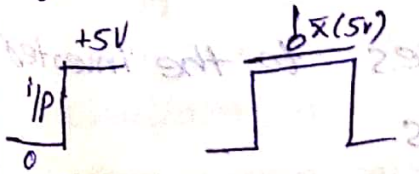
Note:- Here "Vout" logic levels degradation not occurs and i.e free from "V_t" elements.

pass transistor & transmission gates:-

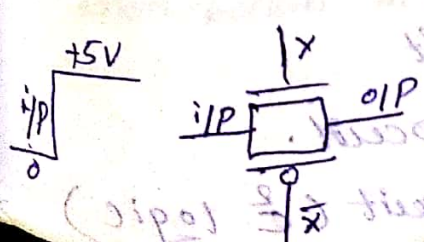
switches and switch logics may be toom from simple n-type (or) P-type pass transistors



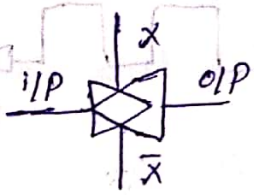
→ n-switch degrades logic '1'.



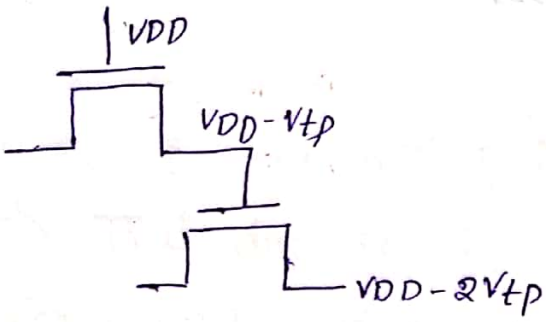
→ p-switch degrades logic '0'.



→ Transmission gate with good logic levels



→ Transmission gate equivalent symbol.



* Loss of logic '1' in the gate of pass transistor of driven from an other pass transistor.
* fig. some properties of pass transistors & some logic families.

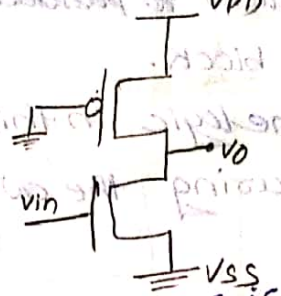
Gate logic :- (or) (Alternative form of switch logics)
(or) Alternative Gate logic.

* cmos circuits suffers from increased Area and corresponding increased capacitance and delays as logic gates become more complex.
* for this reason, the designers developed the circuits that can be used to supplement complementary circuits.
* These are not supposed to replace cmos but either to be used for special purposes.
* we have, various alternatives to the inverter based cmos logic circuits.
  (i) pseudo nmos logic circuit.
  (ii) dynamic cmos logic circuit.
  (iii) clocked cmos logic circuit (C²MOS logic)

(iv) Domino logic ckt.

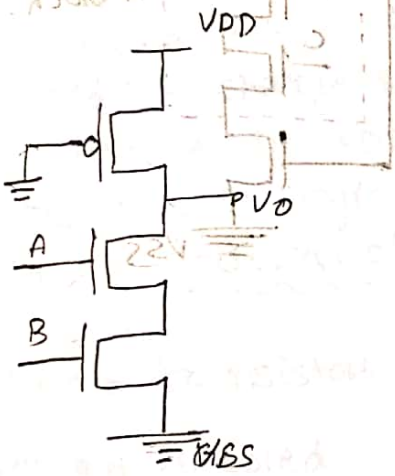
(v) np cmos logic ckt.

(i) Pseudo nmos logic circuit:-

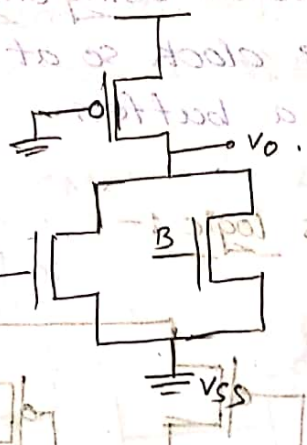


* pseudo nmos logic is one of the type of Alternative gate logic circuits i.e; used to supplement cmos logic circuits.
* In this the depletion mode pullup nmos is to be replaced with pmos and the Gate terminal of pmos is always connected to ground.

2 i/p NAND using pseudo nmos



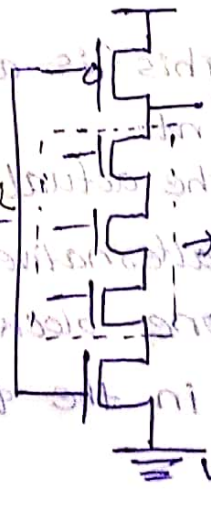
2 i/p NOR using pseudo nmos



(ii) Dynamic cmos logic circuit:-

The actual logic is implemented in the nmos logic and a p-transistors is use for non-time critical pre-charging of output. ie the o/p capacitance is charged to VDD during off period of clock signal ϕ.

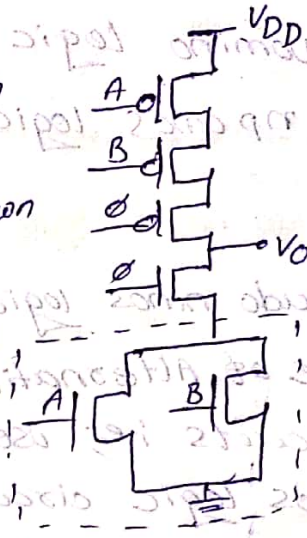
During this gate time, inputs are applied to n-block and state of logic is then evaluated during ON period of clock when bottom nmos will get ON.



3) clocked cmos logic :-

→ The logic is implemented in both n & p transistors in the form of pullup p-block & pulldown n-block.

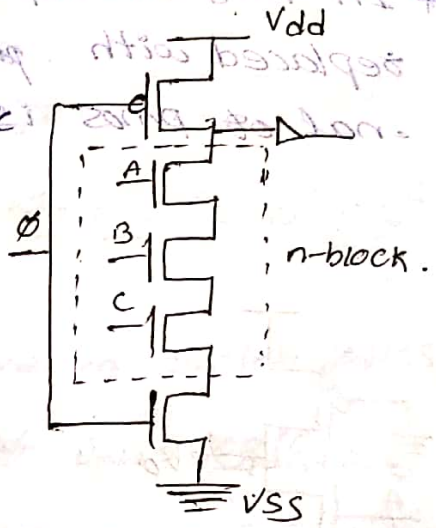
→ the logic in this case is evaluated during the ev period of clk.



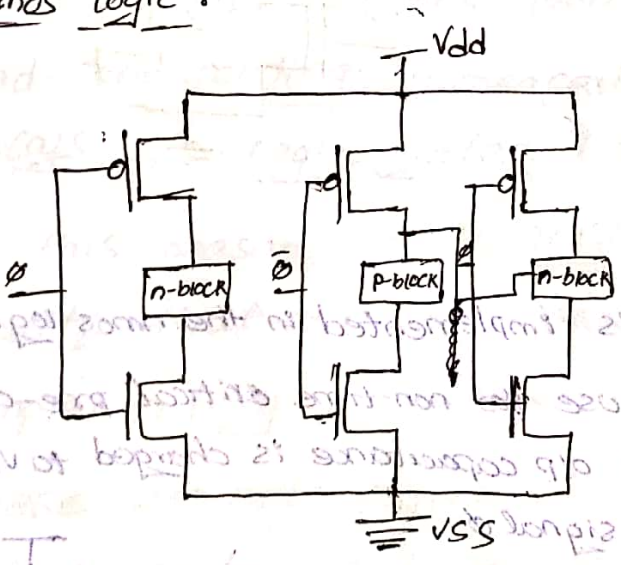
4) Domino cmos logic :-

→ An extension of dynamic cmos logic ckt is called domino logic

→ This is modified arrangment that allows of cascading logic structures using only single phase clock so at the we use a buffer.

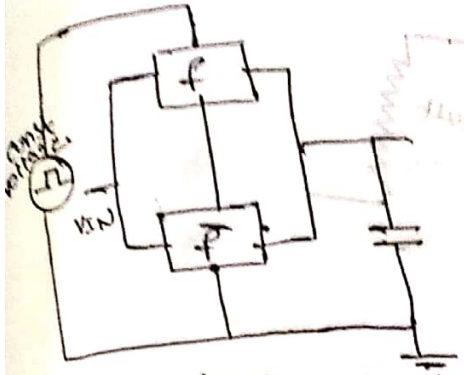


5) npcmos logic :-

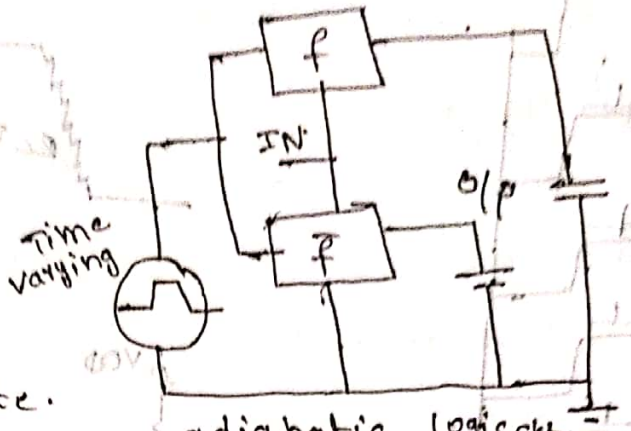


* This is another version basic dynamic logic arrangement.
* the actual logic blocks n & p are arranged in the alternative format in cascaded structure.
* one block is fed with clock signal $\bar{\phi}$. as shown in the figure above.

6th unit:-



conventional CMOS logic gate.



adiabatic logic ckt.

operation of adiabatic logic gate:-

⇒ replace each of PMOS & NMOS devices in the PUNUP & Pulldown N/w with transmission gate

⇒ use expanded PUNUP N/w to drive true o/p.

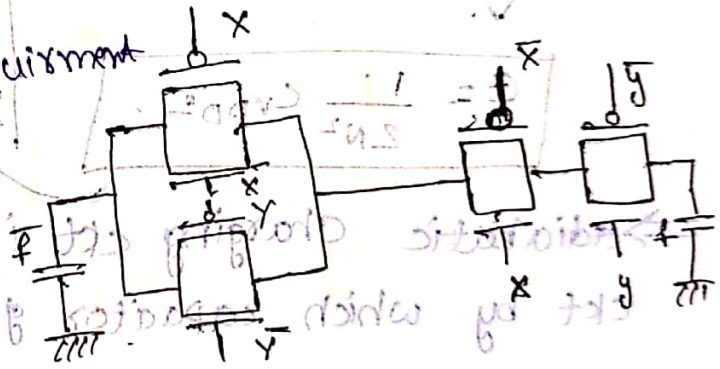
⇒ use expanded Pulldown N/w to drive complimentary o/p.

⇒ Both N/w's in the transformed ckt are used to charge & discharge load capacitance.

⇒ Replace DC VDD by a timevarying VDD by allow adiabatic logic.

Implimentation of adiabatic CMOS 2 i/p NAND/AND:-

⇒ note:- No. of transistors requirment will get doubled



$V_A = f$ if $X=1, Y=1$ (AND)

$V_A = \bar{f}$ if $X=0, Y=0$ (or) X & $Y=0$ (AND)