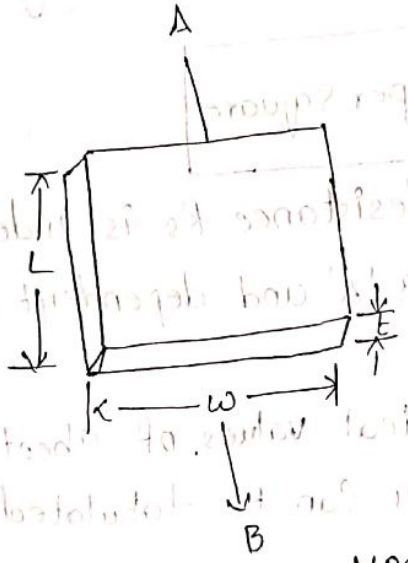
UNIT-II

31/12/18

Basic Circuit Concepts

Sheet Resistance (R_S):-

The concept of sheet Resistance can be understood by Considering a uniform slab material as shown in the figure below.



Sheet Resistance model

* So from the given diagram we can say that it is having a length of 'L' and width of 'w' and with a thickness of 't'.

* The Resistance blw the terminals A and B can be given as R_{AB}.

$$R_{AB} = \frac{\rho l}{A}$$

where ρ - resistivity

l - length of the material

A - cross-sectional Area

* for a uniform slab $L = w$

WKT $R_{AB} = \rho l / A$

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$$R_{AB} = \frac{\rho l}{A}$$

$$R_{AB} = \frac{\rho l}{wt}$$

$$= \frac{\rho l}{wt} \quad (\text{uniform slab } l = w)$$

$$\boxed{R_{AB} = \frac{\rho}{t}}$$

∴ The sheet Resistance R_s can be given as

$$\boxed{R_s = \frac{\rho}{t} \ \Omega \text{ per square}}$$

Note:- The sheet Resistance R_s is independent of Cross-sectional Area 'A' and dependent on thickne 't'.

* Some of the typical values of sheet Resistance f different technologies can be tabulated as like be

Layer	sheet Resistance		
	5μm	2μm (orbit)	1.2μm
Metal	0.03	0.04	0.04
Diffusion (Active)	10→50	20→45	20→45
silicid side	2→4		
polysilicon	15→100	15→30	15→30
N-transistor channel	10^4	2×10^4	2×10^4
P-transistor channel	2.5×10^4	4.5×10^4	4.5×10^4

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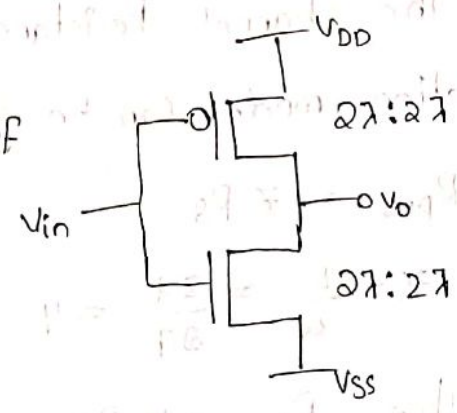
Sheet Resistance Concept Applied to MOS transistors and Inverters:-

The sheet Resistance concept can be extended to inverters.

Here let us consider a cmos inverter as shown below.



* The channel Resistance of pmos can be given as

$R_{pus} = ZR_s$

WKT $Z = \frac{L}{\omega}$

$\Rightarrow \frac{2\lambda}{2\lambda} = 1$

$R_{pus} = 1 \cdot R_s$

$= (2.5 \times 10^4)$

$R_{pus} = 25\ k\Omega$

Rs values can be taken for 5μm technology for convience.

* The channel resistance of nmos can be given as

$R_{pds} = Z \cdot R_s$

$Z = \frac{L}{\omega}$

$= \frac{2\lambda}{2\lambda} = 1$

$R_{pds} = 1 \cdot R_s$

$= 1(10^4)$

$R_{pds} = 10\ k\Omega$

∴ the ON channel Resistance of cmos inverter is

$R_{ON} = R_{pus} + R_{pds}$

$= 25k\Omega + 10\ k\Omega$

$= 35\ k\Omega$

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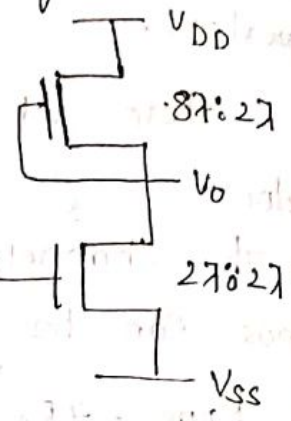
Sheet Resistance Concept Applied for nmos Inverter:

The nmos Inverter is diagramtically as shown below.



The channel Resistance of depletion mode can be given as

$$R_{pus} = Z \cdot R_s$$

$$Z = \frac{L}{\omega} = \frac{8\lambda}{2\lambda} = 4$$

The $R_{pus} = 4 \cdot R_s$

$$= 4 \cdot (2.5 \times 10^4)$$

$$= 40k\Omega$$

The channel Resistance of enhancement mode Can be given as

$$R_{pds} = Z \cdot R_s$$

$$Z = \frac{L}{\omega} = \frac{2\lambda}{2\lambda} = 1$$

$$R_{pds} = 1 \cdot R_s$$

$$= 1(10^4)$$

$$= 10k\Omega$$

$\therefore$ The ON channel Resistance of nmos inverter can be is $R_{ON} = R_{pus} + R_{pds}$

$$= 40k\Omega + 10k\Omega$$

$$= 50k\Omega$$

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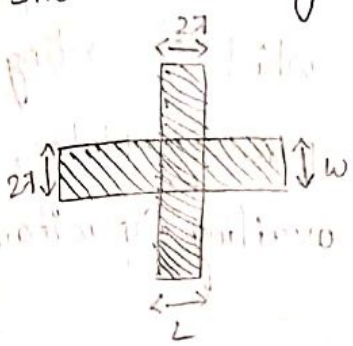
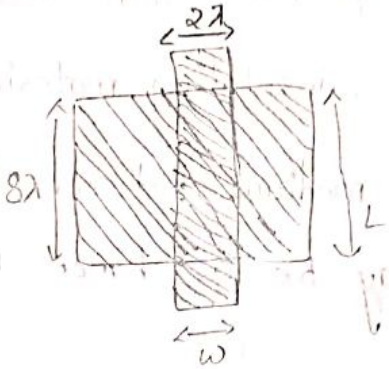
the sheet Resistance Concept can be extended for transistors, for example consider two transistors as shown in figure 'a' and 'b' shown below.



L : W
2λ : 2λ

figure 'a'



L : W
8λ : 2λ

figure 'b'

In the above diagrams figure a is having a length of '2λ' and a width of '2λ' and figure b carriex a length of '8λ' with a width of '2λ'.

for a fig 'a' the channel Resistance can be calculated as $R = ZR_S$

where $Z = \frac{L}{W} = \frac{2\lambda}{2\lambda} = 1$

$R = 1 \cdot R_S$

$R = 1 \cdot (10^4)$

$= 10 K\Omega$

the channel Resistance for fig 'b' can be calculated as $R = Z \cdot R_S$

$Z = \frac{L}{W} = \frac{8\lambda}{2\lambda} = 4$

$R = 4 \cdot R_S$

$= 4(10^4)$

$R = 40 K\Omega$

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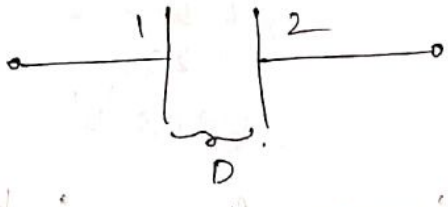
Area Capacitance of Layers :-

MOS

In the IC fabrication process, the layers can be seperated from one another by a oxide layer (i.e, insulating material) which is acting as dielectric medium between two parallel plates, so their may be a chance of availing Capacitance.



The Capacitance 'C' can be given as

$$C = \frac{\epsilon A}{D}$$

Where ϵ = permitivity and can be given as

$\epsilon = \epsilon_0 \epsilon_{ins}$

$\epsilon_0 \rightarrow$ Absolute permitivity (or) permitivity of free space. (8.854×10^{-12} faraday/meter)

$\epsilon_{ins} \rightarrow$ Relative permitivity = 4 for silicon

A = Area of plates

D = thickness of SiO_2

* Some of the typical values of Capacitance for 5um, 2um and 1.2um technologies can Are tabulated below.

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Capacitance	Value in $PF \times 10^{-4}/\mu m^2$ (relative values in brackets)		
	5μm	2μm	1.2μm
gate to channel capacitance	4 (1.0)	8 (1.0)	16 (1.0)
diffusion (active)	1 (0.25)	1.75 (0.22)	3.75 (0.23)
polysilicon to substrate	0.4 (0.1)	0.6 (0.075)	0.6 (0.038)
Metal 1 to substrate	0.3 (0.075)	0.33 (0.04)	0.33 (0.02)
Metal 2 to Substrate	0.2 (0.5)	0.17 (0.02)	0.17 (0.01)
Metal 2 to Metal 1	0.4 (0.1)	0.5 (0.06)	0.5 (0.03)
Metal 2 to polysilicon	0.3 (0.075)	0.3 (0.038)	0.3 (0.018)

Standard unit of Capacitance ($\square C_g$):-

The standard unit of capacitance can be define as gate to channel capacitance of a MOS transistor having the feature size of $L = W$.

Here, for example standard unit of capacitance can be calculated for different technologies.

for 5μm technology:-

The area per standard square $= 5\mu m \times 5\mu m$
$= 25\mu m^2$

The standard unit of capacitance ($\square C_g$) can be given as

$\square C_g$ = Area/standard square × capacitance

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$\Rightarrow 25\mu m^2 \times 4\times10^{-4}\ pF/\mu m^2$

$\Rightarrow 100\times10^{-4}\ pF$

$\square C_g = 0.01\ pF$

for 2um technology

Area/standard, square = $2\mu m \times 2\mu m$

$= 4\mu m^2$

The standard unit capacitance ($\square C_g$) can be given as

$\square C_g$ = Area/standard square x capacitance

$= 4\mu m^2 \times 8\times10^{-4}\ pF/\mu m^2$

$= 32\times10^{-4}\ pF$

$= 0.0032\ pF$

for 1.2um technology

Area/standard Square = $1.2\mu m \times 1.2\mu m$

$= 1.44\mu m^2$

The standard unit Capacitance ($\square C_g$) can be given as

$\square C_g$ = Area/standard Square x Capacitance

$= 1.44\mu m^2 \times 16\times10^{-4}\ pF/\mu m^2$

$= 23.04\times10^{-4}\ pF$

$= 0.023\ pf$

Some Area Capacitance Calculations:-

In this the relative values of capacitance can be used for the representation of capacitance and all values carried out in 'λ' based rules.

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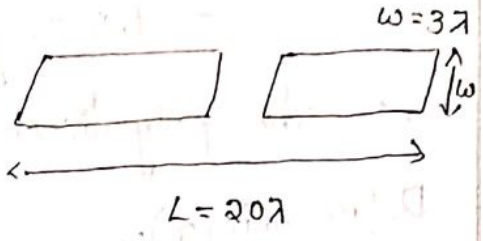
The relative Area can be represented as the ratio of Area of interest to the standard Area.

$$\therefore \text{Relative Area} = \frac{\text{Area of interest}}{\text{standard Area}}$$



$$\text{Relative Area} = \frac{20\lambda \times 3\lambda}{2\lambda \times 2\lambda}$$

$$= \frac{60\lambda^2}{4\lambda^2} = 15$$

(*) for 5μm technology

(1) The Capacitance to substrate can be given as

⇒ Relative area × Capacitance

$= 15 \times 0.075 \square Cg$

$= 1.125 \square Cg$

∴ The Capacitance to substrate is $1.125 \square Cg$ times of Square Cg ($\square Cg$).

(2) The diffusion Capacitance can be calculated as = Relative area × Capacitance

$= 15 \times 0.25 \square Cg$

$= 3.75 \square Cg$

∴ The diffusion Capacitance is 3.75 times of $\square Cg$.

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3) For polysilicon

The capacitance for polysilicon can be calculated as = Relative Area x Capacitance.

$= 15 \times 0.1 \square C_g$

$= 1.5 \square C_g$

∴ the polysilicon capacitance is 1.5 times of $\square C_g$

Delay unit (τ):-

The delay unit (τ) can be given as the product of Sheet Resistance (R_s) and standard unit of gate Capacitance ($\square C_g$).

$$\boxed{\tau = R_s \square C_g}$$

for 5μm technology

WKT $\tau = R_s \square C_g$

$= 10^4 \times 0.01 pf$

$= 10^4 \times 0.01 \times 10^{-12}$

$= 100 \times 10^{-12}$

$= 1 \times 10^{-10}$

$= 0.1 \times 10^{-9}$

$\tau = 0.1 nsec$

for 2μm technology

WKT $\tau = R_s \square C_g$

$= 2 \times 10^4 \times 32 \times 10^{-4} pf$

$= 64 pf$

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$\tau = 64 \times 10^{-12}$

$= 0.064 \times 10^{-9}$

$\tau = 0.064$ nsec

for 1.2 μm technology

$\tau = Rs \, Cg$

$= 2 \times 10^{4} \times 23.04 \times 10^{-4}$ pf

$= 46.08 \times 10^{-12}$

$\tau = 0.046$ nsec

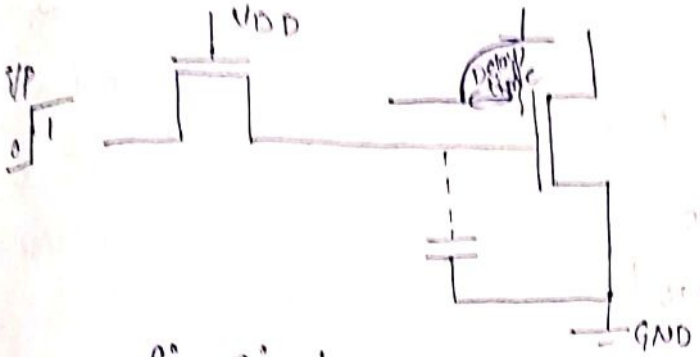

fig: Simple model to calculate delay time.

We know that the electron transit time τ_{ds} as

$$\tau_{ds} = \frac{L^2}{\mu V_{ds}}$$

* when i/p signal is transmitted through the pass transistors the output voltage will get reduce to 63% of V_{DD} that is $0.63 \times V_{DD}$

$= 0.63 \times 5V$

$\simeq 3V$

* for 5μm technology

$$\tau_{ds} = \frac{L^2}{\mu V_{ds}}$$

$$= \frac{5\mu m \times 5\mu m}{650 cm^2/V\text{-sec} \times 3V}$$

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$$= \frac{25\times(10^{-6})^2 m^2}{650(0.01)cm^2/Vsec \times 3V}$$

$$= \frac{25\times10^{-12}}{650\times0.01\times3} \text{ sec}$$

$$= \frac{25\times10^{-12}}{19.5}$$

$$= \frac{25\times10^{-3}\times10^{-9}}{19.5}$$

$$= \frac{2.5\times10^{-9}}{19.5\times10^{3}}$$

$$= 0.128\times10^{-9}$$

$$\simeq 0.13 \text{ nsec}$$

Note:- The delay unit 'τ' is approximately equal to the electron transit time 'τ_{ds}'.

Inverter Delay:-

nmos Inverter Delay:-

Here let us consider an nmos inverter with a ratio of 4:1.

The pullup to pulldown ratio of nmos driven by another nmos is 4:1.

i.e., $\frac{Z_{pu}}{Z_{pd}} = \frac{4}{1}$

$Z_{pu} = 4 Z_{pd}$

$Z_{pu} = 4 R_s$

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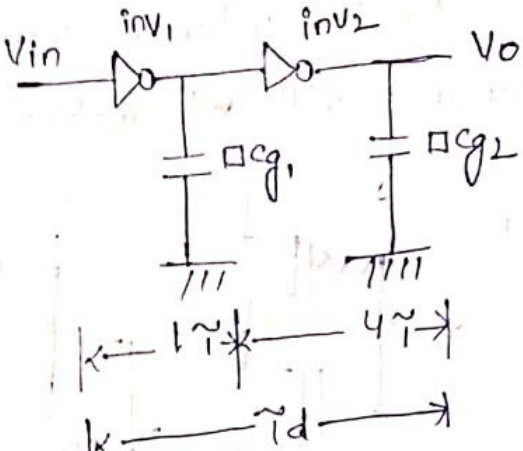
$$\frac{R_{pu}}{R_{pd}} = \frac{4}{1}$$

$$R_{pu} = 4R_{pd}$$

$$R_{pu} = 4R_s$$

$$R_{pu} = 4 \times 10^4$$

$$\boxed{R_{pu} = 40\,K\Omega}$$



* the delay is not effected by the cascade connections of inverters but it is due to the turning on/off actions

* the total delay τ_d is the combination of both inverters.

i.e, $\tau_d = 1\tau + 4\tau$

$= \tau[1+4]$

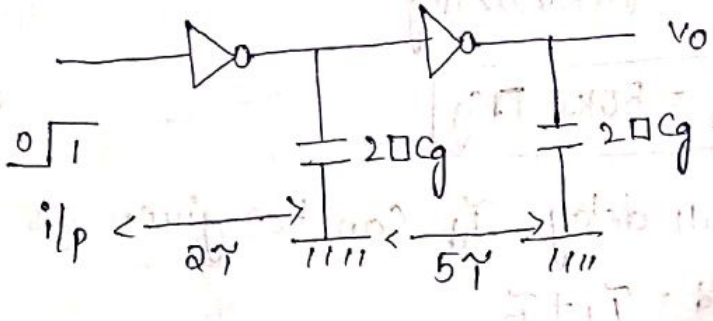
$= \tau\left[1+\frac{4}{1}\right]$

$$\boxed{\tau_d = \tau\left[1+\frac{Z_{pu}}{Z_{pd}}\right]}$$

∴ The total delay for an nmos inverter is $\tau_d = 5\tau$.

CMOS Inverter Delay:-

Here let us consider an arrangement shown below for the Calculation of CMOS inverter delay.



fig(a)

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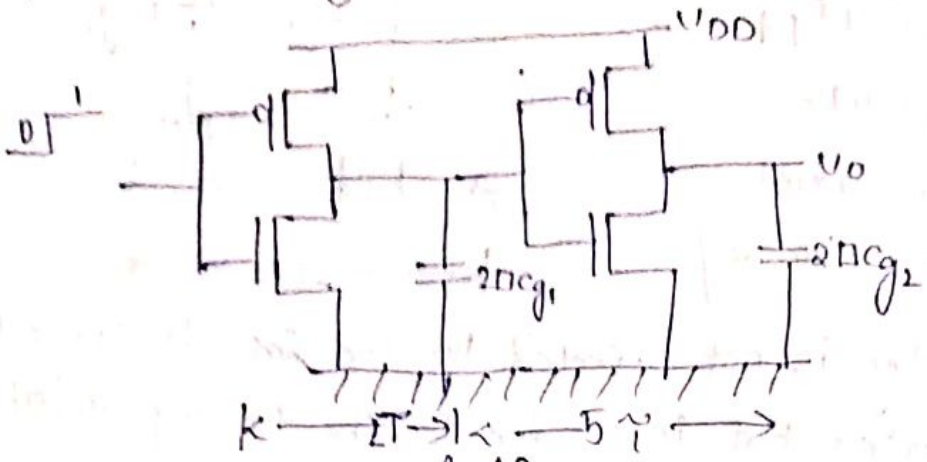
Due to the internal wiring Capacitance the load Capacitance will get doubled that is $2\square C_g$.



fig(b):

* when i/p is V_{DD} (logic 1) then the nmos of inverter will get on and the Capacitor will get discharge path through the nmos.

i.e., $\tilde{\tau}_1 = R_n 2\square C_g$

$$\boxed{\tilde{\tau}_1 = 20K\Omega\,\square C_g}$$

* when the capacitor off inverter 1 is discharge then at the input of inverter 2 we have logic '0'.

i.e, pmos of inverter 2 will get on and the Capacitor will get charge..

$$\tilde{\tau}_2 = R_p 2\square C_g$$

$$= (25\,K\Omega)\times 2\,\square C_g$$

$$\boxed{\tilde{\tau}_2 = 50K\Omega\,\square C_g}$$

∴ The overall delay $\tilde{\tau}_d$ can be given as

$$\tilde{\tau}_d = \tilde{\tau}_1 + \tilde{\tau}_2$$

$$= 20K\Omega\,\square C_g + 50K\Omega\,\square C_g$$

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$= 2R_s \square C_g + 5R_s \square C_g$

$= R_s \square C_g [2+5]$

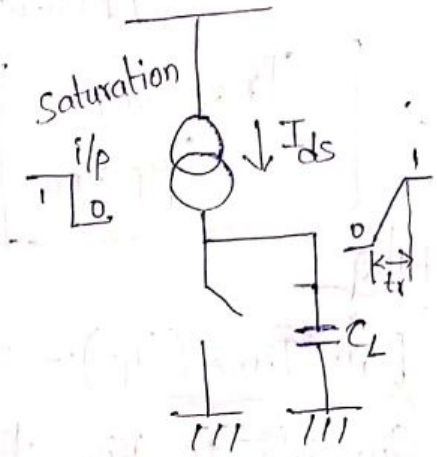
$\boxed{\tilde{T}_d = 7\tilde{T}}$

∴ The overall delay of cmos inverter is $7\tilde{T}$.

* The overall delay can be better understood with a calculations of Rise time (T_r) and fall time (T_f).

Rise time Calculation (T_r):-

The calculation of Rise time 'T_r' can be done when input is logic '0'.



WKT I_{ds} for saturation

$$I_{ds} = \frac{k\omega}{L}\left[\frac{V_{gs}-V_t}{2}\right]^2$$

$$I_{ds} = \beta_p\left[\frac{V_{gs}-V_{tp}}{2}\right]^2 \longrightarrow (1)$$

$$V_{out} = I_{ds} R \longrightarrow (2)$$

WKT $\tilde{T}_r = RC_L$

$$\therefore \boxed{R = \frac{\tilde{T}_r}{C_L}} \longrightarrow (3)$$

Sub (3) in (2)

$$V_{out} = I_{ds} \cdot \frac{T_r}{C_L}$$

$$\tilde{T}_r = \frac{V_{out} C_L}{I_{ds}}$$

$$= \frac{V_{out} C_L}{\beta_p\left[V_{gs}-V_{tp}\right]^2/2}$$

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$$T_r = \frac{2 V_{out} C_L}{\beta_P [V_{gs} - |V_{tp}|]^2}$$

$V_{gs} = V_{DD}$

$V_{out} = V_{DD}$

$V_{tp} = 0.2 V_{DD}$

$$T_r = \frac{2 \cdot V_{DD} C_L}{\beta_P [V_{DD} - 0.2 V_{DD}]^2}$$

$$= \frac{2 V_{DD} C_L}{\beta_P [0.64] V_{DD}^2}$$

$$= \frac{2 C_L}{\beta_P (0.64) V_{DD}}$$

$$\therefore \boxed{T_r \simeq \frac{3 C_L}{\beta_P V_{DD}}}$$

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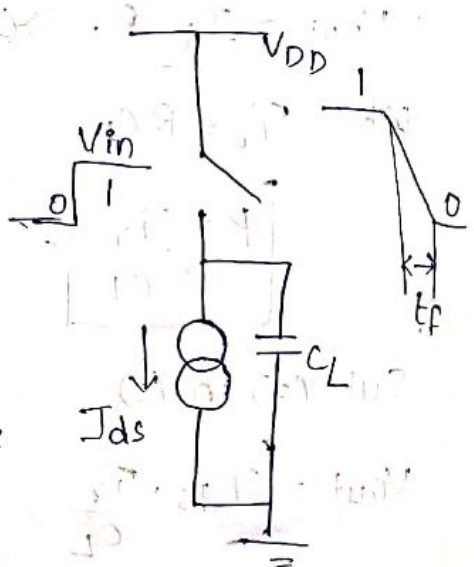
Fall Time (T_f):- The fall time (T_f) can be Calculated Similarly to Rise time (T_r) Calculation.

* The fall time T_f can be given as

$$\boxed{T_f = \frac{3 C_L}{\beta_n V_{DD}}}$$

(reference from Rise time Calculation)



* The ratio of Rise time to fall time can be given as

$$\frac{T_r}{T_f} = \frac{3 C_L / \beta_P V_{DD}}{3 C_L / \beta_n V_{DD}}$$

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$$\frac{T_r}{T_f} = \frac{\beta_n}{\beta_p}$$

$\therefore$ $T_r \propto \frac{1}{\beta_p}$ and fall Time $T_f \propto \frac{1}{\beta_n}$

* The rise time 'T_r' and fall time 'T_f' both are $\propto C_L$ and $\propto \frac{1}{V_{DD}}$.

Driving large capacitive loads:-

* The concept of Driving large capacitive loads may arise when the signals are propagating from on-chip to off-chip periphals, which are having Comparitively very large values.
* Here the load capacitance 'C_L' is equal orders > than the gate capacitance 'C_g' i.e.,

$$C_L > 10^4 C_g \text{ [Assumption].}$$

* Inorder to have decreased delay we need to maintain increased channel length which may furthur decrease the resistance.
* To drive large capacitive loads we are having 3 techniques.

1. Cascoded Connections of inverters as drivers.
2. Superbuffers as drivers.
3. Bi-cmos drivers.

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1. Cascaded Connections of Inverter & as drivers:-

* when driving large capacitive loads to have a minimum delay we should have low resistances.
* Low resistances can be obtained by having low Zpu & Zpd's

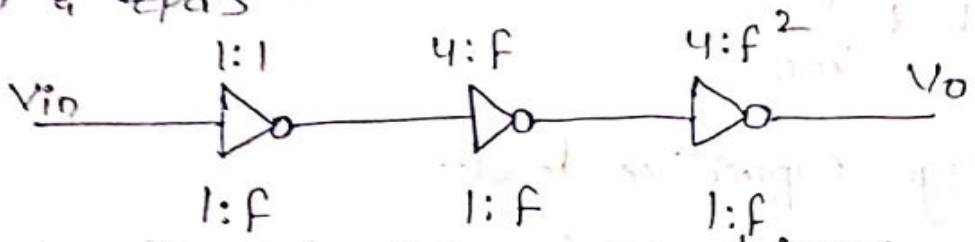

fig:- Cascaded inv as drivers

* the arrangement of Cascaded inverters as drivers is shown below.
* If we increase the width factor 'f' then the load on capacitance may increased that results in larger capacitive area.
* If there is Increase in width factor then the resistance will get automatically decrease thereby we can have minimum delay.

for nmos:- Delay/stage = $1f\tau$ for ΔVin

$= 4f\tau$ for ∇Vin

$\tilde{\tau}_d = 1f\tau + 4f\tau = 5f\tau$

for cmos:- Delay/stage $= 2f\tau$ for ΔVin

$= 5f\tau$ for ∇Vin

$\tilde{\tau}_d = 2f\tau + 5f\tau = 7f\tau$

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* The relation b/w no. of inverters 'N' to width function 'f' can be given as

$$N^f = \frac{C_L}{C_g} = y$$

$$N^f = y$$

Apply 'log' on both sides

$$f \log N = y$$

* If $\boxed{f = e}$, $e \log N = y$.

$$N \log e = y$$

$$\boxed{N = y}$$

* If N = even, then the delay is

$$\tilde{\tau} = \frac{N}{2} 5f\tilde{\tau} = 2.5 f\tilde{\tau} \text{ for nmos}$$

$$\tilde{\tau} = \frac{N}{2} 7f\tilde{\tau} = 3.5 f\tilde{\tau} \text{ for cmos}$$

* If N = odd, then the delay is

$$\tilde{\tau} = [2.5(N-1)+4] f\tilde{\tau} \text{ for nmos} \Big\} \nabla V_{in}$$
$$\tilde{\tau} = [3.5(N-1)+5] f\tilde{\tau} \text{ for cmos} \Big\} \nabla V_{in}$$

$$\tilde{\tau} = [2.5(N-1)+1] f\tilde{\tau} \text{ for nmos} \Big\} \Delta V_{in}$$
$$\tilde{\tau} = [3.5(N-1)+2] f\tilde{\tau} \text{ for cmos} \Big\} \Delta V_{in}$$

Note:- If there is increasing width factor 'f' then no. of transistors per chip will get reduced.

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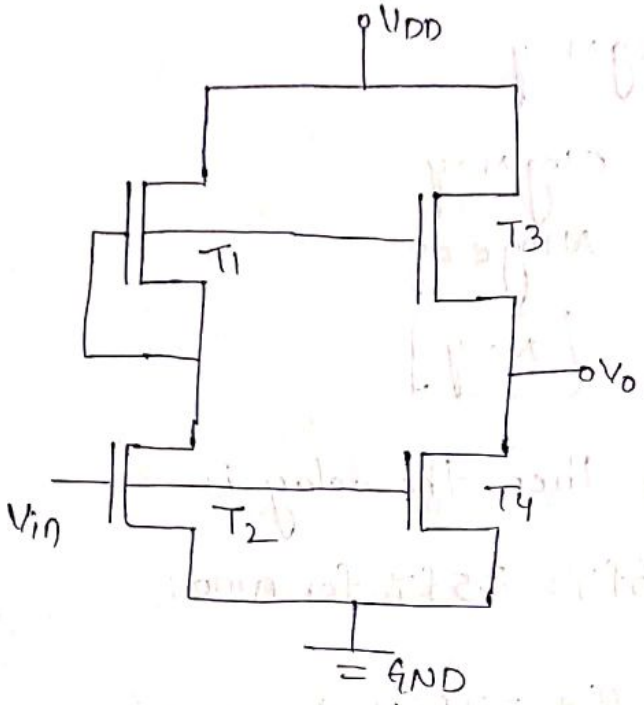
2. Superbuffers as drivers:- It is classified into two types.

1. Inverting type super buffers
2. Non inverting type superbuffers

1. Inverting type Superbuffers:-



* When Vin is logic '0' then the transistors T_2 & T_4 will get off and the transistor T_1 & T_3 will get on, thereby producing o/p as logic '1'.
* If Vin is logic '1' then the transistors T_1 & T_3 will get on and the transistors T_2 & T_4 will get on thereby producing o/p as logic '0'.

2. Non-inverting type Superbuffers:-

* When Vin is logic '0' then the transistors T_1 & T_4 will get on and the transistors T_2 & T_3 will get off thereby producing o/p as logic '0'.

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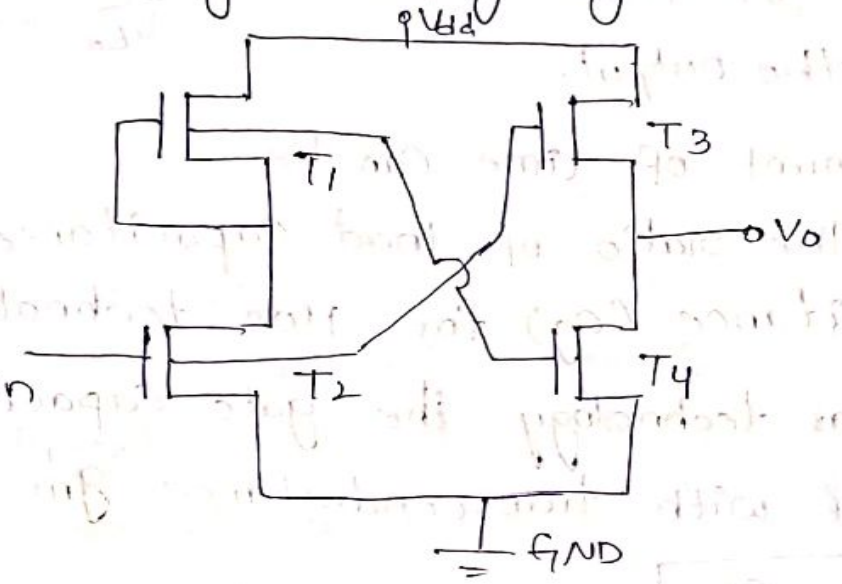
* when Vin is logic '1' then the transistors T_2 & T_3 will get on and the transistors T_1 & T_4 will get off and thereby producing logic '1'.



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Bicmos Divers:-

1. In Bipolar technology, the output drive current is more for a given minimum Silicon area.
2. In this the transconductance gm and low current driving capabilities and current/area (or) more compared to MOS technology.

* in this the current I_c is exponentially related to the input voltage.

* in this technology it is having the capability of driving large currents for the application of smaller voltages. and the current through the device depends on the base width W_b and the amount of doping level.

A simple representation that is use bipolar technology to change their states is shown below.

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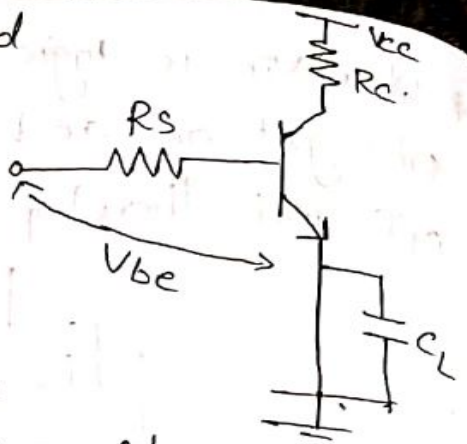
* The amount of time required to change the input is equal to amount of time taken to change the output.



* The amount of time can be given as the ratio of load capacitance (CL) to gate capacitance (Cg) for Mos technology $\Delta t = \frac{C_L}{C_g}$.

* In Bipolar technology the gate capacitance 'Cg' is replaced with transconductance 'gm'.

$$\Delta t = \frac{C_L}{g_m}$$

* Therefore the total time taken can be represented as follows

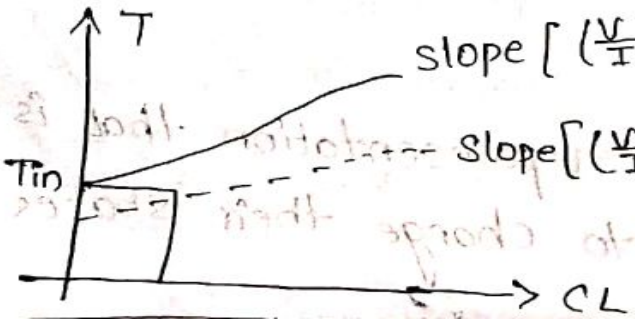
$$T = T_{in} + \left(\frac{V}{I}\right) C_L \frac{1}{h_{fe}}$$ for bipolar

where Tin - the inbuilt time produced by device

CL - load capacitance

hfe - current amplification factor.

The graphical representation of mos and bipolar technology are drawn as below:



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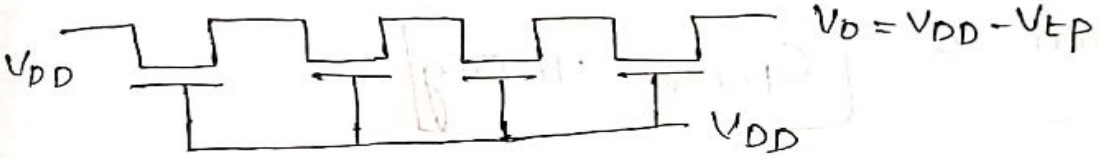
$T = T_{in} + \left(\frac{V}{I}\right) C_L$ for cmos

propagation delays:-

To transfer logic levels from one place to another place we are using series of pass transistors in b/w two points.

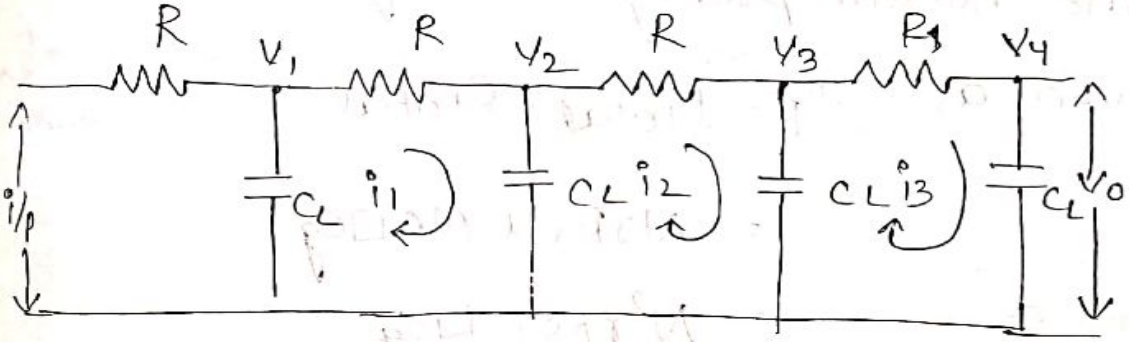
Here in this case nmos pass transistors are use in series connection, all the gate terminals are tight together and it is beengiven V_{DD}.

for example a series of four pass transistors are shown below.



Model for propagation delay

The equivalent circuit model can be drawn as



At node 2, we get write $C\frac{dV_2}{dt} = i_1 - i_2$

$$C\frac{dV_2}{dt} = \frac{V_1 - V_2}{R} - \frac{V_2 - V_3}{R}$$

$$C\frac{dV_2}{dt} = \frac{V_1 - 2V_2 + V_3}{R}$$

$$RC\frac{dV_2}{dt} = V_1 - 2V_2 + V_3$$

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$$Rc\frac{dv}{dt} = \frac{d^2x}{dx^2}$$

$\therefore x \Rightarrow$ distance

$\therefore$ the propagation delay $t_p \propto x^2$.

* For 'N' no of networks the total resistance can be given as $\boxed{R_{total} = N\gamma R_s}$

where R_s - sheet Resistance

γ - relative Resistance

N - no. of stages

* For 'C' the total no of capacitance can be given as $\boxed{C_{total} = NC\square C_g}$

Where C -

* The overall propagation delay 'tp' can be given as $t_p = R_{total} \times C_{total}$

$$= N\gamma R_s \times NC\square C_g$$

$$= N^2\gamma R_s C \square C_g$$

$$= N^2\gamma C R_s \square C_g$$

$$\boxed{t_p = N^2\gamma C\tau}$$

$$\boxed{\tau = R_s \square C_g}$$

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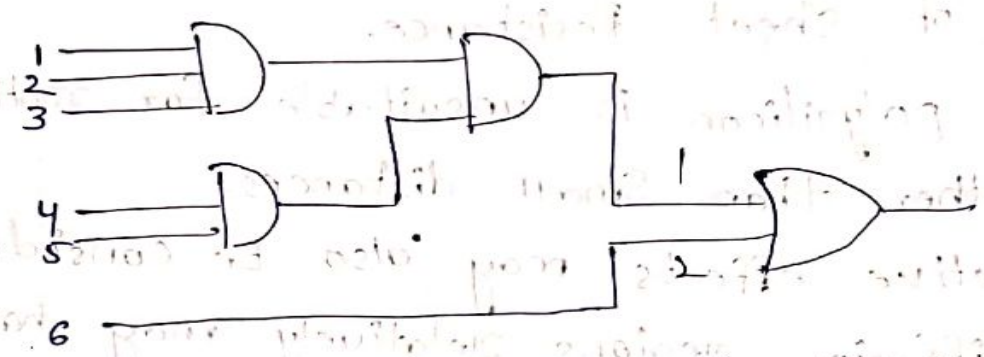
∴ The propagation delay is αN^2.

If there is increase in N, it results in increased propagation delay.

fan-IN and fan-out characteristics:-

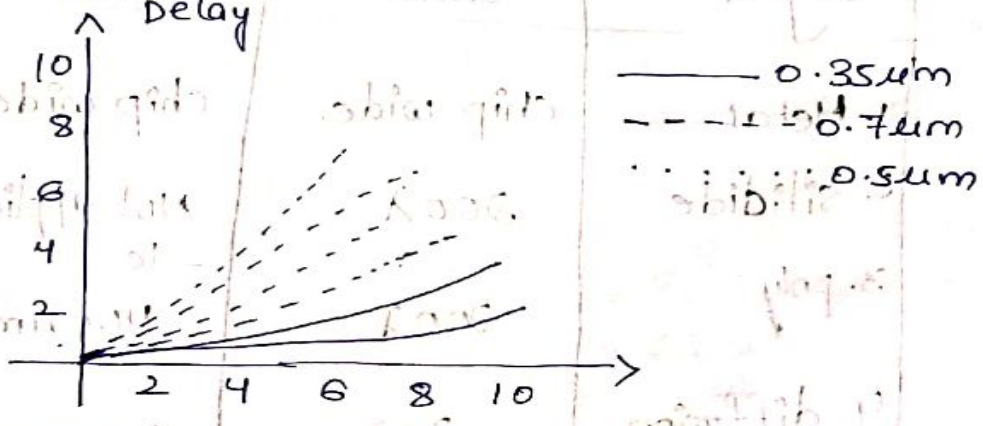
We have two major factor that influence operational speed of a gate terminal these are fan-IN and fan-out.

fan-IN :- The maximum no. of inputs that are applied to driven in gate is called fan-IN



Fan-out:- The max no. of i/p's that are applied to driven gate is called fan-out.

* The delay associated with Fan-in & Fan-out for three technologies is represented as



Fan-in & Fan-out characteristics

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Choice of layers :-

In designing circuits for our convience of Suitable specifications we have to consider several Number of considerations which includes choice of layers

1. V_{DD} and V_{SS} should be distributed on metal layer whenever possible.
2. The length of polysilicon should be use after careful consideration because of relatively high value of sheet Resistance.
3. The polysilicon is unsuitable for routing V_{DD} & V_{SS} other than small distances.
4. Capactive effects may also be consider because the diffusion regions relatively may have high capactive values to the substrate.

Table for electrical roots:-

	Max length of wires		
Layers	5μm	2μm	1.2μm
1. Metal	chip wide	chip wide	chip wide
2. Silidide	200λ	Not applicable	Not applicable
3. poly	200λ	400μm	250μm
4. diffusion	20λ	100μm	60μm

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Choice of layers:-

Layer	capacitance	Resistance	comment
1. Metal	Low	Low	* Good current capability without Large voltage drop and it is used for power distributions and global.
2. silicide	Moderate	Moderate	* It has Rc product has a moderate value, long wires are applicable: this layer is useful in place of poly silicon in some cases of nmos process
3. poly silicon	Moderate	High	* It has Rc product has moderat and high IR drop
4. diffusion (Active)	High	Moderate	* Rc product is moderate and it has moderate IR drop hence it is hard to drive

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Wiring Capacitance:-

We have Area Capacitance contributed in the Calculation of overall Calculation Capacitance.

The Area capacitances are associated with the layers to substrate and from gate to channel.

We have three other Source for the Calculation of overall Capacitance.

1. Inter layer Capacitance
2. peripheral (Junction) Capacitance
3. (fringing field) fringing fields capacitance

1. Inter layer Capacitance:-

parallel plate effects are present blw one layer to another layer.

for example, for a given area metal to polysilicon capacitance is higher than metal to Substrate Capacitance.

2. peripheral Capacitance:-

The Source and drains of n-diffusion regions forms junctions with P-type substrate at uniform depth.

Similarly, P active regions may form junctions with n-well (or) n type of Substrate.

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* for diffusion regions each diode thus form has associated with peripheral capacitance which is measured in PF/unit length.

-the typical values for different -technologies given by

diffusion Capacitance	Chemical values		
	5μm	2μm	1.2μm
1. C_{Area}	1.082×10^{-4} Pf/μm²	1.25×10^{-4} pf/μm²	1.7×10^{-4} PF/μm²
2. $C_{peripheral}$	8×10^{-4} PF/μm²	negligible	negligible

3. fringing fields:-

Capacitance due to fringing field effect can be a major component of overall capacitance of inter connected wires.

frining field capacitance can be of same order of area capacitance.

The capacitance of frining field can be given as

$$C_{ff} = \epsilon_{ins} \epsilon_0 \ell \left[\frac{\pi}{\ln\left\{1 + \frac{2d}{t}\left(1 + \sqrt{\frac{t}{d}}\right)\right\}} - \frac{t}{4d} \right]$$

where ℓ = length of the wire

t = thickness of the wire

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d = Seperation b/w wire and Substrate.

* The total wire capacitance can be given as

$$C_w = C_{Area} + C_{ff}$$

Where C_{area} = Area Capacitance

C_{ff} = fringing field Capacitance

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3.2 Scaling of Mos ckts

Micro electronic technology can be characterised with the help of several indicators (or) figure of merits which includes

1. No of transistors per chip
2. minimum feature size
3. power disspiation
4. max operational frequency
5. die size
6. production cost

* many of these fig of merits can be improved by reducing dimensions of transistors, interconnections and separation blw features and by adjusting doping level and Supply voltage.

Scaling Models and Scaling factors:-

Basically we are having two Scaling models

1. Constant electric field Scaling model
2. constant voltage scaling model

In accordance with these two Scaling models we are having a special scaling model which is the Combination of both Scaling models stated above and is called as Combined voltage above and dimension Scaling model.

the following fig indicates that substrate doping level which are assosicated with Scaling of transistors.

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* To scale any parameter we are using two Scaling factors as $\frac{1}{\alpha}$ & $\frac{1}{\beta}$

* $\frac{1}{\beta}$ is used for supply voltage levels (V_{dd}) and for gate oxide thickness (t_{ox}) for all other linear dimensions we use $\frac{1}{\alpha}$ as a Scaling factor for both horizontal and vertical dimensions.

Note:- For Constant electric field Scaling model we use $\boxed{\beta = \alpha}$ and for Constant voltage scaling model $\boxed{\beta = 1}$.

Scaling factors for device parameters:-

1. Gate area (A_g):- $A_g = L \times W$

'L' is the length of the channel which is Scalled by $1/\alpha$

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and 'w' is the width of channel which is scaled by $1/\alpha$

$$A_g = L \times W$$
$$= \frac{1}{\alpha} \times \frac{1}{\alpha}$$
$$\boxed{A_g = \left(\frac{1}{\alpha^2}\right)}$$

2. Gate Capacitance per unit area (C_o' or C_{ox}):-

$$C_x = \frac{\epsilon}{D}$$

where ϵ = permitivity

D = gate oxide thickness

$$C_x = \frac{\epsilon}{D} = \frac{\epsilon_o \epsilon_{ins}}{D} = \frac{1}{1/\beta} = \beta$$

3. Gate Capacitance (C_g):- $C_g = C_o W L$

where $C_o \Rightarrow$ absolute Capacitance and It is Scaled by β.

$$C_g = C_o W L = \beta W L = \beta \left(\frac{1}{\alpha}\right)\left(\frac{1}{\alpha}\right)$$
$$= \frac{\beta}{\alpha^2}$$

4. parasite Capacitance (C_x):-

$$C_x = \frac{A_x}{d}$$

A_x = Area , d = Separation

$$C_x = \frac{1/\alpha^2}{1/\alpha} = 1/\alpha$$

5. Carrier density in the channel (Q_{ON}):-

$$C = \frac{Q}{V}$$
$$C_o V_{gs} = Q_{ON}$$

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$$Q_{ON} = \beta \cdot \frac{1}{\beta} = 1$$

6. Channel ON Resistance :-

$$R_{ON} = \frac{L}{W} = \frac{1/\alpha}{1/\alpha} = 1$$

7. gate delay (τ_d) :-

$$T_d = R_{ON} C_g$$
$$= 1 \cdot \beta/\alpha^2$$
$$= \beta/\alpha^2$$

8. Maximum operating frequency (f_o) :-

$$f_o = \frac{w}{L} \frac{\mu C_o V_{dd}}{C_g} = \frac{\beta \cdot \frac{1}{\beta}}{\beta/\alpha^2} = \frac{1}{\beta/\alpha^2}$$
$$= \frac{\alpha^2}{\beta}$$

9. Saturation Current (I_{ds}) :-

$$I_{ds} = \frac{kw}{L} \frac{[V_{gs} - V_t]^2}{2}$$
$$= 1 \left[\frac{\frac{1}{\beta} - \frac{1}{\beta}}{2}\right]^2$$
$$= 1/\beta^2$$

$$I_{ds} = \frac{C_o w \mu}{L} \frac{[V_{gs} - V_t]^2}{2}$$
$$= \beta \cdot \frac{1}{\beta^2}$$
$$= 1/\beta$$

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10. Current density (J):-

$$J = \frac{Ids}{A} = \frac{1/\beta}{1/\alpha^2}$$

$$= \alpha^2/\beta$$

11. Switching energy per gate:-

$$Eg = \frac{1}{2} C_g V_{dd}^2$$

$$= \frac{1}{2} \frac{\beta}{\alpha^2} \cdot \frac{1}{\beta^2}$$

$$= \frac{1}{2\alpha^2\beta}$$

12. power dissipation per gate:-

$$Pg = Pgs + Pgd \quad Pgs = \frac{V_{dd}^2}{R_{ON}}, \quad Pgd = Eg \cdot fo$$

$$Pgs = \frac{1/\beta^2}{1} = 1/\beta^2 \; ; \; Pgd = 1/\beta^2$$

$$Pg = 2/\beta^2 = 1/\beta^2$$

13. power dissipation per unit area (P_A):-

$$P_A = \frac{Pg}{Area} = \frac{1/\beta^2}{1/\alpha^2}$$

$$= \alpha^2/\beta^2$$

14. power Speed product:-

$$P_t = Pg\, T_d = 1/\beta^2 \cdot \beta/\alpha^2$$

$$= 1/\alpha^2\beta$$

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Scaling effects:-

S.No	parameter	Combined Voltage and dimension model	Constant electric field model $\beta = \alpha$	Constant Voltage Scaling model $\beta = 1$
1.	Supply Voltage (V_{dd})	$1/\beta$	$1/\alpha$	1
2.	Channel length (L)	$1/\alpha$	$1/\alpha$	$1/\alpha$
3.	width of the channel (W)	$1/\alpha$	$1/\alpha$	$1/\alpha$
4.	gate oxide thickness (D)	$1/\beta$	$1/\alpha$	1
5.	gate Area (A_g)	$1/\alpha^2$	$\frac{1}{\alpha^2}$	$\frac{1}{\alpha^2}$
6.	gate capacitance per unit area (C_D)	β	α	1
7.	gate capacitance (C_g)	β/α^2	$\frac{\alpha}{\alpha^2} = \frac{1}{\alpha}$	$\frac{1}{\alpha^2}$
8.	parastic Capacitance	$\frac{1}{\alpha}$	$\frac{1}{\alpha}$	$\frac{1}{\alpha}$
9.	Carrier density in the channel (Q_{ON})	1	1	1
10.	Channel ON Resistance	1	1	1
11.	gate delay	β/α^2	$1/\alpha$	$1/\alpha^2$
12.	maximum operating frequency	α^2/β	α	α^2

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13.	Saturation Current	$1/\beta$	$1/\alpha$	1
14.	Current density	α^2/β	α	α^2
15.	Switching energy per gate	$1/\alpha^2\beta$	$1/\alpha^3$	$1/\alpha^2$
16.	power disspation per gate	$1/\beta^2$	$1/\alpha^2$	1
17.	power disspation per unit area	α^2/β^2	1	α^2
18.	Power speed product	$1/\alpha^2\beta$	$1/\alpha^3$	$1/\alpha^2$

*Limitations of Scalling:-

Substrate Doping:-

So far we are discussed about various effects, we have neglected built in (junction) potential V_B which inturned depends on substrate doping level and this is acceptible so long as V_B is smaller compared to V_{DD}.

Substrate doping Scalling factors:-

As the length of the channel of a mos transistor is reduce, that depletion region width also to be scalled down to prevent d source and drain depletions regions from meeting.

The depletion width 'd' for the junction can be given as

$$d = \sqrt{\frac{2\epsilon_0\epsilon_{ins} V_B}{q N_B}}$$

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where q = charge

ϵ_0 = permitivity of free space

ϵ_{ins} = permitivity of material

V_B = V. built in potential

The inbuilt potential V_B can be given as

$$V_B = \frac{KT}{q} \ln\left[\frac{N_D N_B}{n_i^2}\right]$$

where N_D = drain (or) Source doping level

n_i = intrinsic Carrier Concentration

* If we increase N_B to reduce d, at the same time V_B is also increase.

*. For Combined voltage & dimension model the total applied voltage can be given as

$$V_a = mV_B$$

where m is a real number

then $V = V_a + V_B$

$$V_1 = mV_B + V_B$$

$$\boxed{V_1 = V_B(m+1)}$$

Now if is Scale down V_a then the voltage can be given as

$$V_a = \frac{mV_B}{\beta}$$

$$V = \frac{mV_B}{\beta} + V_B$$

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$$V = \frac{mV_B + \beta V_B}{\beta}$$

$$\boxed{V_2 = \frac{V_B(m+\beta)}{\beta}}$$

∴ The effective Scale voltage can be given as

$$V_S = \frac{V_2}{V_1}$$

$$= \frac{\frac{V_B(m+\beta)}{\beta}}{V_B(m+1)}$$

$$\boxed{V_S = \frac{(m+\beta)}{\beta(m+1)}}$$

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Limitations due to Sub threshold Currents (I_{sub}):-

one of the major Concern in the Scaling of devices is the effect of Sub threshold Current I_{sub} which can be given as

$$\boxed{I_{sub} \propto e^{\frac{(V_{gs}-V_t)}{KT/q}}}$$

when a transistor is in of off state, the value of $V_{gs}-V_t$ is negative and it should be as large as possible to minimize I_{sub}.

As the voltages are Scaled down then the ratio of $V_{gs}-V_t$ to KT/q will reduce so that Sub threshold increase.

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* For this reason, it may be desriable to scale both v_{gs} & V_t by a factor $1/b > 1/a$. Since 'a' is generally greater than 'b'.

* The maximum electric field across the depletion region can be given as

$$E_{max} = \frac{2V}{d} = \frac{2(V_a - V_b)}{d}$$

* The junction breakdown voltage can be given as

$$BV = \frac{\varepsilon_0 \varepsilon_{ins} E^2}{2qN_B}$$

Note:- Extra care is therefore require in estimating the breakdown voltages for scalled devices.

* The Electric field are greater and breakdown voltage is greater at the corcern of diffusion regions underlying SiO_2.

Limitations on logic levels and Supply voltages due to Noise :-

The major advantages in Scalling of devices are Smaller gate delay time ie, higher operating frequency and Lower internal power Consumption.

* The lowering of interface Spacing and higher Switching increase noise in VLSI chips. so noise may also be amplified and is thus a major concern.

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* The mean square current fluxations in the channel can be given as

$$\overline{i^2} = 4kT\, R_n g_m \Delta f \longrightarrow (1)$$

where R_n = Noise Resistance

Δf = Band width

$g_m = \beta V_p$

V_p = pinch off Voltage

The equivalent Resistance R_n can be given as

$$R_n = \frac{\left(\frac{1}{2}\frac{V_g'}{V_p'} + \frac{1}{6}\right)}{g_m} \longrightarrow (2)$$

where $V_g' = V_{gs} - V_t + V_B$

$V_p' = V_p + V_B$

Similarly the thermal equivalent '$R_n g_m$' can be given as

$$R_n g_m = \frac{1}{2}\frac{(V_{gs} - V_t + V_B)}{(V_p + V_B)} + \frac{1}{6} \longrightarrow (3)$$

Observing eqn(3) the value '$R_n g_m$' is also dependent on V_g but very small extent. for the modified expression for $R_n g_m$ when t_{ox} is scaled as

$$\left(R_n g_m\right)_{t_{ox}} = \frac{1}{2}\left[\frac{V_g}{V_g - \frac{1}{2}\left(\frac{a}{C_{ox}}\right)^2\left(1 + \frac{V_g' C_{ox}}{a}\right)^{1/2} - 1}\right] + \frac{1}{6}$$

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* If their is an increase in the value of C_{ox} then R_{ngm} decreases by a small amount which inturn decrease the ratio of logic levels to thermal noise by same Amount.

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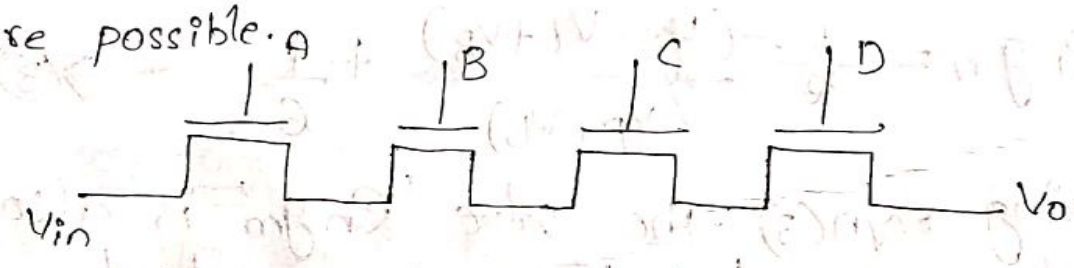
Switch logic:-

Switch logic is based on pass transistors (or) on the transmission gates.

* this approach is fast for small arrays and takes no static current from supply rails.
* Hence power dissipation such arrays is small.

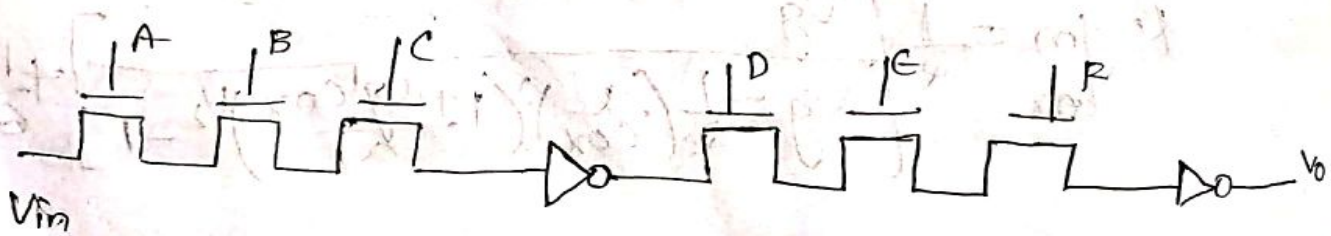
∴ Current flow only on Switching.

* pass transistor logic is similar to logic arrays based on relayed contacts.
* The basic AND connections are set out as shown in fig below but many combinations of switches are possible.



$V_o = V_{in}$ when ABCD = 1

Here Vo logic levels will be degraded by Vt effects.



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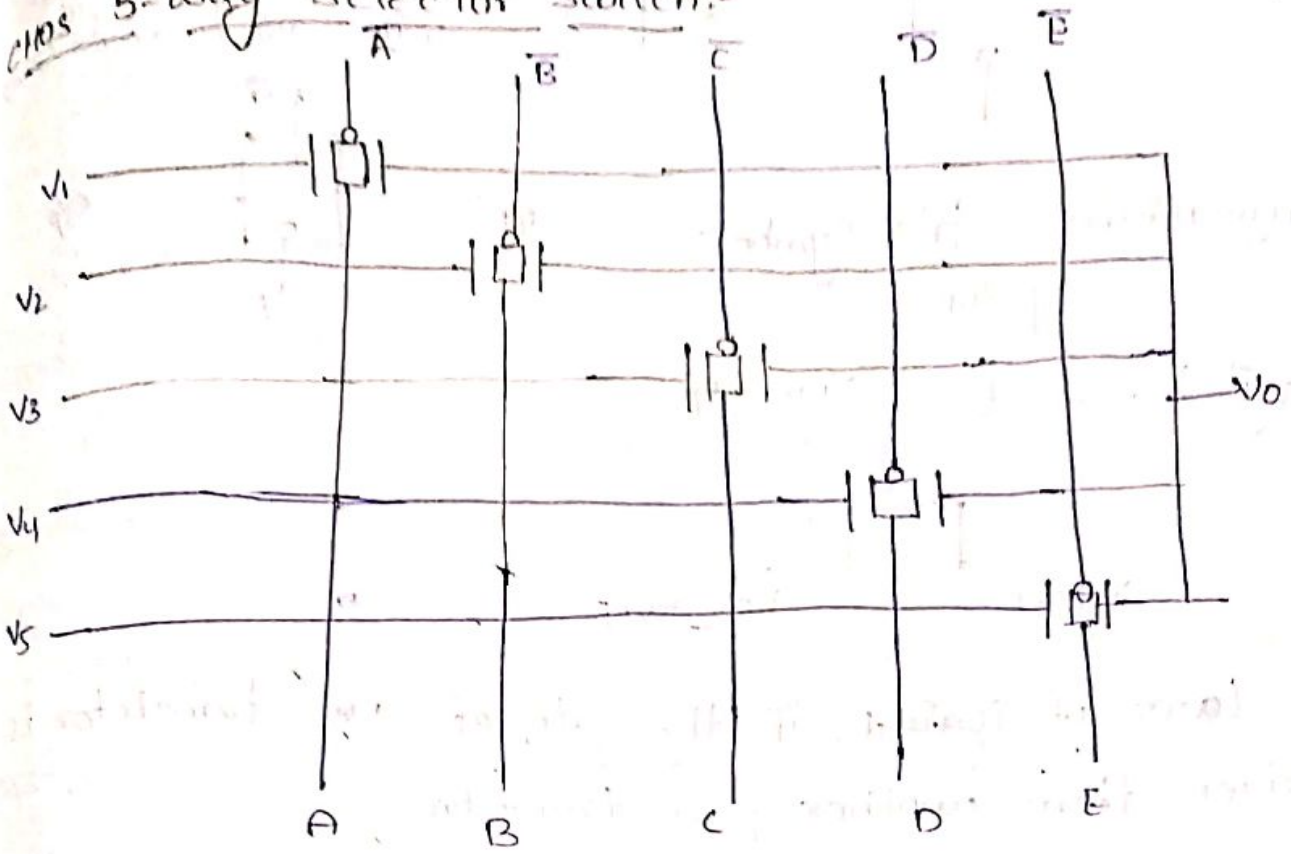
V_o = V_{in} when ABCDEF = 1

CMOS 5-way Selector Switch:-

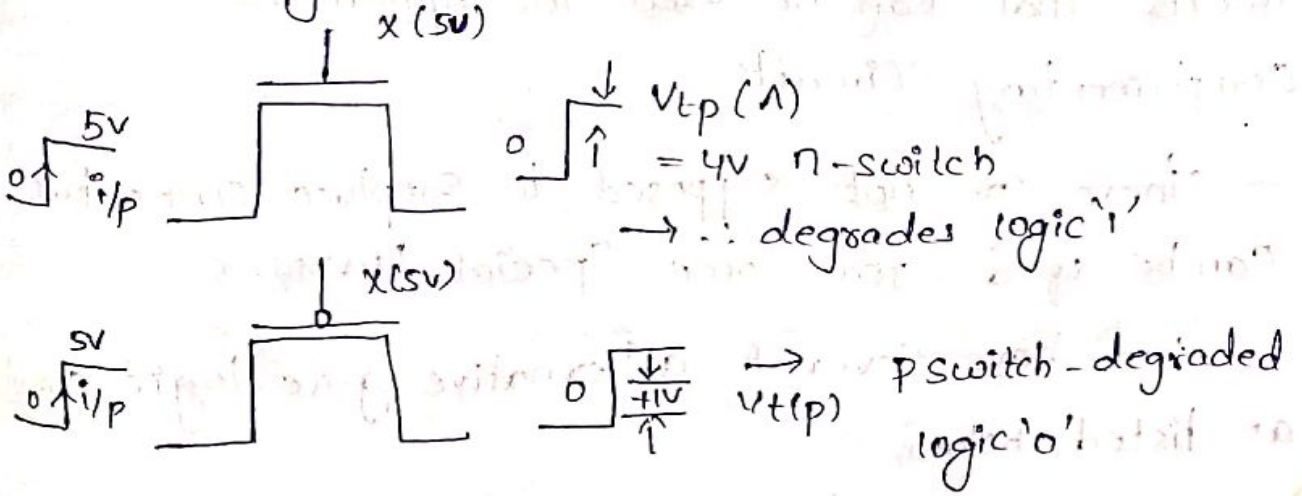


$$V_o = V_1A + V_2B + V_3C + V_4D + V_5E$$

Assuming A, B, C, D, E are mutually exclusive i.e., Vout logic levels are not degraded by 'V_t' effect.

Pass transistor and Transmission gates:-

Switches and switch logics may be form from simple 'n' (or) p-type pass transistors in parallel as shown in figure below.



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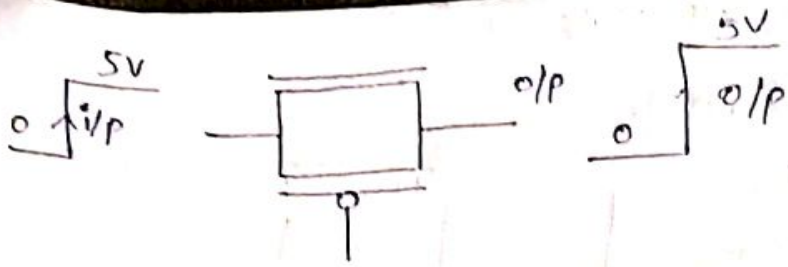
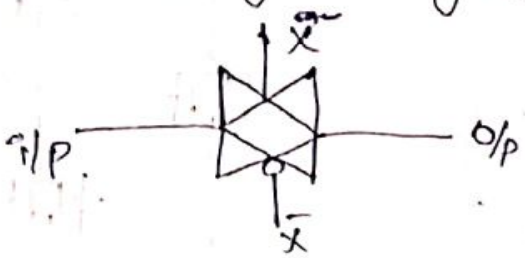
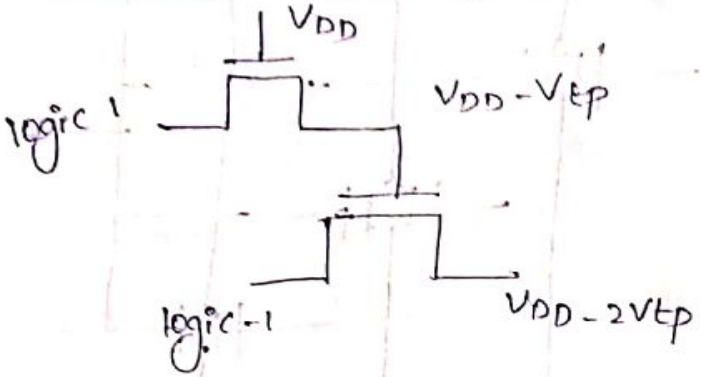


→ Transmission gate with good logic levels



Transmission gate symbol:-



Laws of logic-1, if the gate of pass transistor is driven from another pass transistor.

fig:- Some properties of pass transistor and some logic families.

Alternative Gate Circuits (or) Gate logic:-

CMOS circuits suffer from increased area and Corresponding increasing capacitance and delays logic gates becomes more complicate.

For this Reason, the designers develops the circuits that can be used to suppliment the complimentary circuits.

There are not supposed to replace cmos but can be used for some Special purposes.

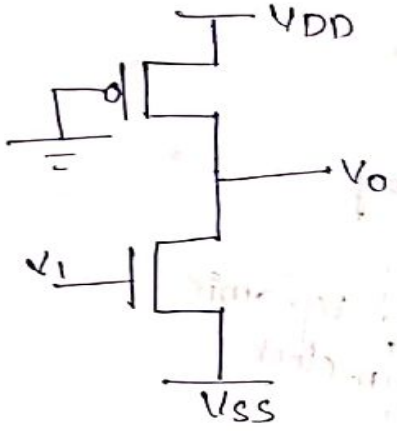
We have several alternative gate logic circuits as listed below,

(1) pseudo nmos
(2) Dynamic
(3) C^2mos (clocked cmos)
(4) Domino logic
(5) np cmos logic

pseudo nmos logic:-

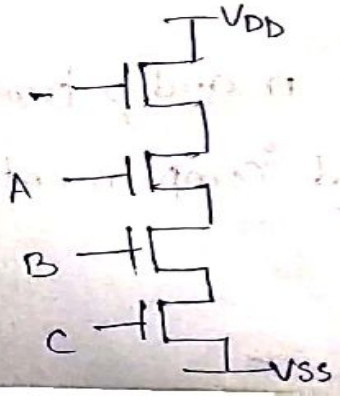
The pseudo nmos logic is one of the type of alternative gate circuits ie., use to supliment for mos circuits.

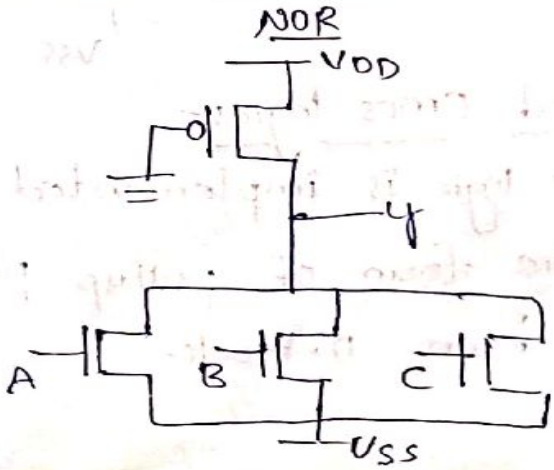
In this pseudo nmos circuit the depletion mode pull up mos transistor is replaced with p-mos transistor whose gate terminal is always ground.



Implementation of 3 Input NAND gate & NOR gates

Implementation of three i/p NOR gate and Nand gate using pseudo nmos logic:-





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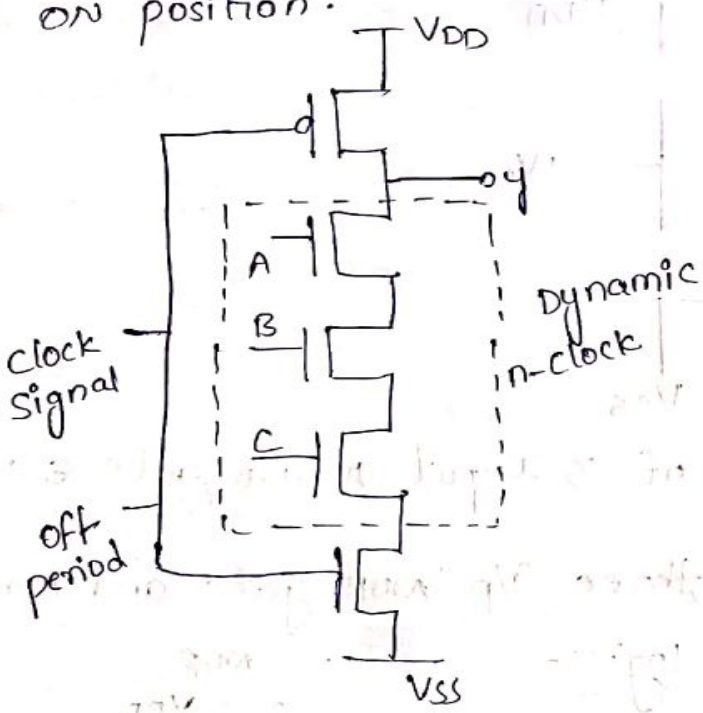
Note:- For 'n' numbers of i/p Pseudo nmos logic requires 'n+1' numbers of transistors cmos logic require '2n' number of transistor.

Dynamic cmos logic:-

The actual logic is implemented in the n-block an P transistor is used for non-time critical pre-chargi outputt.

i.e the output capacitance is charged to VDD during off period of clock signal (ϕ).

During this time, inputs due applied to n-block and state of logic is then evaluated during on period of clock ... when the bottom n-transistor is in ON position.



Clocked cmos logic:-

The logic is implemented in both n and p transistors in the form of pullup p-block and complimentary pull down n-block.

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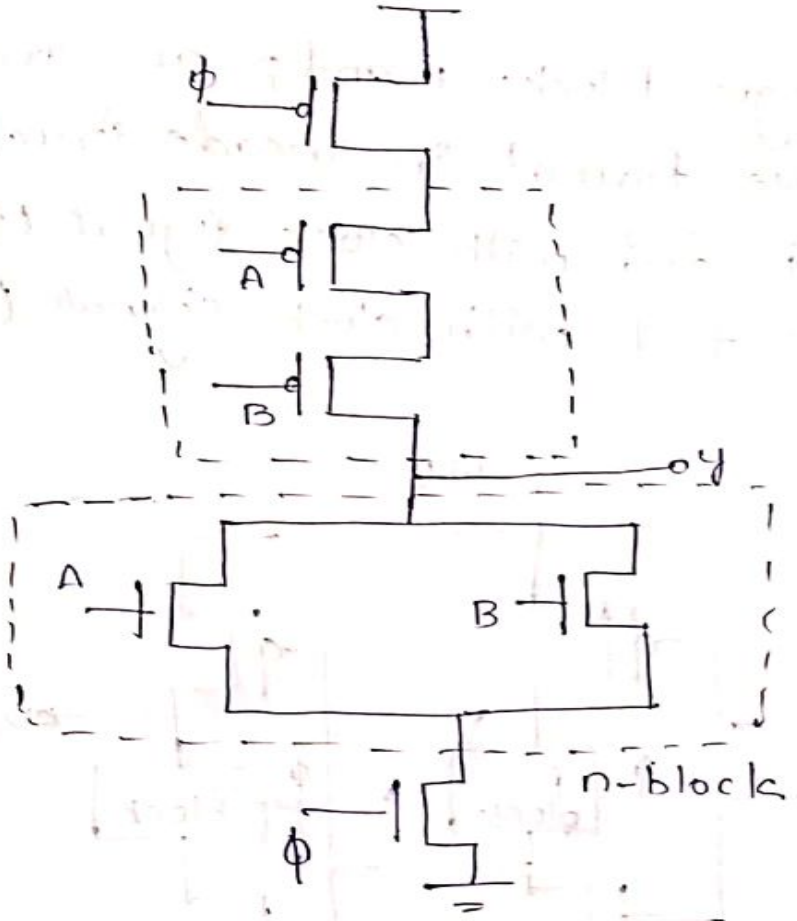
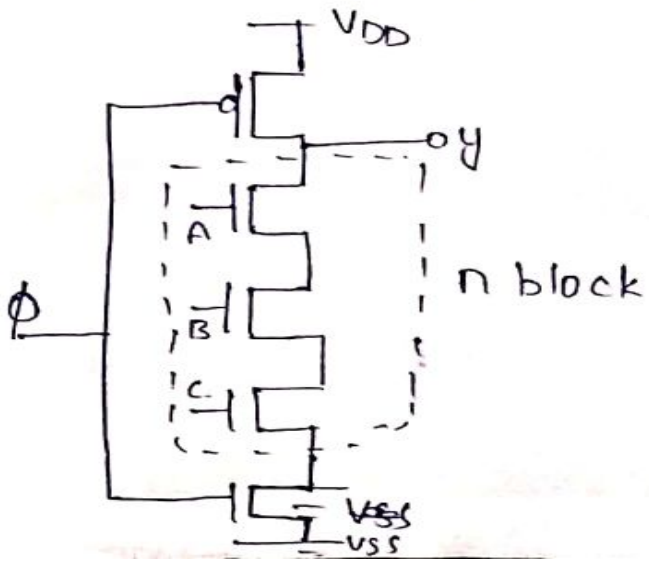
the logic in this can is evaluated only during the ON period of clock.



Domino cmos logic:-

An extension of dynamic cmos logic is called domino cmos logic. this is an modified arrangement that allows cascading of logic structures using only a single phase clock. So, at the output we use a buffer.



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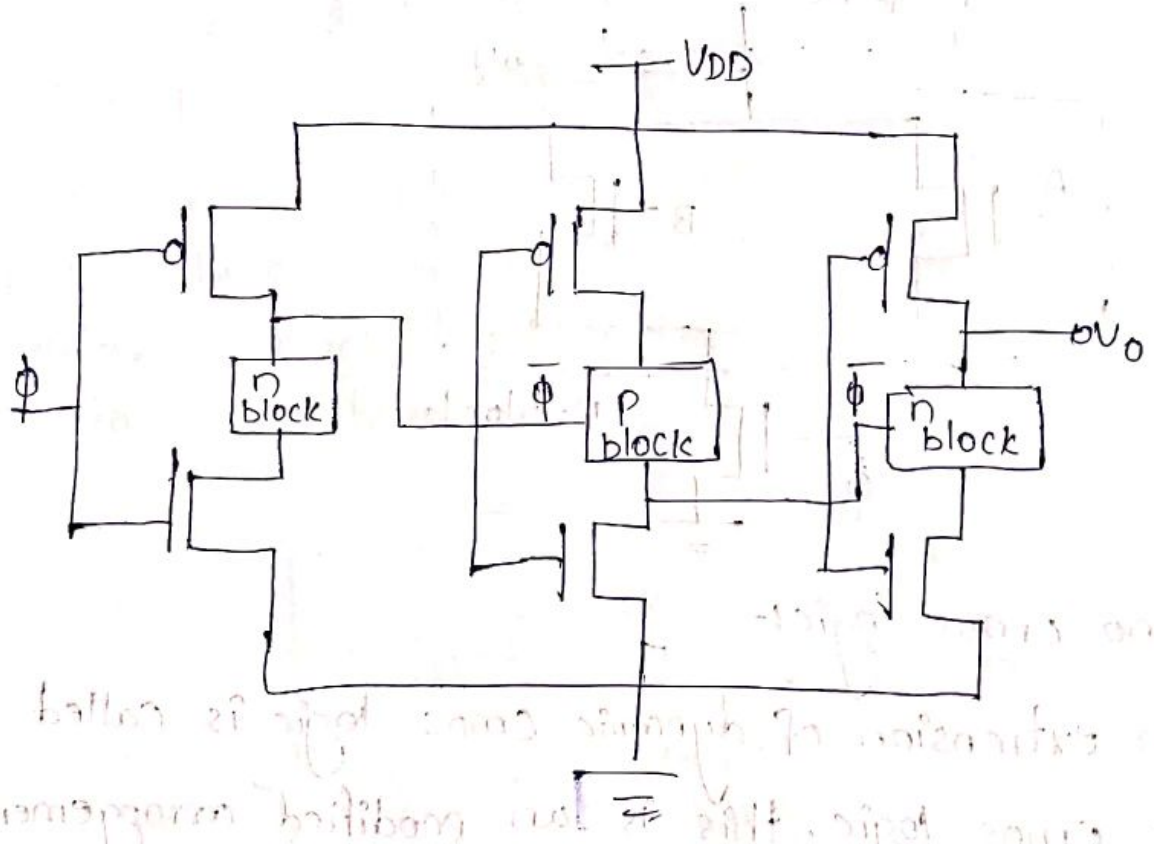
n p cmos logic:

This is another version of basic dynamic logic circuit.

The actual logic blocks n and p are arranged in the alternative format in cascade structure.

One block is fed with clock signal (ϕ) and another block is fed with clock signal ($\bar{\phi}_1$).



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