UNIT - 1

Introduction & Basic Electrical properties of MOS ckts:-

VLSI - very large Scale integration

Definition of Ic:-

Ic is an electronic for integrated circuit and may be given as combination of active of passive. elements that are integrated on signle silicon chip.

As there are several advantages of using Silicon which includes, if acts as good insulating material, oxiding material.

Most of the Ic's avaliable in the market are made using silicon only [i.e., 90 %]

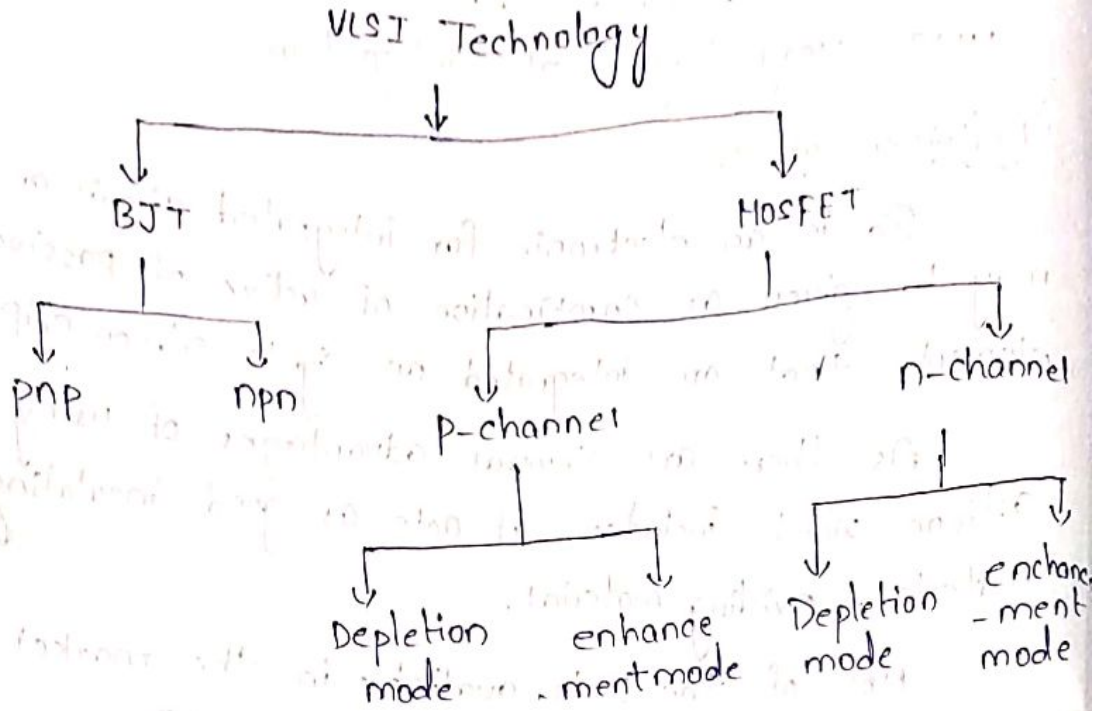
Trends in micro electronics:-

The electronics now a days available in the market are categorized by reliability, size, weight, volume, cost.

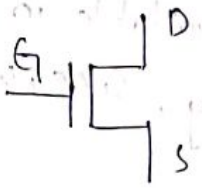
In addition these the VLSI technology made an aduantage to have a more powerful & flexible processor for availing a good source.

* The BJT was first invented by william shockley & John barden in 1947 at bell laboratories.
* up to 1950's the BJT technology was dominated by vaccum tubes.
* The 1st Ic technology was deveioped in 1960's and there by a revolutionary come into the electronics industries.

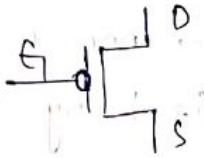
Symbols of MOSFET:-



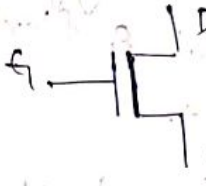
N-MOS

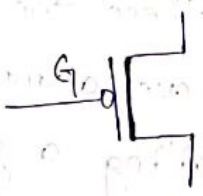


P MOS

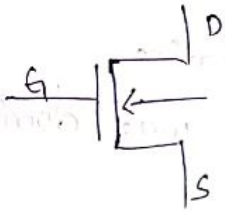


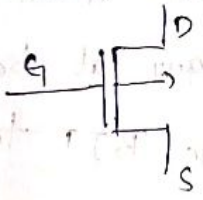
enhancement mode





Depletion mode





Current Supply

BJT is a Current Controlled device where as MOSFET is a Voltage Controlled device.

Levels of integration:-

Depending upon the complexity of integrated ckt the classification can be given as

SSI (small scale integration) - 10 to 100

MSI (Medium scale integration) - 100 to 1000

LSI (large scale integration) - 1000 to 10^5

VLSI (very large scale integration) - 10^5 to 10^6

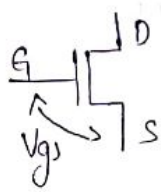
the upcoming technology i.e.,

ULSI (ultra large scale integration) - 10 to 100 million

Difference Between BJT and MOSFET

BJT	MOSFET
1. It is current control device.	1. It is voltage control device.
2. Collector and emitter terminal's are not inter change.	2. Drain and Source terminals are interchange.
3. Impedance is low.	3. Impedance is high.
4. Ip Impedance is low	4. Ip Impedance is high
5. Trans conductance is high.	5. Transconductance is low

* Why it is called FET?

A) 

Vgs = Voltage blw gate and source terminals.

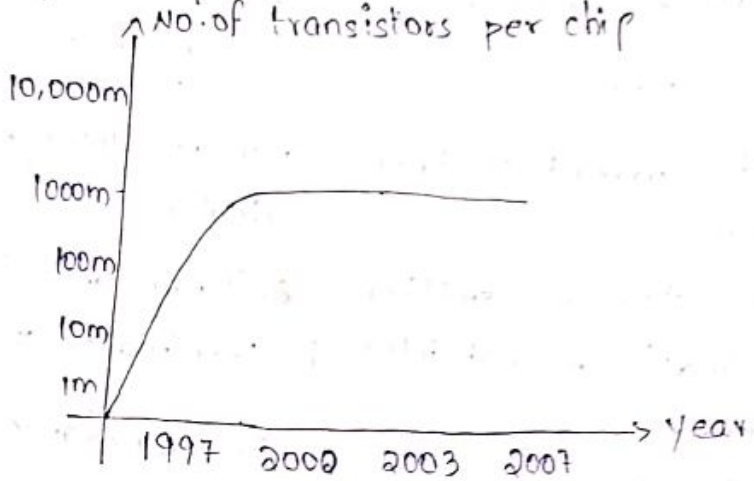
By the external application of vgs they is an electric field development blw gate and source

V1

and hence it will get effected in corresponds with V_{GS}. Hence it is called field effect Transistor (FET).

The IC Era:-

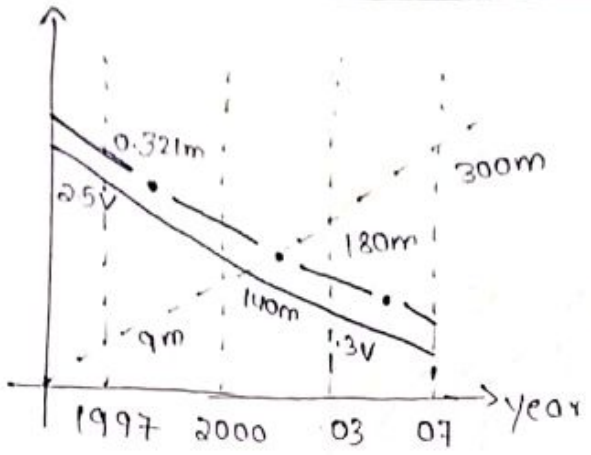
* The first IC emerged in the early 1960's.
* Depending upon the potential of that IC, we can find no. of transistors that are being integrated in the single silicon chip.
* In less than 3 decades the no of transistors count has rasin form 100 to 1000 millions of transistors per chip.



Moore's law:-

The graphical representation that gives the relation-ship b/w the year. V/s no. of transistor per chip is called moora's law.

No of transistors per chip	supply voltage	channel length (um)
10000m	3v	0.3
1000m	2.5v	0.25
100m	2v	0.2
10m	1.5v	0.15
1m	1V	1



Channel length (μm) — • — • — • —

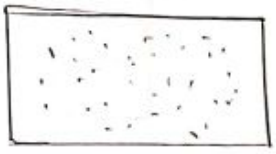
Supply voltage ————————————

No. of transistors per chip - - - - - - - - - - - - - -

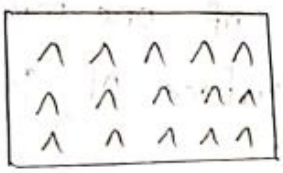
To have powerful and flexible processors, some more modifications are made to moore's law which includes reducing supply voltage and channel length.

Symbol's for Ic fabrication process:-

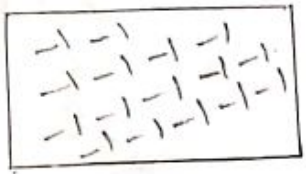
oxide layer →



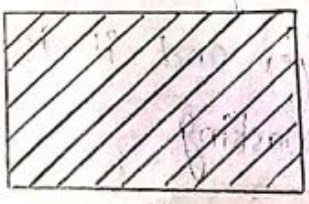
P-Subtrate →



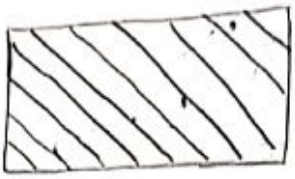
N-Subtrate →



P- diffusions →



n-diffusions 

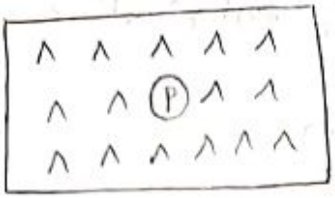
polysilicon 

metal 

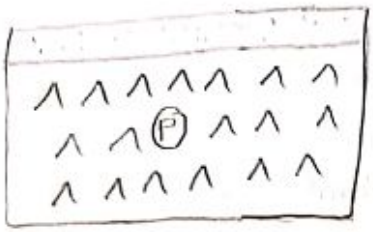
depletion 

N-MOS fabrication process:-

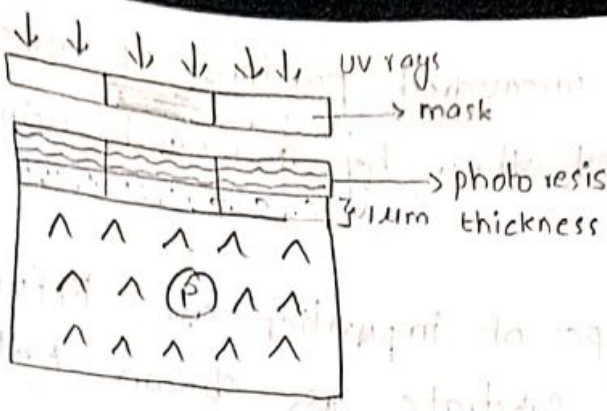
Step 1:- for the desiging of n-mos transistor we have to Consider P type of substrate material.



Step 2:- To improve the quality and protection an oxide layer of one micrometer thickness is grown over all surface of p-substrate.

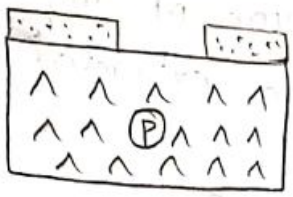


Step 3: A photo resistive layer is grown at the top of oxide layer and it is exposed to uv light through suitable masking.

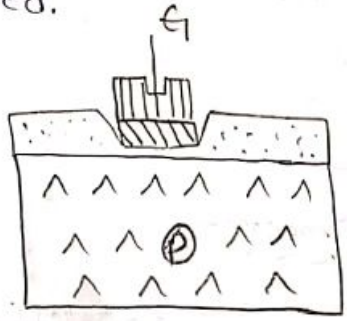


Step 4:- The uncovered portion of mask allows UV light to flow through it, the oxide layer will be get softened and remain covered position will be remain harden.

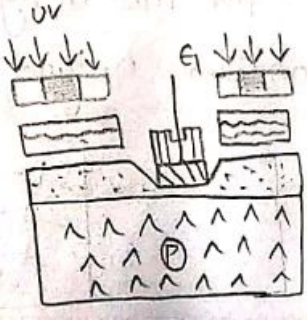
The portion which is softned will be remove and the process is called "Etching".



Step 5:- An oxide layer of 0.1μm thickness is grown and using polysilicon and metal gate terminal can be extracted.

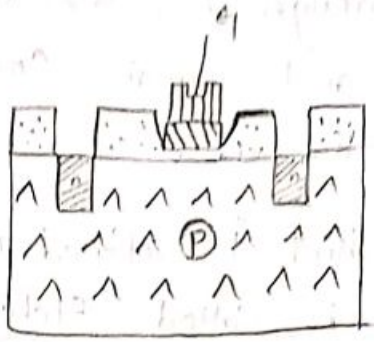


Step 6:- To diffuse n-type of impurities into p-type of substrate the masking and Etching processes are again carried out

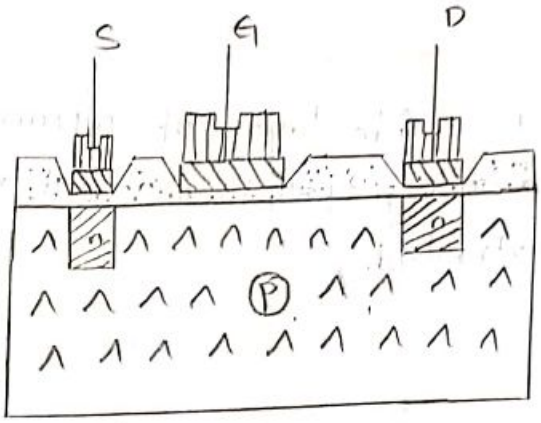


Step 7:- The uncovered portions of mask will be get softend and their by removed using Etching process.

The n-type of impurities are diffused into the P-type of substrate as shown below.



Step 8:- From the n-type of impurities drain and Source terminals can be extracted using polysilicon and metals.

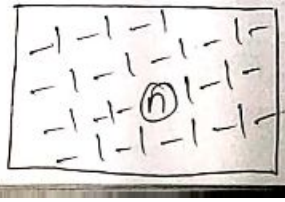


9) P-MOS fabrication Process:-

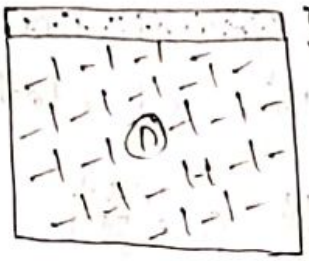
P-(N)-P P-diffusion

Substrate

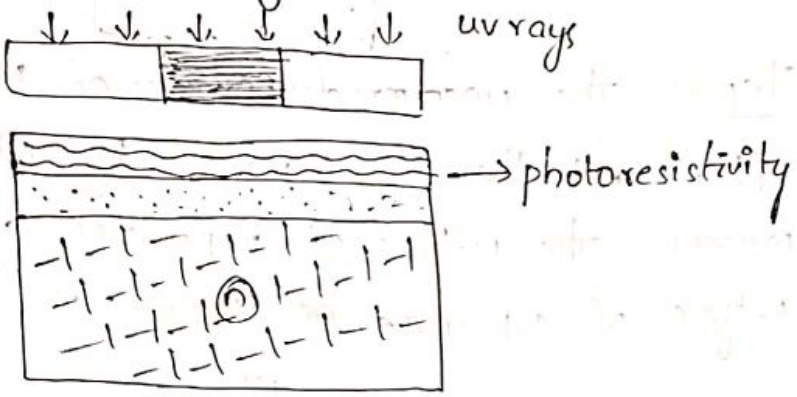
Step 1:- for the designing of P-MOS transistor we have to consider n-type of substrate material.



step 2:- To improve the quality and protection on oxide layer of 1um thickness is grown overall surface of n- substrate.

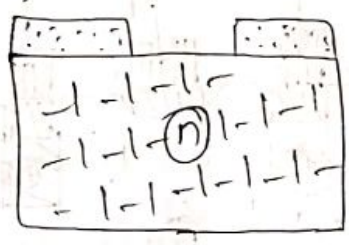


step 3:- A photoresistive layer is grown at the top of oxide layer and it is exposed to uv light through suitable Masking.

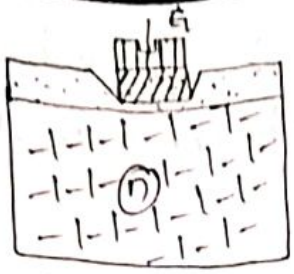


step 4:- The uncovered position of mask allows uv light to flow through it. the oxide layer will get soften and remain covered portion will remain harden.

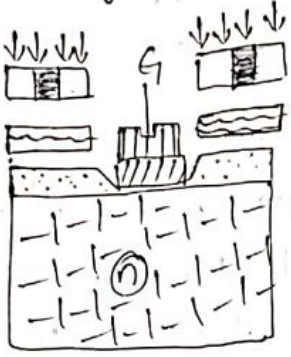
the portion which is soften will be removed and this process is called Etching.



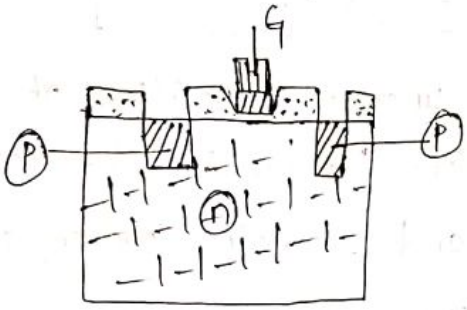
step 5:- An oxide layer of 0.1um thickness is grown and using polysilicon and metal gate terminal can be exerted.



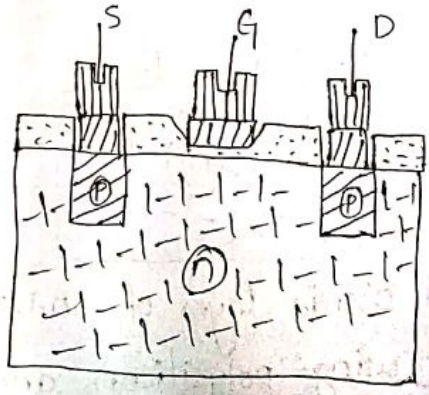
Step 6:- To diffuse p-type of impurities into n-type of substrate the Masking and etching process are again carried out.



Step 7:- The uncovered portion of Mask will be get soften and there by removed by using "Etching" process. the n-type of impurities are diffused into P-type of substrate as shown in below.



Step 8:- from the p-type of impurities drain and source terminals can be extracted by using polysilicon and metals.



CMOS Inverter:-

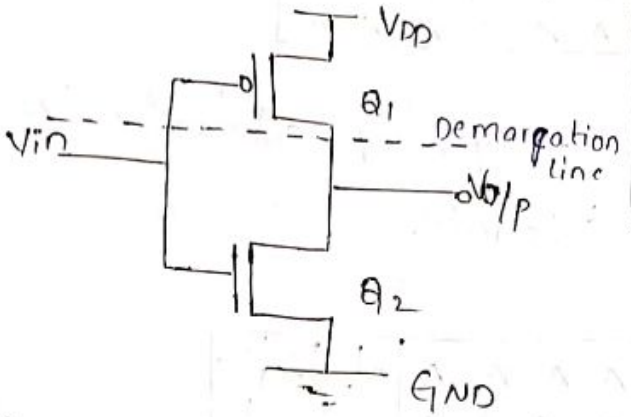
* CMOS is known as complementary metaloxide semi-conductor and it will produce output has complemen-tation of input.

* the CMOS can be designed with the help of PMOS and NMOS.

* NMOS transistors are faster than pmos devices because the Mobility of electrons are greater compare to Mobility of holes.

i.e., $\mu_n = 2.5\mu_p$

CMOS Inverter circuit:-



Vin	Q1	Q2	Vo/p
0	ON	OFF	1
1	OFF	ON	0

Operation:-

Case(1):- when Vin is zero

when the input is logic 0 then the transistor Q_1 will get ON, Q_2 will get off there by producing Vo as logic '1'.

Case(2):- when Vin is logic '1'.

when the Input is logic 1 then Q_1 will get turn off, Q_2 will get turn on, hence the Vo as logic '0'.

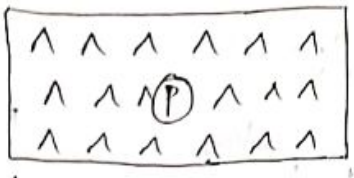
fabrication of CMOS:-

for the fabrication of CMOS we have different types

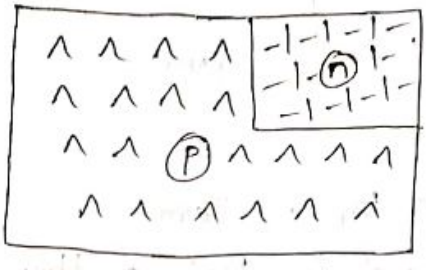
1. CMOS using p-well process
2. CMOS using N-well process
3. Twin-Tub process

CMOS fabrication using N-well process:-

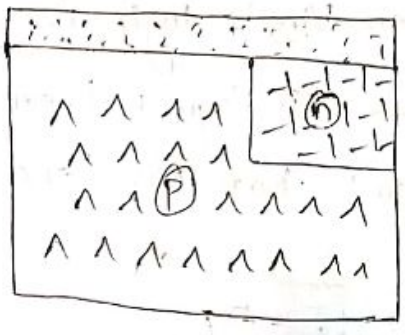
Step 1:- for the designing of CMOS using N-well process we have to consider a p-type of substrate.



Step 2:- Diffuse N-type of substrate (N-well) into p-type of substrate.

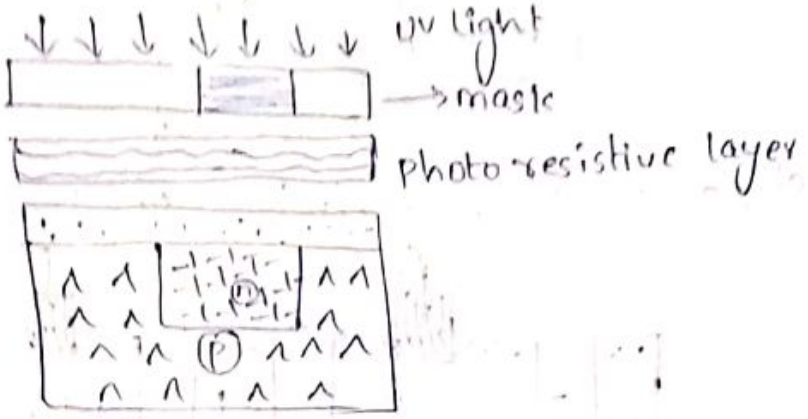


Step 3:- grow oxide layer on the surface of p-type substrate of 1um thickness

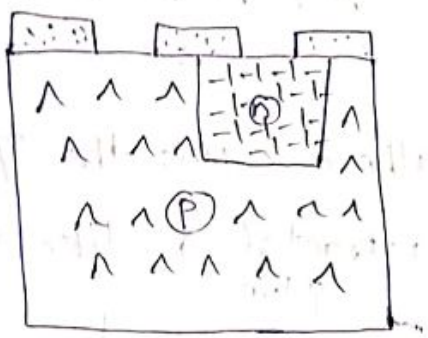


} 1um thiox

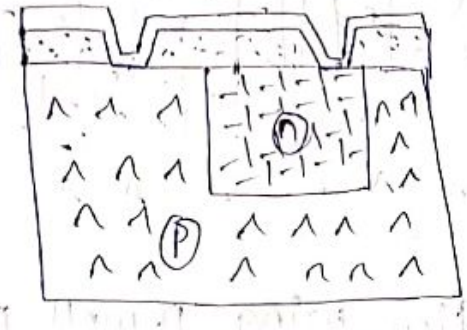
Step 4:- To improve photoelectiveness, a photoresistive layer is grown and it is exposed to uv light through suitable Masking.



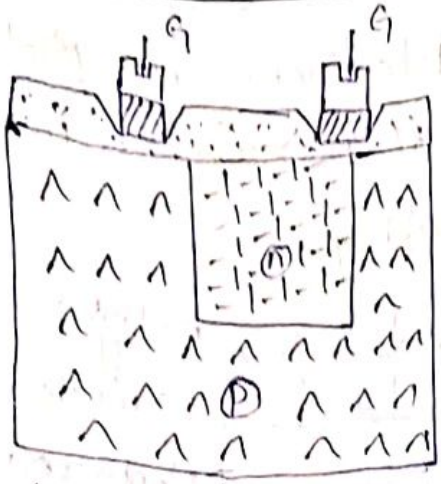
Step 5:- The uncovered portions of mass will get soften and removed by etching process.



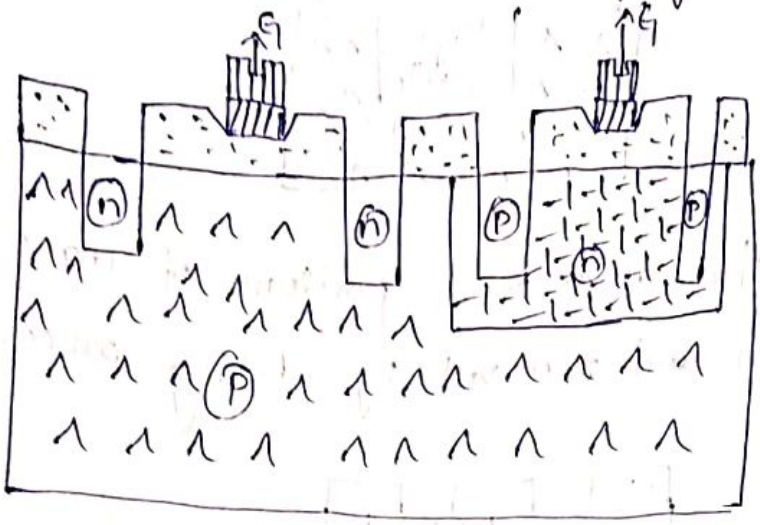
Step 6:- An oxide of 0.1 layer is grown on the top of p-type of Substrate.



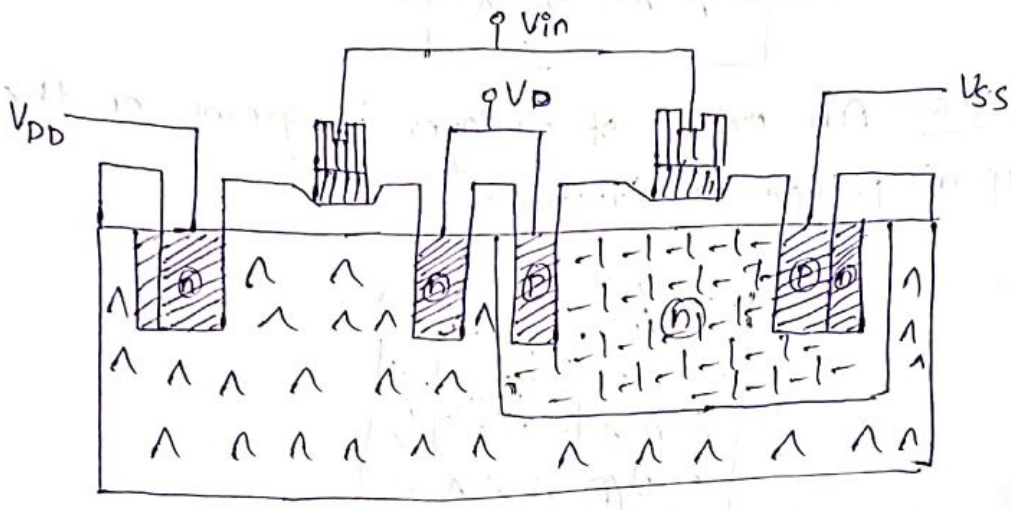
Step 7:- The gate terminals can be extracted from p and n type of substrates using polysilicon and metal.



Step8:- To have diffusions of n-type and p-ty

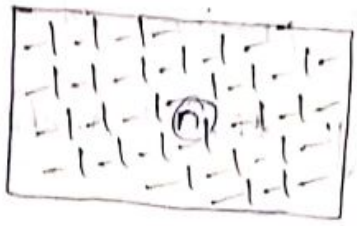


Step9: finally Furthere C-MOS the i/p and o/p terminals can be extracted as like shown below.

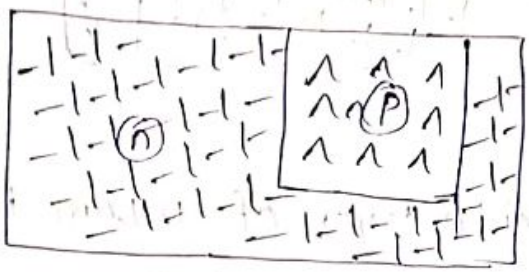


2) C-MOS fabrication using P-well process:-

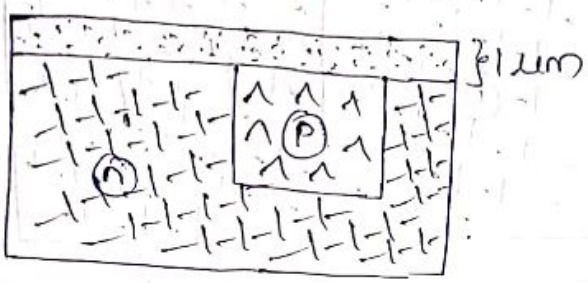
Step 1: For the designing of C-MOS using P-well process we have to Consider a n-type substrate.



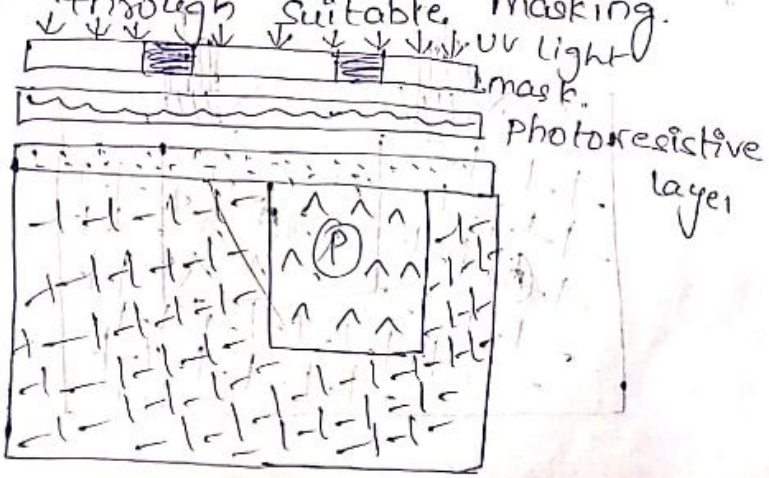
Step2:- diffuse p-type substrate (p-well) into n-type of substrate.



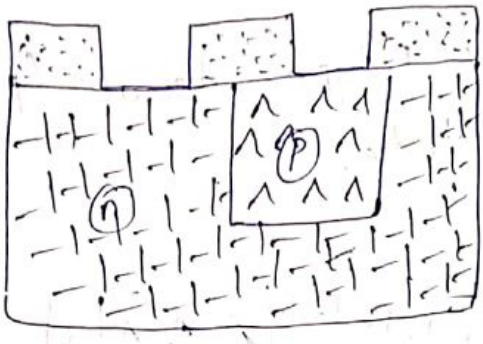
Step 3:- grow oxide layer on the surface of P-type of substrate of 1um thickness.



Step4:- To improve the protectiveness a photo resistive layer is grown and it is exposed to uvlight through suitable masking.

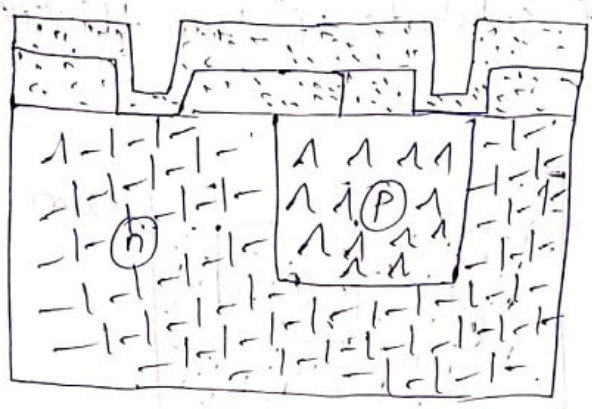


Step 5: The uncovered portions of mask will get soften and removing the "etching" process.

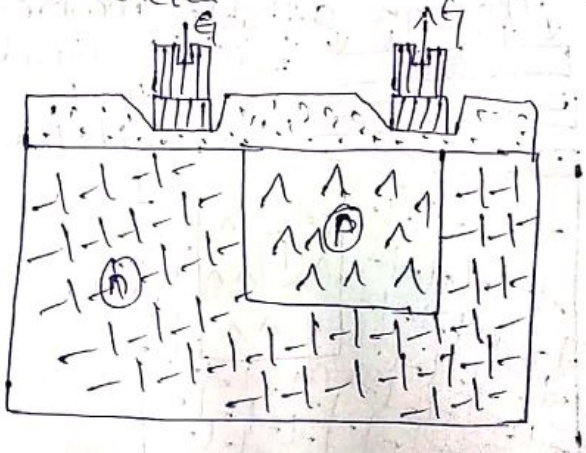


Step 6:-

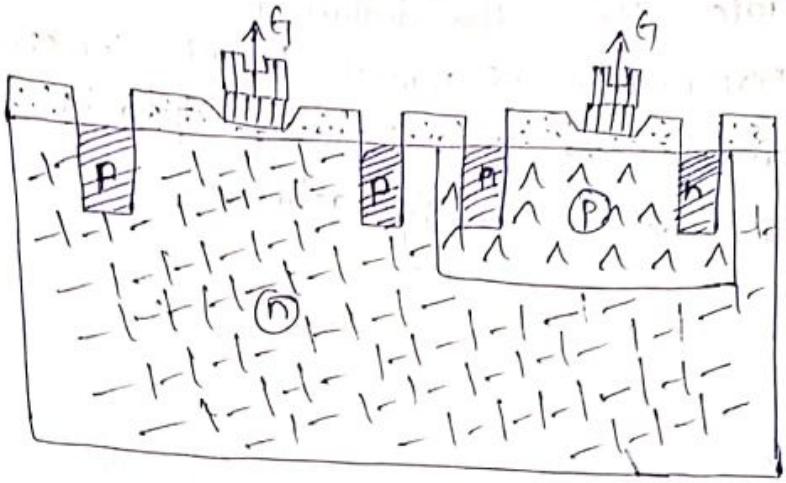
An oxide layer of 0.1um is grown on the top of P-type substrate.



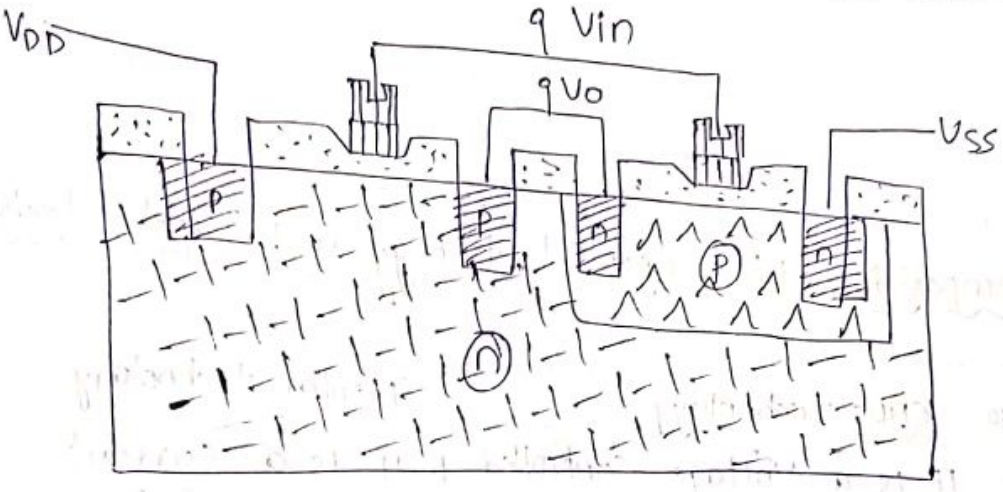
Step 7:- The gate terminal can be extracted from P and n-type of the substrate using polysilicon metal



Step8:- To have diffusion p-type and n-type into corresponding n & p type of substrates Repeat the steps from (4) to (6).

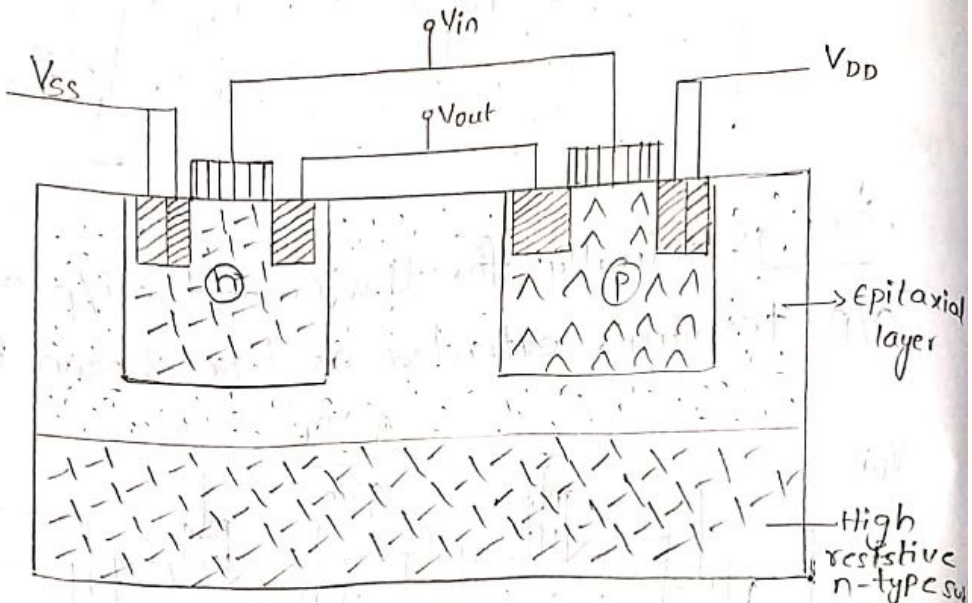


Step 9: finally for the cmos the i/p and o/p terminals extracted as like shown below.



CMOS fabrication using Twin-Tub process:-

CMOS using twin-tub process is the logical extension of P-well and N-well process. the desiging can be carrier out by taking a high resistitive n-type of Substrate. Here the design is consider such that the performance of P-well do not comprise the Performance of N-well using Epitaxial layer. Hence doping level is readily acheieve.



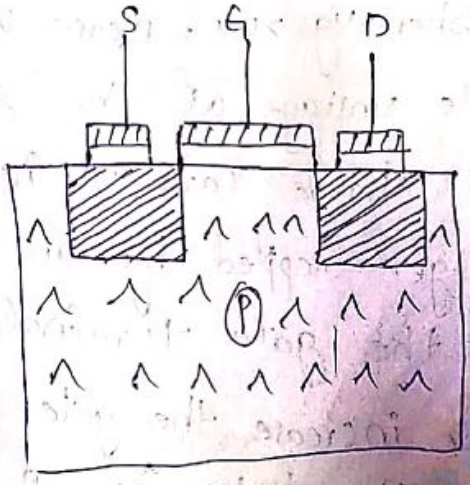
Comparision blw CMOS technology and Bipolar technology

S.No	CMOS technology	Bipolar technology
1.	It is a Voltage controlled device.	1. It is a current controlled device.
2.	High input impedance and low output drain current	Low input impedance and high output drain current.
3.	Low static power dissipation	High static power dissipation
4.	Scable threshold voltage	threshold voltage may depend on type of Semiconducting material & on device parameters.

5.	Bidirectional Capability that is drain and source terminals can be inter change.	These are essentially uni -directional,
6.	low transconductance. i.e., g_m is directly proportional to 1/impedance $g_m \propto \frac{1}{\text{Impedance}}$.	High transconductance that is $g_m \propto eV_{in}$
7.	High package density	low package density.
8.	High noise margin	low voltage swing levels

Enhancement mode MOSFET:- [nmos]

While desinging N-MOS we have to take p-type of substrate and it has two n-type of diffusions to form drain and source terminals for extracting gate, drain and source terminals polysillicon and metal contacts are use for necessary leads. Here we have to apply a suitable positive voltage at the gate terminal to create channel blw drain and source



Operation of NMOS:-

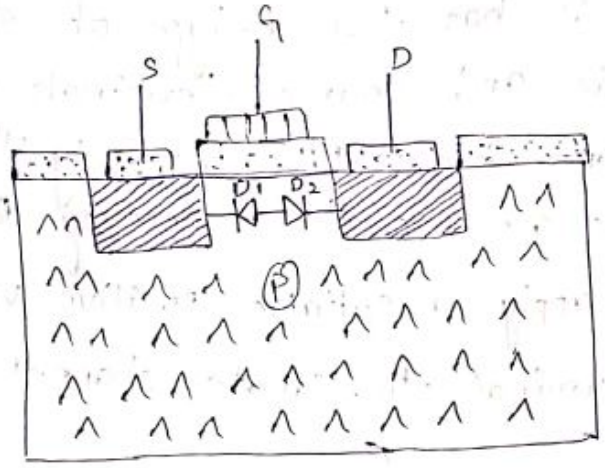
The designing of N-mos includes Considering a P-type of substrate and to heavily doped n+ impurities are diffuse into p-type of substrate to get drain and Source terminals.

Case (1):-

When $V_{gs}=0V$

When $V_{gs}=0V$ no channel will be form and no current condition takes place.

* Here when $V_{gs}=0$ we can find two junction diodes that are connected in series back to back manner in b/w drain and source and these two diodes are in reverse bias condition.



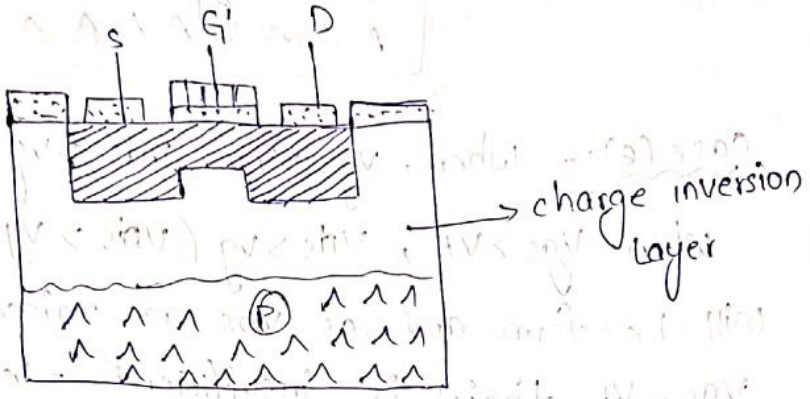
Case (2):- when $V_{gs}>0V$, means we are applying Some possible voltage at the gate terminal then the majority charge carriers in N-mos that is holes will get repelled by an amount of voltage applied at the gate terminal.

* If We increase the gate potential step by step then the holes in the substrate will get

rippled and pushed down leaves a depletion region b/w drain and source. Hence it is called charge inversion layer.

* After having a charge inversion layer the holes in the gate terminal will get attracted to n+ diffusions present in drain and source terminals, thereby forming N-channel b/w drain and source.

** Note:- The voltage at which charge inversion layer forms and the gate terminal can be inverted is called threshold voltage of mass device.



Case(3):- when $V_{gs} < V_t$, $V_{DS} = 0$

No channel will be form and hence no current conduction takes place i.e., $I_{DS} = 0$

Case(4):- $V_{gs} > V_t$, $V_{DS} = 0$

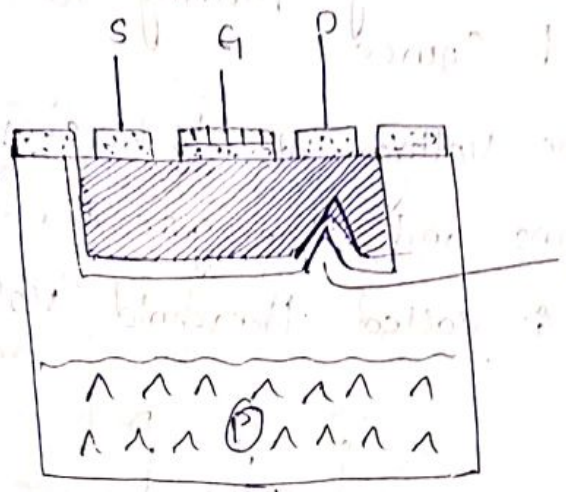
when $V_{gs} > V_t$ then channel will be form but no current conduction takes place i.e., cutoff region.

Active region → current conduction takes place

Saturation Region → Acts as Constant Current source

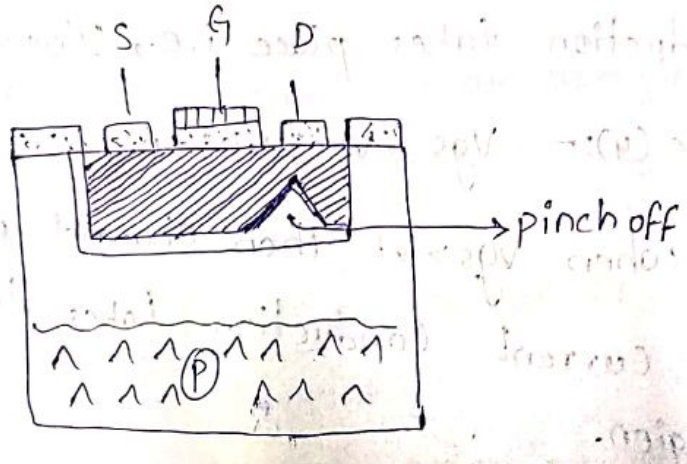
Case(5):- when $V_{gs} > V_t$, $V_{ds} \leq V_g$

When $V_{gs} > V_t$ channel will be form, when $V_{DS} = V_g$ ($V_{DS} = V_{gs} - V_t$) then near drain terminal their is an insufficient electric field and it is in non-saturation condition.



Case(6):- when $V_{gs} > V_t$, $V_{ds} \geq V_g$

When $V_{gs} > V_t$, $V_{DS} > V_g$ ($V_{ds} > V_{gs} - V_t$) then channel will be form and as V_{DS} as raised greater than $V_{gs} - V_t$ their is insufficient electric field near the drain terminal which causes the channel pinch off



Here when $V_{gs} > V_t$, $V_{ds} > V_{gs} - V_t$ it is in saturation mode and hence acts as constant current source.

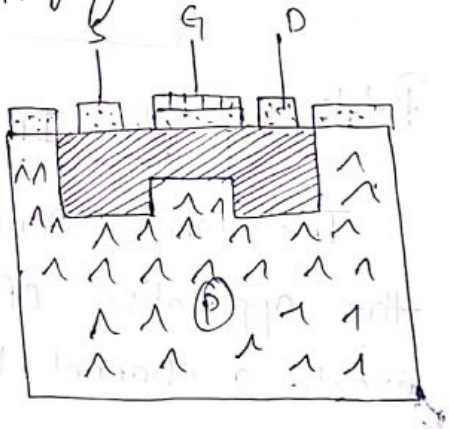
Note:- for an enhancement mode n-mos the channel will be created by applying a suitable positive voltage at the gate terminal.

* If it is p-MOS, to create channel we need to apply negative voltage at the gate terminal.

Depletion Mode N-MOS:-

In Depletion mode MOSFET it is having an inbuilt channel that is no need to apply external voltage.

In this depletion mode n-mos the channel will be created blw drain and source prior to Manufactoring stage before applying insulating and metals.

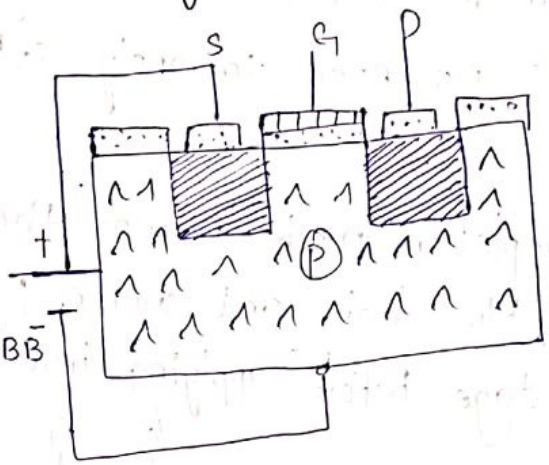


Body Mass effect:-

Note:- Depletion mode N-mos is always ON. If you want to remove channel, we need to apply the Negative voltage at the gate terminal.

Body Mass Effect:-

-for N-mos, basically the source voltage and Body potential should be equal that is $V_S = V_B = 0$. If $V_B \neq 0$ i.e., it is having some inbuilt possible potential than it causes an effect on threshold voltage. hence threshold voltage level is increased. to avoid this the body is connected to suitable negative voltage w.r.to source hence this effect is called Body Mass effect.



Relationship b/w I_{ds} Vs V_{ds} :-

The whole concept of mass transistor revolves the application of V_{gs} which in turn causes to create a channel b/w drain and source.

∴ The current I_{ds} is a dependent on both V_{gs} and V_{ds}.

The current I_{ds} can be given by

$$I_{ds} = -I_{sd}$$

$$\therefore I_{ds} = \frac{Q_c}{\tilde{T}_{ds}} \longrightarrow (1)$$

where Q_c is charge and

$\tilde{T}_{ds}$ is electron transit time

we know that $\tilde{T}_{ds} = \frac{L}{v} \longrightarrow (2)$

where L = length of the channel and

v = velocity

The velocity 'v' can be given as

$$v = \mu E_{ds} \longrightarrow (3)$$

where μ is called mobility constant

E_{ds} = Effective electric field b/w drain and source.

$$E_{ds} = \frac{V_{ds}}{L} \longrightarrow (4)$$

Sub (4) in (3)

$$v = \mu E_{ds}$$

$$V = \mu \frac{V_{ds}}{L} \longrightarrow (5)$$

Sub (5) in (2)

$$\tilde{T}_{ds} = \frac{L}{v}$$

$$\tilde{T}_{ds} = \frac{L}{\frac{\mu V_{ds}}{L}}$$

$$\tilde{T}_{ds} = L^2/\mu V_{ds} \longrightarrow (6)$$

Sub (6) in (1)

$$I_{ds} = \frac{Q_c}{\tau_{ds}}$$

$$I_{ds} = \frac{Q_c}{\frac{L^2}{\mu V_{ds}}}$$

$$\boxed{I_{ds} = \frac{Q_c \mu V_{ds}}{L^2}}$$

* μ_n - 650 $cm^2/vsec$
μ_p - 240 $cm^2/vsec$ at room temperature

Case (i):- Non-saturation

when it is in non-saturation then the effective voltage is $\frac{V_{ds}}{2}$.

The charge 'Q_c' can be given as

$$Q_c = E_g \varepsilon_0 \varepsilon_{ins} w L \longrightarrow (1)$$

where E_g is effective gate voltage

ε_0 is permittivity of free space

$\varepsilon_0 = 8.854 \times 10^{-12}$ F/m

ε_{ins} = Relative Permittivity

$\varepsilon_{ins} = 4$ (for silicon)

w = width

L = length

we know that $E_g = \frac{\left[V_g - \frac{V_{ds}}{2}\right]}{D}$

where D = oxide thickness,

wkt $V_g = V_{gs} - V_t$

$$E_g = \frac{\left[(V_{gs} - V_t) - \frac{V_{ds}}{2}\right]}{D} \longrightarrow (2)$$

$$Q_c = \left[\frac{(V_{gs} - V_t) - \frac{V_{ds}}{2}}{D} \right] \varepsilon_0 \varepsilon_{ins} \omega L$$

$$Q_c = \left[(V_{gs} - V_t) - \frac{V_{ds}}{2} \right] \frac{\varepsilon_0 \varepsilon_{ins} \omega L}{D} \longrightarrow (3)$$

ωKT

$$I_{ds} = \frac{Q_c \mu V_{ds}}{L^2}$$

Sub eqn (3) in I_{ds}, we get

$$I_{ds} = \left[(V_{gs} - V_t) - \frac{V_{ds}}{2} \right] \frac{\varepsilon_0 \varepsilon_{ins} \omega L}{D} \frac{\mu V_{ds}}{L^2}$$

$$I_{ds} = \left[(V_{gs} - V_t) - \frac{V_{ds}}{2} \right] \frac{\varepsilon_0 \varepsilon_{ins} \mu \omega V_{ds}}{DL}$$

$$I_{ds} = \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right] \frac{\varepsilon_0 \varepsilon_{ins} \mu}{D} \frac{\omega}{L}$$

Let $k = \frac{\varepsilon_0 \varepsilon_{ins} \mu}{D}$

$$\boxed{I_{ds} = \frac{k\omega}{L} \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right]}$$

Let $\frac{k\omega}{L} = \beta$

$$\boxed{I_{ds} = \beta \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right]}$$

$$C_g = \frac{k\omega L}{\mu} \implies k = \frac{C_g \cdot \mu}{\omega L}$$

C_g = gate to channel capacitance

$$I_{ds} = \frac{C_g \mu}{\cancel{W} L} \cdot \frac{\cancel{W}}{L}\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right]$$

$$\boxed{I_{ds} = \frac{C_g \mu}{L^2}\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right]}$$

wkt $C_g = C_o \omega L$

$$\boxed{I_{ds} = \frac{C_o \omega \mu}{L^2}\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right]}$$

Case(2):- Saturation $[V_{ds} = V_{gs} - V_t]$

$$I_{ds} = \frac{K\omega}{L}\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right] \longrightarrow (1)$$

→ Saturation starts at $V_{ds} = V_{gs} - V_t$

→ $$I_{ds} = \frac{K\omega}{L}\left[V_{ds}^2 - \frac{V_{ds}^2}{2}\right]$$

$$I_{ds} = \frac{K\omega}{L}\left[\frac{V_{ds}^2}{2}\right]$$

$$\boxed{I_{ds} = \frac{K\omega}{L}\left[\frac{(V_{gs} - V_t)^2}{2}\right]}$$

let $\frac{K\omega}{L} = \beta$

$$\boxed{I_{ds} = \beta\left[\frac{V_{gs} - V_t}{2}\right]^2}$$

$$I_{ds} = \frac{K\omega}{L}\left[\frac{(V_{gs} - V_t)^2}{2}\right]$$

WKT $C_g = \frac{K W L}{\mu} \Rightarrow K = \frac{C_g \cdot \mu}{WL}$

$\Rightarrow I_{ds} = \frac{C_g \mu}{WL} \frac{W}{L} \cdot \left[\frac{(V_{gs}-V_t)^2}{2}\right]$

$$\boxed{I_{ds} = \frac{C_g \mu}{L^2}\left[\frac{(V_{gs}-V_t)^2}{2}\right]}$$

WKT $C_g = C_o W L$

$I_{ds} = \frac{C_o W L \mu}{L^2} \left[\frac{(V_{gs}-V_t)^2}{2}\right]$

$$\boxed{I_{ds} = \frac{C_o W \mu}{L}\left[\frac{(V_{gs}-V_t)^2}{2}\right]}$$

Trans Conductance (g_m)

Trans conductance is defined as the relationship between output current 'I_{ds}' and input voltage 'V_{gs}'.

$\because g_m = \left.\frac{\delta I_{ds}}{\delta V_{gs}}\right|_{V_{ds} = \text{constant}}$

WKT $I_{ds} = \frac{Q_c}{\tilde{T}_{ds}}$

$\tilde{T}_{ds} = \frac{L^2}{\mu V_{ds}}$

$$\boxed{I_{ds} = \frac{Q_c \mu V_{ds}}{L^2}}$$

$$\boxed{\delta I_{ds} = \frac{\delta Q_c \mu V_{ds}}{L^2}}$$

WKT $C_g = \frac{K W L}{\mu} \Rightarrow K = \frac{C_g \cdot \mu}{WL}$

$\Rightarrow I_{ds} = \frac{C_g \mu}{WL} \frac{W}{L} \cdot \left[\frac{(V_{gs} - V_t)^2}{2}\right]$

$$\boxed{I_{ds} = \frac{C_g \mu}{L^2} \left[\frac{(V_{gs} - V_t)^2}{2}\right]}$$

WKT $C_g = C_o W L$

$I_{ds} = \frac{C_o W L \mu}{L^2} \left[\frac{(V_{gs} - V_t)^2}{2}\right]$

$$\boxed{I_{ds} = \frac{C_o W \mu}{L} \left[\frac{(V_{gs} - V_t)^2}{2}\right]}$$

Trans Conductance (g_m)

Trans conductance is defined as the relationship between output current 'I_{ds}' and input voltage 'V_{gs}'.

$\because g_m = \left.\frac{\delta I_{ds}}{\delta V_{gs}}\right|_{V_{ds} = \text{constant}}$

WKT $I_{ds} = \frac{Q_c}{\tau_{ds}}$

$\tau_{ds} = \frac{L^2}{\mu V_{ds}}$

$$\boxed{I_{ds} = \frac{Q_c \mu V_{ds}}{L^2}}$$

$$\boxed{\delta I_{ds} = \frac{\delta Q_c \mu V_{ds}}{L^2}}$$

WKT

$$C_g = \frac{Q_c}{V_{gs}}$$

$$V_{gs} = \frac{Q_c}{C_g}$$

$$\boxed{\delta V_{gs} = \frac{\delta Q_c}{C_g}}$$

$$\therefore g_m = \frac{\delta I_{ds}}{\delta V_{gs}}$$

$$= \frac{\frac{\delta Q_c \mu V_{ds}}{L^2}}{\frac{\delta Q_c}{C_g}}$$

$$\boxed{g_m = \frac{C_g \mu V_{ds}}{L^2}}$$

WKT $C_g = C_o \omega L$

$$\therefore g_m = \frac{C_o \omega L \mu V_{ds}}{L^2}$$

$$\boxed{g_m = \frac{C_o \omega \mu V_{ds}}{L}}$$

Output Conductance [g_{ds}]:-

The output conductance g_{ds} is defined as the relationship between output current I_{ds} and input voltage V_{gs}.

$$g_{ds} = \left.\frac{I_{ds}}{V_{gs}}\right|_{V_{ds}=\text{constant}}$$

WKT $I_{dc} = \frac{Q_c \mu V_{ds}}{L^2}$ and $V_{gs} = \frac{Q_c}{C_g}$

$\therefore$ $g_{ds} = \frac{\frac{Q_c \mu V_{ds}}{L^2}}{\frac{Q_c}{C_g}}$

$$\boxed{g_{ds} = C_g \frac{\mu V_{ds}}{L^2}}$$

$\therefore$ $\boxed{g_{ds} \propto \frac{1}{L^2}}$

An increase in the channel length of a device may cause reduce output conductance g_{ds}.

Figure of Merit (ω_0):-

The figure of merit ω_0 is defined as the ratio of transconductance to the gate to channel capacitance (C_g).

$\therefore$ $\boxed{\omega_0 = \frac{g_m}{C_g}}$

WKT $g_m = \frac{C_g \mu V_{ds}}{L^2}$

$$\omega_0 = \frac{\frac{C_g \mu V_{ds}}{L^2}}{C_g}$$

$$\therefore W_D = \frac{\mu V_{ds}}{l^2}$$

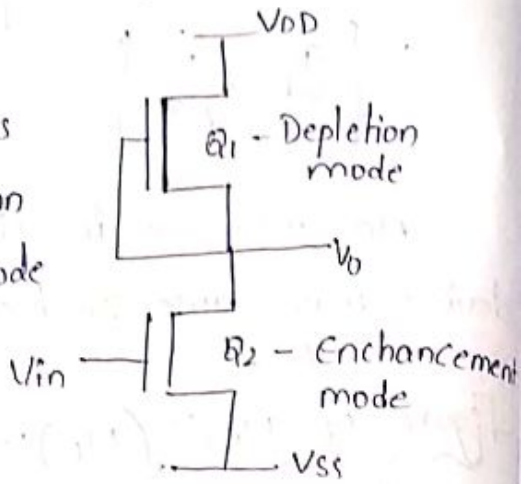
Since $V_{ds} = V_{gs} - V_t$

$$\boxed{W_D = \frac{\mu (V_{gs} - V_t)}{l^2}}$$

N-MOS Inverter:-

The N-mos inverter is more oftenly use and it can produce full amount of logic levels.

Description:-



* The arrangement of nmos inverter consists of depletion mode and enchancement mode transistors.
* Here the gate terminal of depletion mode nmos is connected to the drain terminal of enchancement mode nmos.
* The depletion mode transistor is always on because of the inbuilt channel.

Operation:-

Case(1):-

When V_{in} is logic '1'

When Input is logic 1 the transistor Q_2 turns ON and transistor Q_1 is always turns ON because it is depletion mode

Truth Table:-

V_{in}	Q_1	Q_2	V_0
0	ON	OFF	1
1	ON	ON	0

then Vout is logic 0.

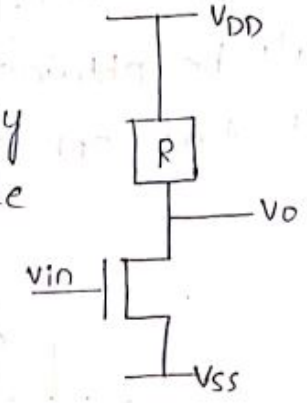
Case(2):-

When V_1 is logic '0'

When input is logic '0' then the transistor Q2 remains OFF and Q1 is ON hence the o/p voltage is logic '1'.

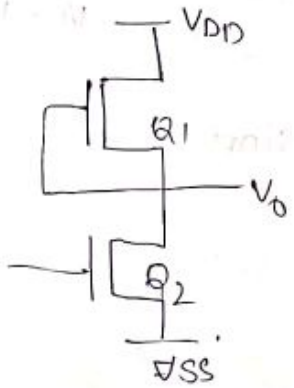
Alternative Forms of pull-up:-

1. Resistive pull-up:- the Resistive pull-up configuration is not oftenly used while designing silicon substrate because high Resistive values are not incooperated in that silicon substrate.



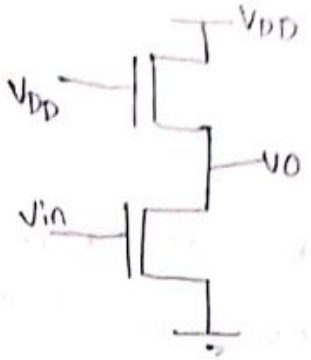
2. Depletion mode pull-up:-

It can produce High power disspitation and there may be a current flow in blw supply rails when vin is logic '1'.



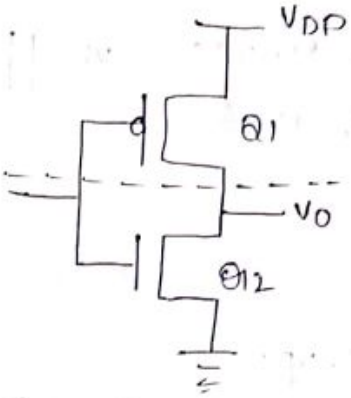
3. Enchancement mode pull-up:-

It produces high power disspiation blw supply rails and conduction starts when $V_{DD} = V_{gg}$



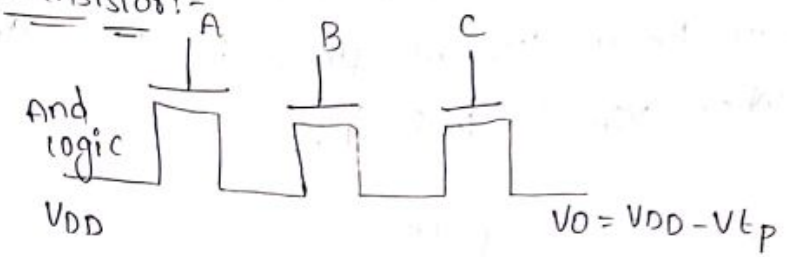
4. Complementary mass pull-up:-

In this configuration full-amount of logic level can't be obtained and only one transistor will get turn ON either for logic '0' or (1).



Pass transistor:-

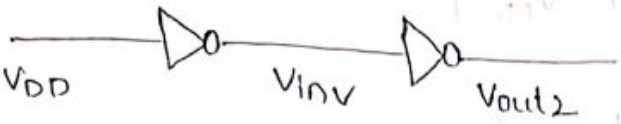
Eg:-



* unlike Bipolar transistors

pullup to pulldown ratio of nmos-inverter driven by another nmos inverter :-

The arrangement of pullup to pulldown ratio for one nmos inverter driven by another nmos is shown as below.



WKT

I_{ds} for saturation mode

$$I_{ds} = \frac{k w}{L}\left[\frac{(V_{gs}-V_t)}{2}\right]^2$$

for depletion mode $V_{gs}=0$

$$I_{ds} = k\frac{w_{pu}}{L_{pu}}\left[\frac{(-V_{td})}{2}\right]^2 \longrightarrow (1)$$

I_{ds} for enchancement mode, $V_{gs} = V_{inv}$

$$I_{ds} = \frac{k w_{pd}}{L_{pd}}\left[\frac{(V_{inv}-V_t)^2}{2}\right] \longrightarrow (2)$$

equating (1) and (2), (1) = (2) we get

$$\frac{k w_{pu}}{L_{pu}}\frac{(-V_{td})^2}{2} = \frac{k w_{pd}}{L_{pd}}\frac{(V_{inv}-V_t)^2}{2}$$

$$\frac{1}{Z_{pu}}(-V_{td})^2 = \frac{1}{Z_{pd}}(V_{inv}-V_t)^2$$

$$(-V_{td})^2 = \frac{Z_{pu}}{Z_{pd}}(V_{inv}-V_t)^2$$

$$\frac{Z_{pu}}{Z_{pd}} = \frac{(-V_{td})^2}{(V_{inv}-V_t)^2}$$

$$\frac{Z_{pu}}{Z_{pd}} = \frac{(0.6V_{DD})^2}{(0.5V_{DD} - 0.2V_{DD})^2}$$

$V_{td} = 0.6V_{DD}$

$V_t = 0.2V_{DD}$

$V_{inv} = 0.5V_{DD}$

$$= \left(\frac{0.6V_{DD}}{0.3V_{DD}}\right)^2$$

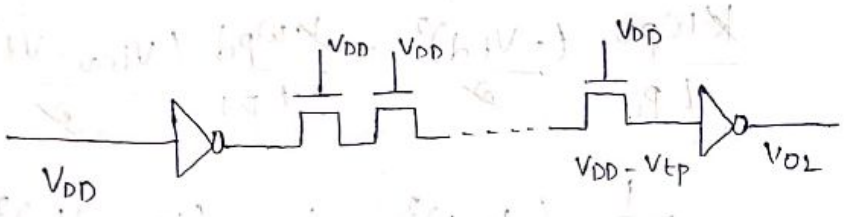
$$\frac{Z_{pu}}{Z_{pd}} = \frac{4}{1}$$

$$\boxed{\frac{Z_{pu}}{Z_{pd}} = 4:1}$$

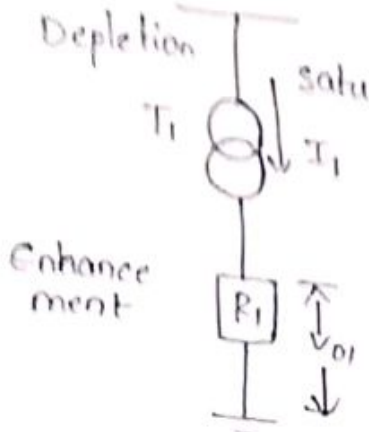
∴ The pullup to pulldown ratio of nmos inverter driven by another nmos is 4:1

Pullup to pulldown ratio of nmos driven by another nmos with one or more pass transistors:-

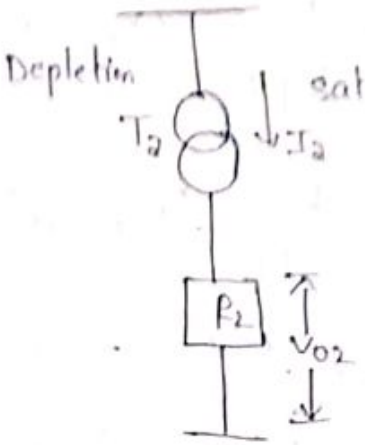
The arrangement of pullup to pulldown ratio for nmos driven by another nmos with one or more pass transistors is depicted as below.



* when the output of inverter 1 is passed through series of pass transistors then full logic levels are not obtain due to threshold voltage of pass transistors. ie., $V_{inv2} = V_{DD} - V_{tp}$.



(a) inv_1 with i/p as V_{DD}



(b) inv_2 with i/p as $V_{DD}-V_{tp}$

for inverter 1

I_{ds} for saturation mode

$$I_{ds} = \frac{kw}{L}\left(\frac{V_{gs}-V_t}{2}\right)^2$$

for depletion mode, $V_{gs}=0$

$$I_{ds1} = \frac{k w_{pu1}}{L_{pu1}}\left(\frac{-V_{td}}{2}\right)^2$$

$$\boxed{I_1 = \frac{K}{Z_{pu1}}\left(\frac{-V_{td}}{2}\right)^2}$$

for non-saturation, I_{ds} can be similar

$$I_{ds} = \frac{kw}{L}\left[(V_{gs}-V_t)V_{ds} - \frac{V_{ds}^2}{2}\right]$$

for enhancement mode, $V_{gs}=V_{DD}$

$$I_{ds1} = \frac{k w_{pd1}}{L_{pd1}}\left[(V_{DD}-V_t)V_{ds1} - \frac{V_{ds1}^2}{2}\right]$$

$$\frac{I_{ds1}}{V_{ds1}} = \frac{k w_{pd1}}{L_{pd1}}\left[(V_{DD}-V_t) - \underbrace{\frac{V_{ds1}}{2}}_{\text{neglecting}}\right]$$

$$\frac{I_{ds1}}{V_{ds1}} = \frac{k}{Z_{pd1}} (V_{DD} - V_t)$$

$$\frac{1}{R_1} = \frac{k}{Z_{pd1}} (V_{DD} - V_t)$$

$$\boxed{R_1 = \frac{Z_{pd1}}{K(V_{DD} - V_t).}}$$

$$V_{O1} = I_1 R_1$$

$$V_{O1} = \frac{K}{Z_{pu1}} \frac{(-V_{td})^2}{2} \times \frac{Z_{pd1}}{K(V_{DD} - V_t)}$$

$$\boxed{V_{O1} = \frac{Z_{pd1}}{Z_{pu1}} \frac{(-V_{td})^2}{2(V_{DD} - V_t)}}$$

For inverter 2

For saturation mode, I_{ds} can be seen by

$$I_{ds} = \frac{k\omega}{L} \frac{(V_{gs} - V_t)^2}{2}$$

For depletion mode, $V_{gs} = 0$

$$I_{ds2} = \frac{k\omega_{pu2}}{L_{pu2}} \frac{(-V_{td})^2}{2}$$

$$\boxed{I_2 = \frac{K}{Z_{pu2}} \frac{(-V_{td})^2}{2}}$$

I_{ds} in non-saturation can be given by

$$I_{ds} = \frac{k\omega}{L} \left[[V_{gs} - V_t] V_{ds} - \frac{V_{ds}^2}{2} \right]$$

For enhancement mode, $V_{gs} = V_{DD} - V_{tp}$

$$I_{ds2} = \frac{k w_{pd2}}{l_{pd2}} \left[(V_{gs} - V_t) V_{ds2} - \frac{V_{ds2}^2}{2} \right]$$

$$\frac{I_{ds2}}{V_{ds2}} = \frac{k}{z_{pd2}} \left[(V_{gs} - V_t) - \underbrace{\frac{V_{ds}}{2}}_{\text{neglecting}} \right]$$

$$\frac{1}{R_2} = \frac{k}{z_{pd2}} \left[V_{gs} - V_t \right]$$

$$\therefore \boxed{V_{gs} = V_{DD} - V_{tp}}$$

$$\frac{1}{R_2} = \frac{k}{z_{pd2}} (V_{DD} - V_{tp} - V_t)$$

$$\boxed{R_2 = \frac{z_{pd2}}{k (V_{DD} - V_{tp} - V_t)}}$$

$$V_{O2} = I_2 R_2$$

$$= \frac{k}{z_{pu2}} \frac{(-V_{td})^2}{2} \times \frac{z_{pd2}}{k (V_{DD} - V_{tp} - V_t)}$$

$$\boxed{V_{O2} = \frac{z_{pd2}}{z_{pu2}} \frac{(-V_{td})^2}{2 (V_{DD} - V_{tp} - V_t)}}$$

$$V_{O1} = \frac{z_{pd1}}{z_{pu1}} \frac{(-V_{td})^2}{2 (V_{DD} - V_t)}$$

$$\boxed{V_{O1} = V_{O2}}$$

$$\frac{z_{pd1}}{z_{pu1}} \frac{(-V_{td})^2}{2 (V_{DD} - V_t)} = \frac{z_{pd2}}{z_{pu2}} \frac{(-V_{td})^2}{2 (V_{DD} - V_{tp} - V_t)}$$

$$\frac{Z_{pd1}}{Z_{pu1}(V_{DD}-V_t)} = \frac{Z_{pd2}}{Z_{pu2}(V_{DD}-V_{tp}-V_t)}$$

$$\frac{Z_{pd2}}{Z_{pu2}} = \frac{Z_{pd1}(V_{DD}-V_{tp}-V_t)}{Z_{pu1}(V_{DD}-V_t)}$$

$$\frac{Z_{pu2}}{Z_{pd2}} = \frac{Z_{pu1}(V_{DD}-V_t)}{Z_{pd1}(V_{DD}-V_{tp}-V_t)}$$

$$\frac{Z_{pu2}}{Z_{pd2}} = \frac{4}{1} \times \frac{V_{DD}-0.2V_{DD}}{(V_{DD}-0.3V_{DD}-0.2V_{DD})}$$

$V_t = 0.2V_{DD}$

$V_{tp} \simeq 0.3V_{DD}$

$$= \frac{4}{1} \times \frac{0.8\,V_{DD}}{0.5\,V_{DD}}$$

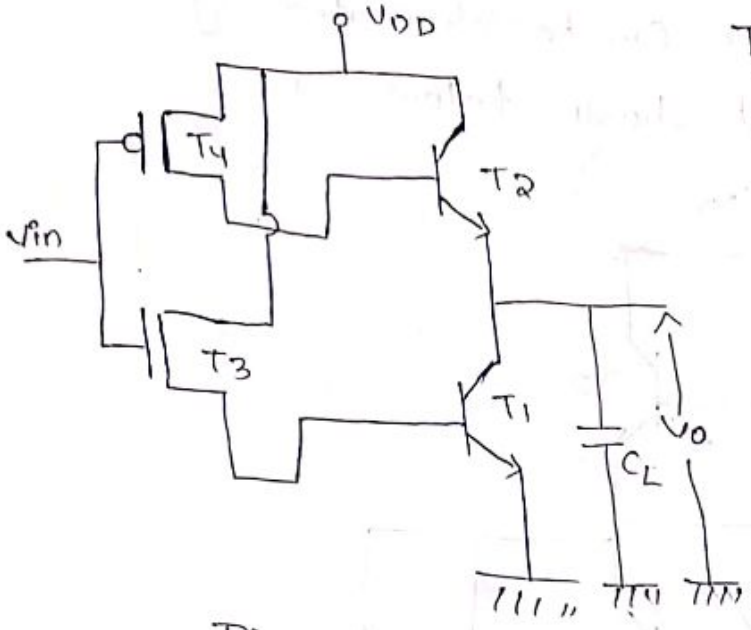
$$\simeq \frac{4}{1} \times \frac{8}{4}$$

$$\boxed{\frac{Z_{pu2}}{Z_{pd2}} \simeq \frac{8}{1}}$$

∴ The pullup to pulldown ratio of nmos driven by another nmos with one or more pass transistors is 8:1

BiCMOS Inverter:-

To get logical switching of mos transistor, bipolar transistors are attach at their ends.



Truth Table

Vin	T_1	T_2	T_3	T_4	V_o
0	OFF	ON	OFF	ON	1
1	ON	OFF	ON	OFF	0

BiCMOS Inverter

operation:-

Case(1):- when Vin = logic '0'.

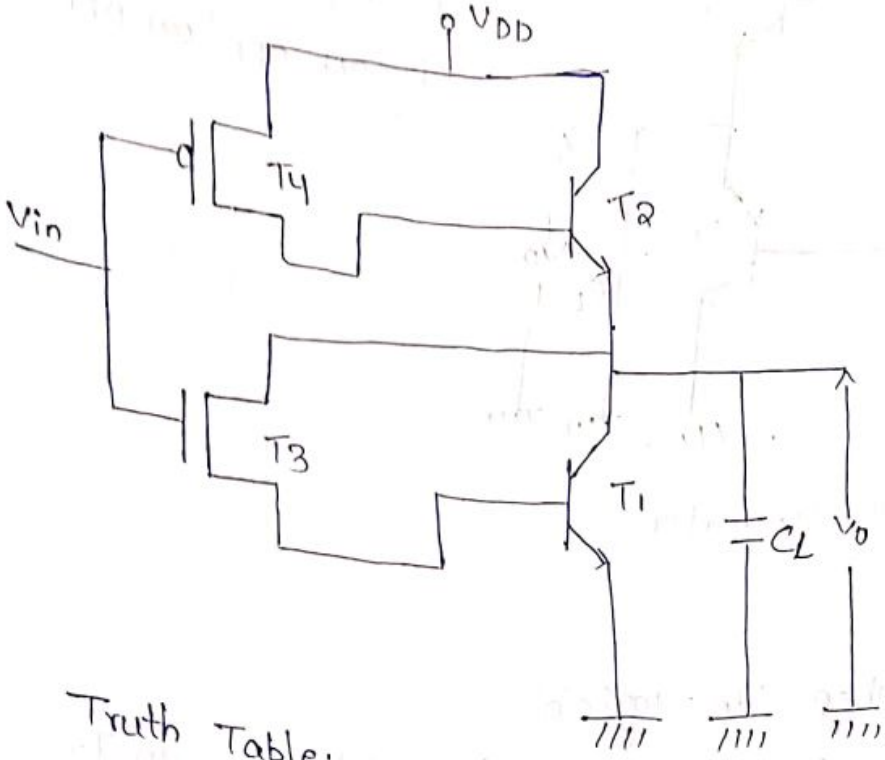
when Vin is logic '0' but transistor T_4 on T_2 will get turn ON and transistor T_3 and T_1 will get turn OFF. then the capacitor C_L gets change hence output is logic 1.

Case(2):- when Vin is logic '1'.

when Vin is logic '1' then t_3 and t_1 will get ON and t_2 and t_4 will get OFF. Here that capacitor C_L gets discharge hence output is logic '0'.

* for logic '1' t_1 and t_3 will get ON and their by it forms a short circuit path between V_{DD} and V_{SS} which inturn cause static power disspiation and this will slowdown transistor action.

* The above drawback can be eliminated by the modified arrangement shown below.



Truth Table:-

Vin	T_1	T_2	T_3	T_4	V_o
0	OFF	ON	OFF	ON	1
1	ON	OFF	ON	OFF	0

Alternative BiCMOS with no static power dissipation

* In this circuit for logic '1' their is no short ckt path between V_{DD} and V_{SS}, means their is no static power dissipation.

* Hence output swing is reduce.

Since output voltage can't fall below the base emitter of T_2 that is V_{BE} of T_2 and this can be overcome by another improved circuit shown below.

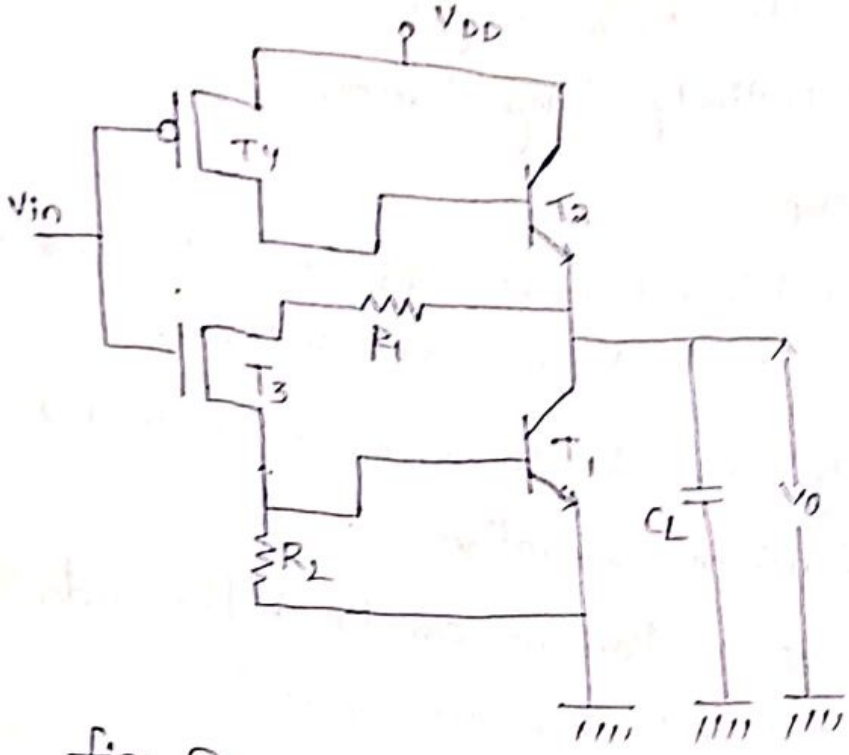


fig: Improved Bicmos with Better logic levels

*In this arrogement the resistors provide the improved Swing of output voltages when BJT's are off and also provide discharge path for Base Currents during turn off.

* However the profision of onchip Resistors of Suitable value is not always convient and maybe Space Consuming so the above circuit may be further modified as shown below.

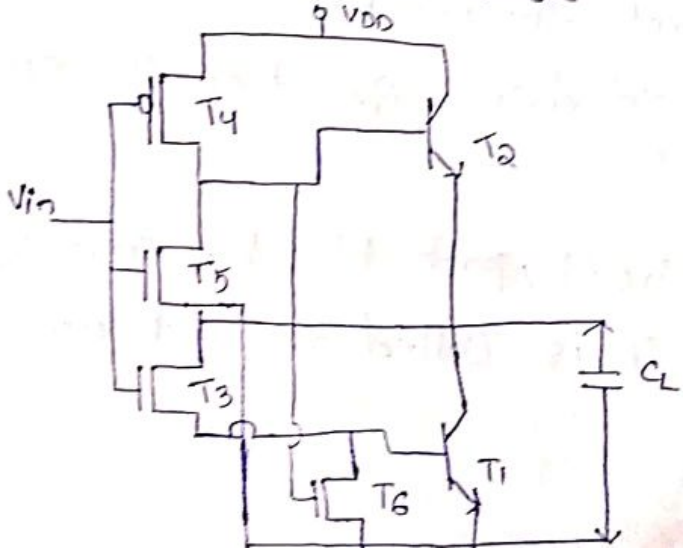
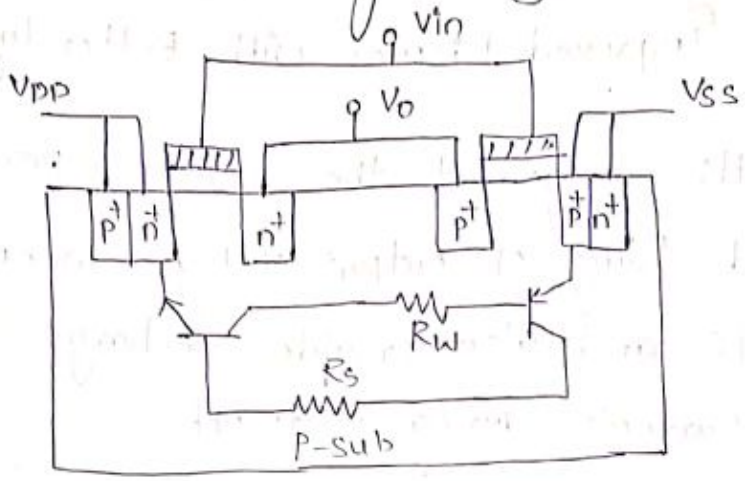


fig: Improve bicmos Inverter using mos transistors for base current drive

The Transistors T_5, T_6 will get turn ON when T_1 and T_2 respectively being turn off.

Latch up in CMOS:-

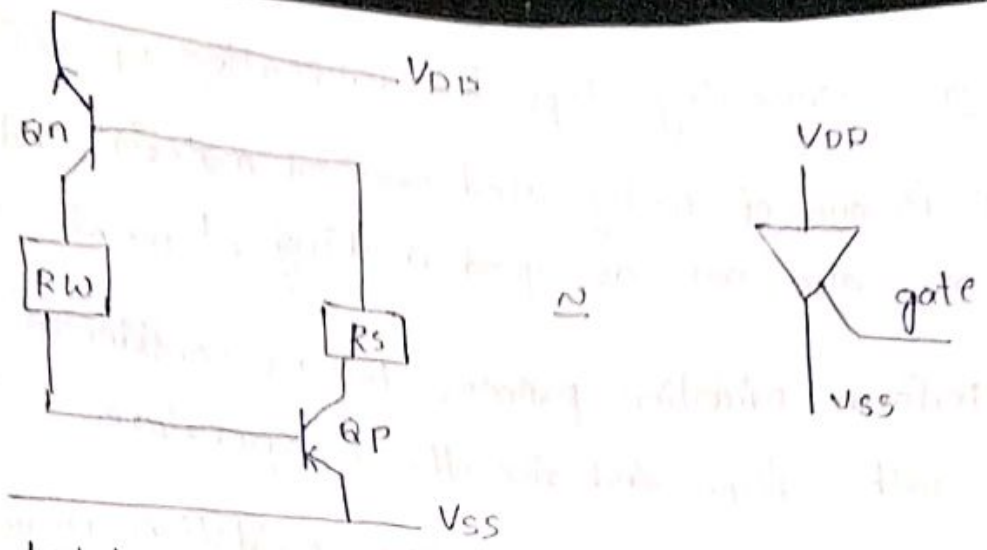
* Latch of is a inherent problem in CMOS, that provide a low impedance path between V_{DD} and V_{SS}.
* latch up may arise due to noise, switch ON and OFF or by Incident radiation.
* The latch up mechanism can be better understood with the following arrangement



Latch up effecting n-well substrate

* In the above figure, if Sufficient substrate current flows for Q_P, then Q_P will turn ON & it draws some current through R_S.
* If it is enough to drive Q_n then it will also turn ON.

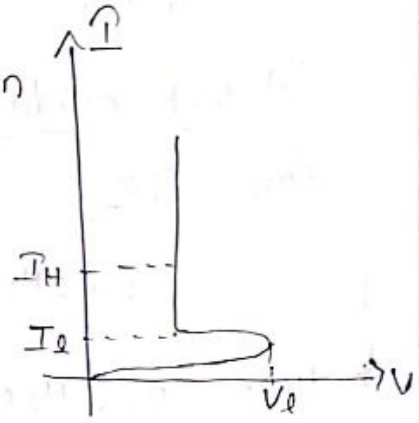
Hence a short circuit path blw V_{DD} and V_{SS} is obtained and it is called as latch up problem.



Latch up circuit model

* The swinging characteristics of the arrangement are shown as below.

* once it is latch, this condition will be maintain untill latch up Current drops below I_L



latch up V I Characteristics of SCR.

Remidies for latch up:-

* Introduction of gard rings Can eliminate latch up problem.

* Increase in the substrate dopping levels, with a constitute drop in the value of Rs.

* Reduce Rw by control of fabrication parameters and by ensuring low contact resistance to Vss.

* **Oxidation:-** Processing steps for fabrication of ICs:

Silicon is one of mostly used oxidised material and which may also acts as good masking element.

* To perform oxidation process let us consider a furnace with silicon and rise the temperature.

* Oxidation is two types 1) Dray oxidation: Here the silicon is reacting with O_2 to form SiO_2.

$$Si + O_2 \longrightarrow SiO_2$$

2) Wet oxidation: Silicon reacts with H_2O to form SiO_2.

$$Si + 2H_2O \longrightarrow SiO_2 + 2H_2$$

* Here O_2, H_2O are called oxidants that are use to oxidise silicon.

* **Ion implantation:-**

ion implantation process is use to diffuse the dopands into a specified material (or) Substrate.

* Here the dopand is to be diffuse into a substrate material with a sufficient energy.

* By the strength of the dopand it penterates through the substrate and may cause some effect on lattice atom.

Nuclear Stoping:- when the dopand is injected into the Substrate, depending upon the strength the dopand

may change the position of lattice atom and may damage the lattice atom. If the strength is further more increase. Hence it is called Nuclear stoping.

electronic
* During ion implantation process, if the dopands change the position of the lattice atom and it is shows no damage of lattice atom. Hence it is called electronic stoping.

* photolithography (or) Lithography :-
(light → photo, stone → litho)

photolithography is a process that is used to diffuse dopands into substrate in a selected position through masking element.

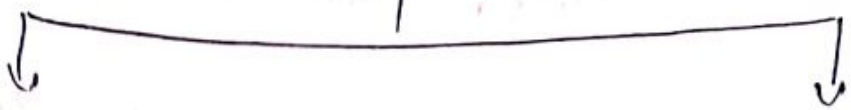
i.e; Lithography (or) photolithography is the process of transfering geometrical patterns from masking element to silicon.

* In olden days, we don't have photolithography technology then a mask of suitable pattern is transfer into silicon using a litho (stone).

* Metalization :-

Metalization is the process that is use to extact terminals from the device. these terminals are used to have contact to the outside world that is means to measure output (throughput).

Metalization



ohmic contacts (Al)

Normal silicides (poly + silicon)

* Encapsulation:-

Encapsulation is the process that is use after manufacturing of the device.

Encapsulation provides protection to the whole body (or) package.

UNIT - II

Mos and Bicmos circuit designing processes

Introduction:-

To design any circuit first of all we need to take the design considerations that is the specifications of the component of the system.

All those individual components are to be interconnected and metalizations are used to have a package circuit.

Mos layers:-

The basic mos layers that are used to design a circuit includes n^+ diffusions, p^+ diffusions, poly-silicon and etc..

Stick diagrams:-

Stick diagroms are outlined representations of layouts.

The stick diagrams convey the designing of the circuit through colour codes.

* For the designing of stick diagroms and layouts the Mos layers using colour codes are drawn as below.

For Nmos

S.No	layer	color	stick diagram representation	layout representation
1.	n^+ diffusion	Green		
2.	p^+ diffusion	yellow		
3.	Polysilicon	Red		
4.	Metal	Blue		
5.	Ion implantation	yellow		
6.	Burried contact	Brown		
7.	Contact cut	Black	•	
8.	Supply lines	Black	X	
9.	Demarkation line	Brown	-----	

For PMOS:-

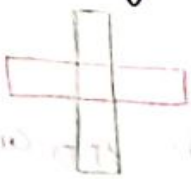
for pmos designing the only charge is ion implantation.

S.No.	layer	color	stick diagram representation	layout representation
1.	Ion Implant -ation	green		

Mos transistor representations:-

NMOS Enhancement

stick diagram



layout

PMOS Enhancement

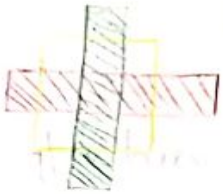
stick diagram

layout

NMOS depletion mode

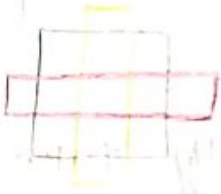
stick diagram

layout

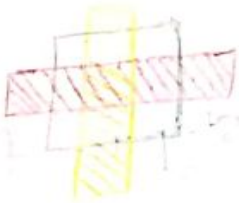


PMOS depletion mode

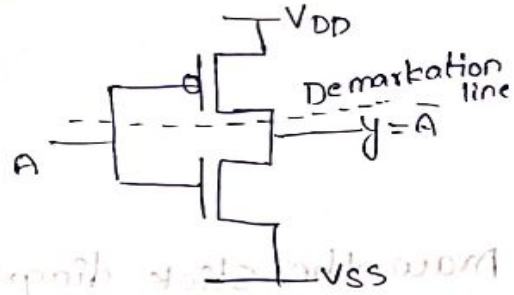
stick diagram



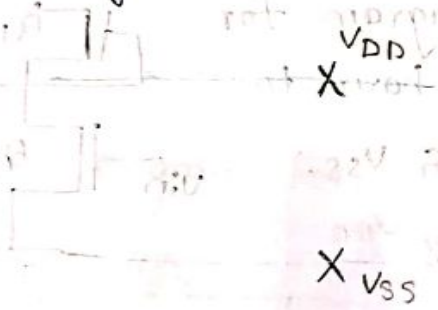
layout



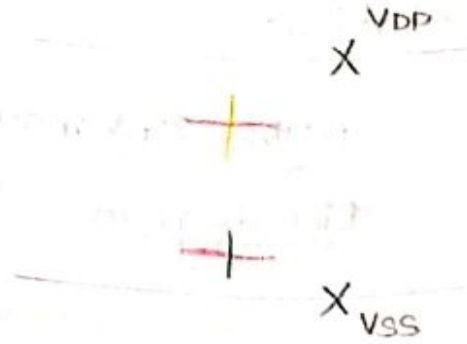
1. Design a stick diagram for Cmos inverter:-



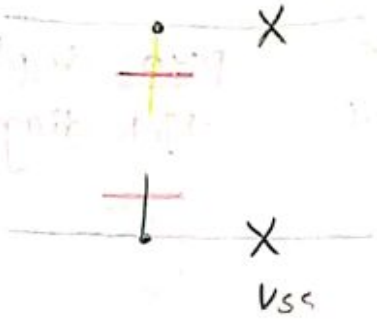
Step 1:- To design a cmos inverter, first we have to draw the supply lines V_{DD} and V_{SS}



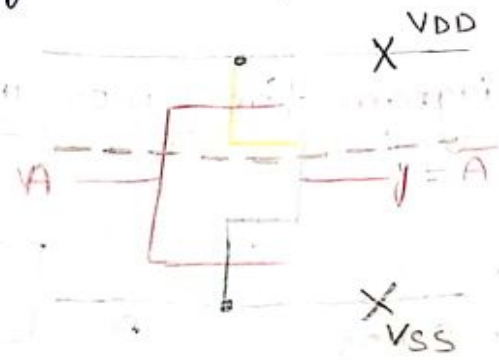
Step 2:- After V_{DD} and V_{SS} place the required transistors at a given place.



Step 3:- extend the transistors towards V_{DD} and V_{SS} and make contact cuts V_{DD}

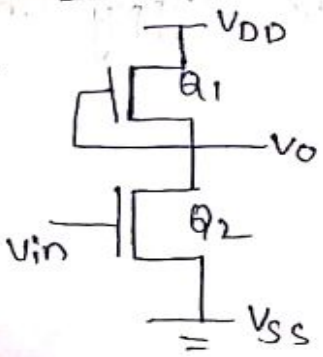


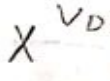
Step 4:- finally take i/p and o/p terminals

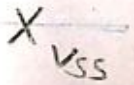


Q. Draw the stick diagram for nmos inverter:-

Step 1: To draw stick diagram for nmos inverter first we have to draw supply lines V_{DD} & V_{SS}.

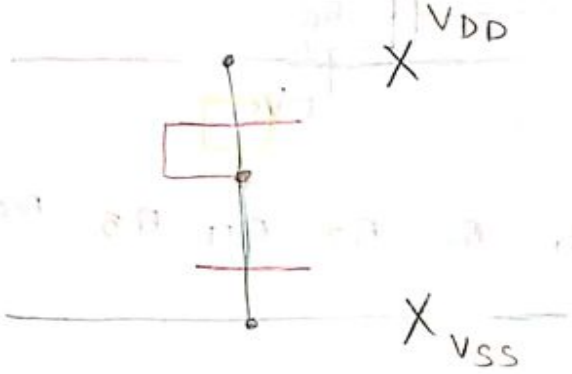




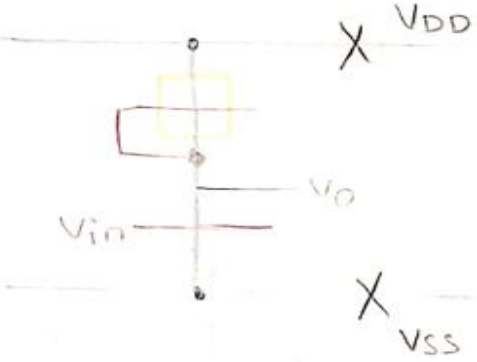


Step2:- After drawing supply lines place the required transistors.

Step3:- extend the transistor lines toward VDD and Vss and place contacts and Burried contact



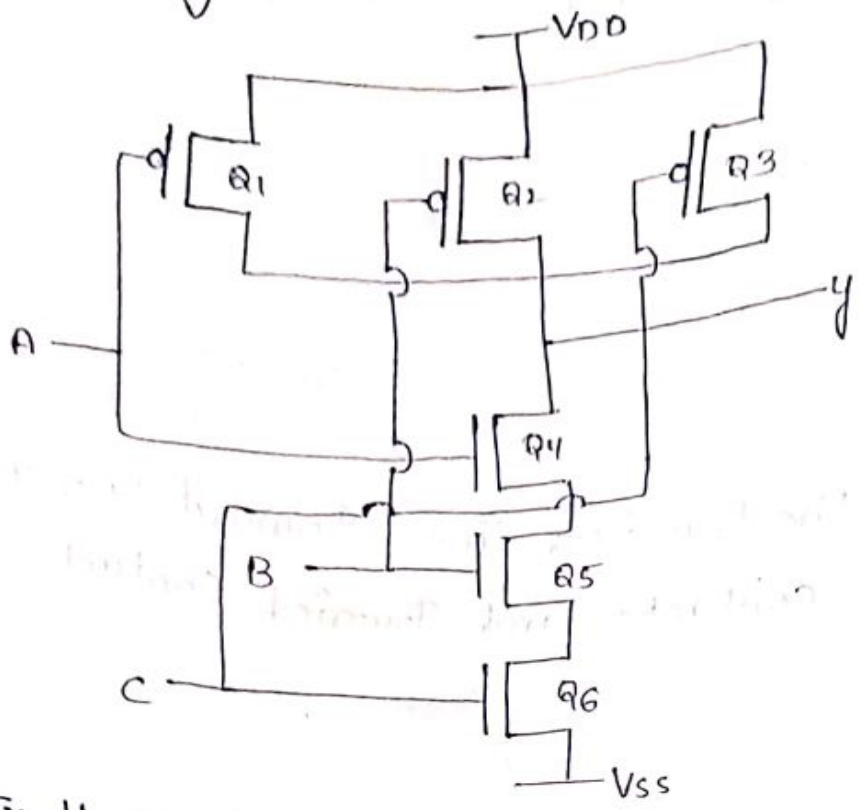
Step4:- finally take i/p and o/p's terminals.



3. Draw stick diagram for three input NAND gate using cmos technology.

	Nmos	pmos
NAND	series	parallel
NOR	parallel	series

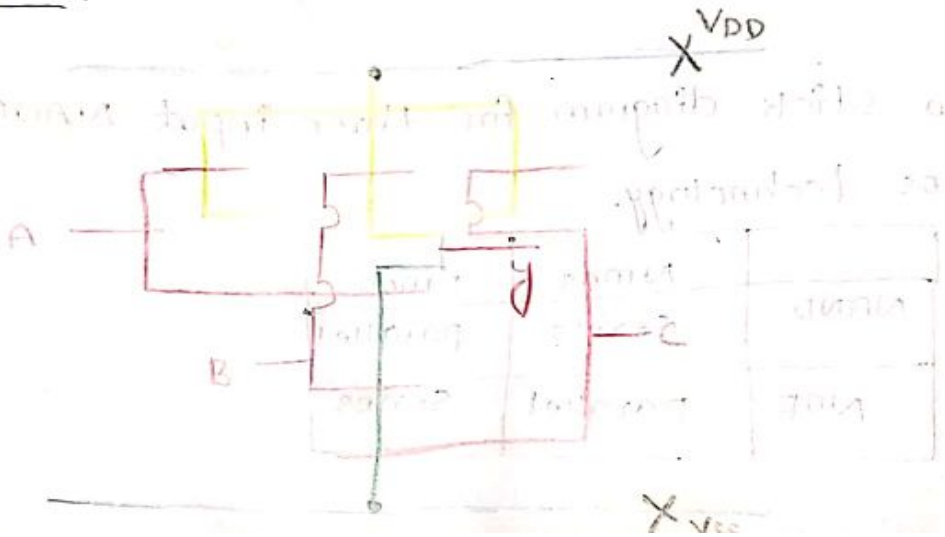
Circuit diagram



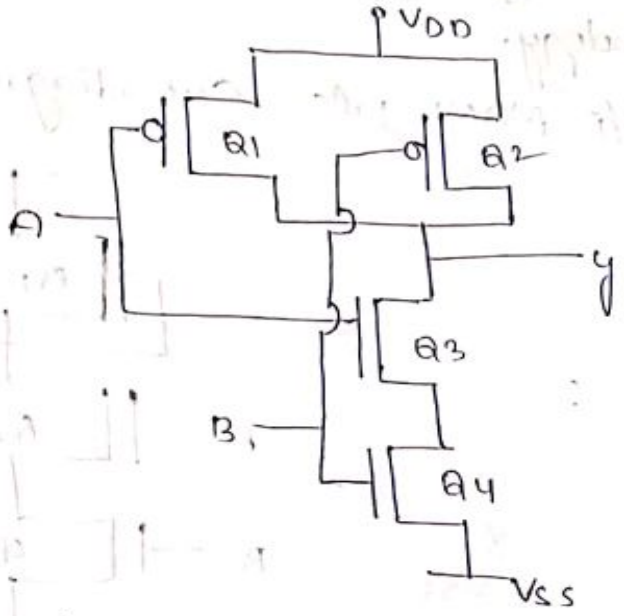
Truth Table

A	B	C	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	y
0	0	0							
0	0	1							
0	1	0							
0	1	1							
1	0	0							
1	0	1							
1	1	0							
1	1	1							

Stick diagram:-

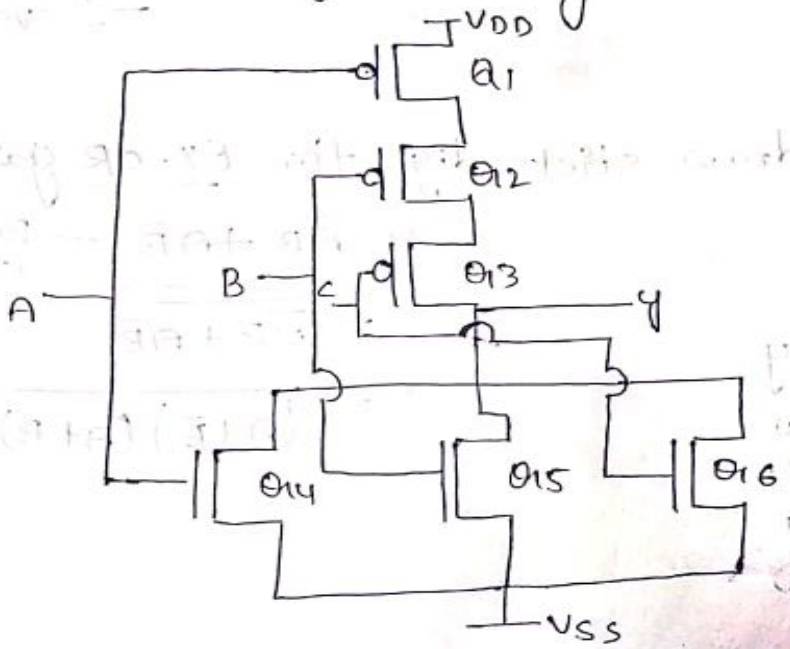


4. Draw the 2 i/p NAND gate using cmos technology



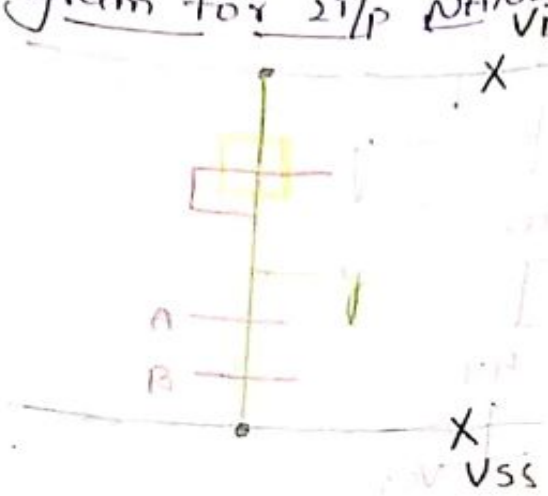
stick diagram:-

5) Draw 3 i/p NOR gate using cmos technology

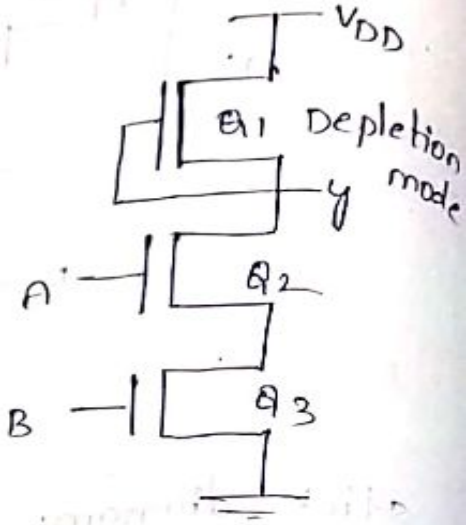


6) Draw the stick diagram for 2 i/p NAND gate using Nmos technology.

Stick diagram for 2 i/p NAND gate

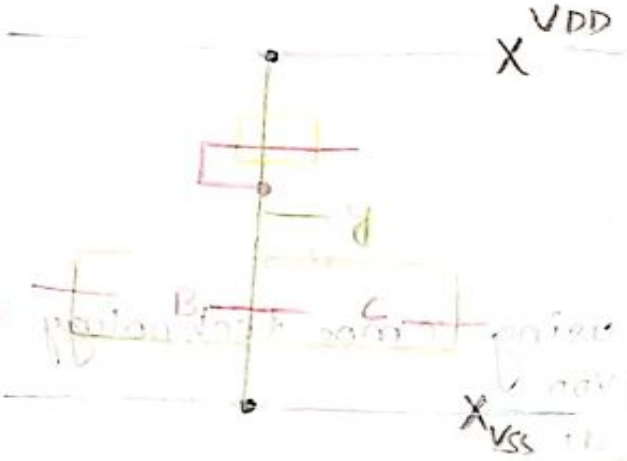


Ckt diagram

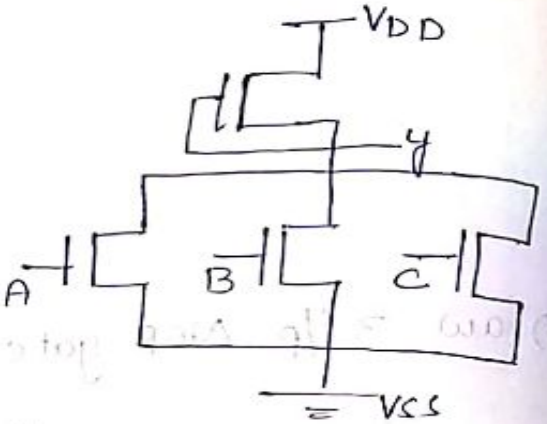


7) Draw the 3 i/p NOR gate using Nmos technology

Stick dig for 3 i/p NOR gate:-



Ckt diagram



8) Desig and draw stick dig for Ex-OR gate

Truth Table

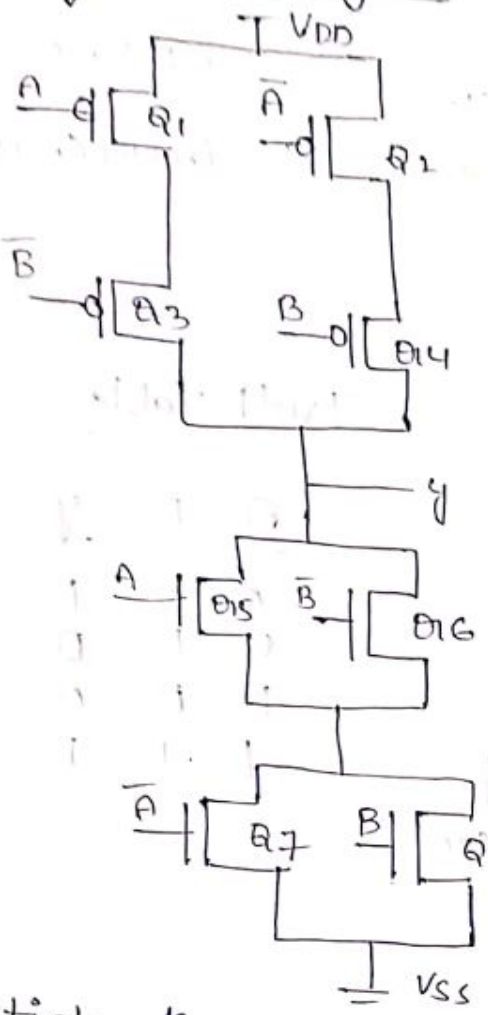
A	B	y
0	0	0
0	1	1
1	0	1
1	1	0

$y = \bar{A}B + A\bar{B}$ — Boolean expression

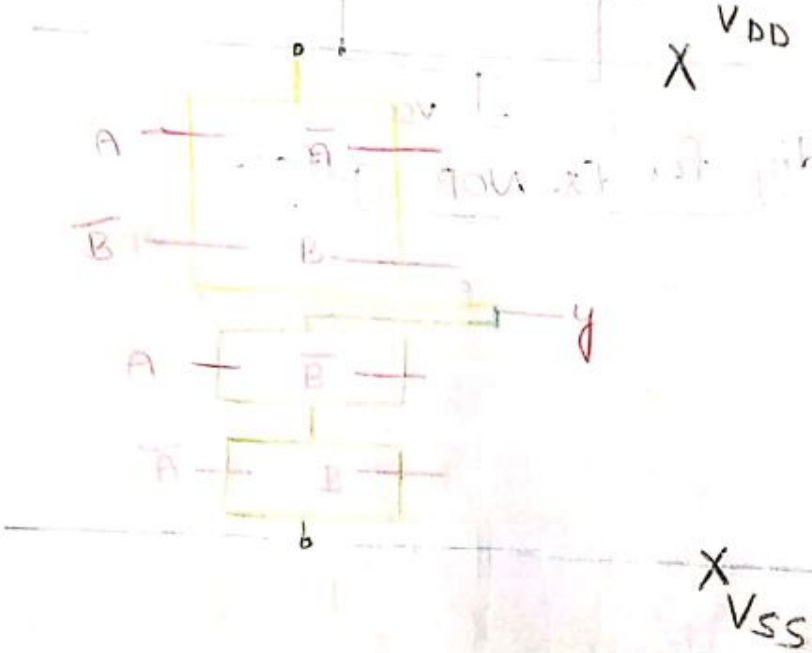
$= \overline{\bar{A}B + A\bar{B}}$

$= \overline{(A+\bar{B})(\bar{A}+B)}$

CKt dig for Ex-OR gate:-



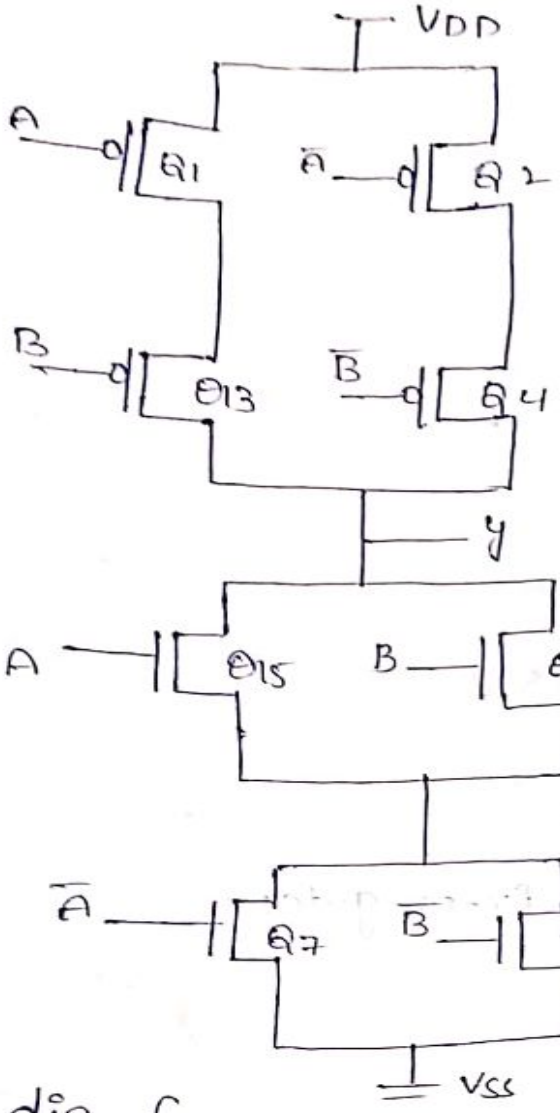
Stick diagram for Ex-or gate:-



9) Design ckt for Ex-NOR gate

$$y = \bar{A}B + A\bar{B}$$
$$= \overline{\overline{\bar{A}B + A\bar{B}}}$$
$$= \overline{(A+B)(\bar{A}+\bar{B})}$$

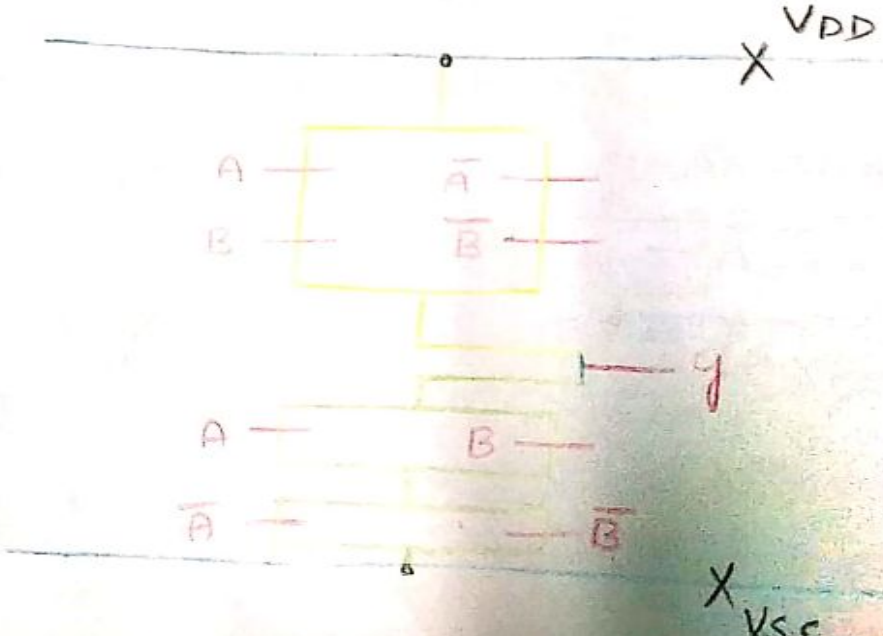
Ckt dig for Ex-NOR gate:-



Truth table

A	B	y
0	0	1
0	1	0
1	0	0
1	1	1

Stick dig for Ex-NOR gate:-



Design rules and layouts:-

* As the complexity of VLSI technology is more and more to have better understanding we are using a set of rules called Design rules.
* The design rules are the effective interface b/w Design Engineering and fabrication Engineering.
* ckt designers in general want tighter, smaller layouts for improved performance and reduced silicon area.
* The process Engineer want's Design rules that result's in a controlable and reproduces process.
* So, we need to have compromise b/w ckt designer and process engineer requirments.
* Basically we are having two types of design rules
  1. Scalable Design rules ('λ' base)
  2. Absolute Design rules (micron base)

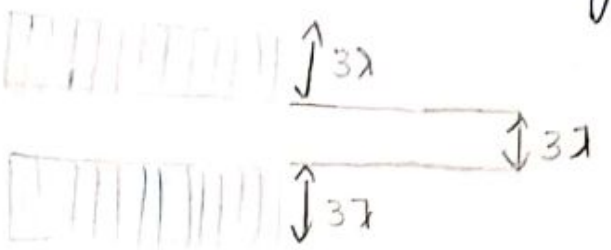
Scalable Design rules:-

1. The minwidth of metal 1 is 3λ and spacing b/w metal 1 and metal 1 is 3λ.
2. The minwidth of metal 2 is 4λ and spacing b/w metal 2 & metal 2 is 4λ.
3. The minwidth of n^+ diffusion (or) p^+ diffusion is 2λ and spacing b/w n^+ diffusion to n^+ diff & p^+ diffusion to p^+ diffusion is 3λ.

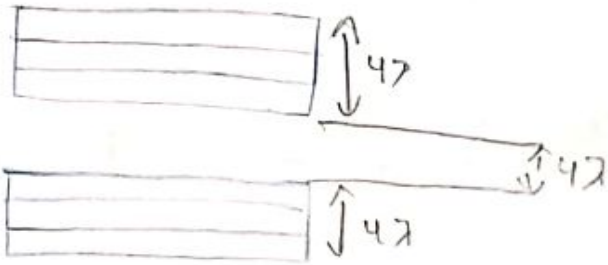
4. The minwidth of polysilicon is 2λ and spacing b/w polysilicon to polysilicon is 1λ.

Minwidth Min spacing

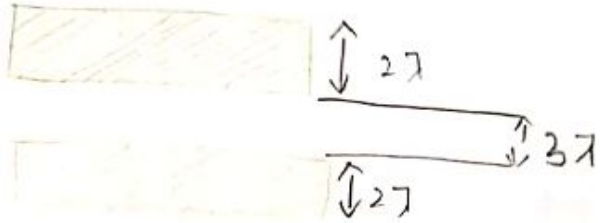
Metal 1:



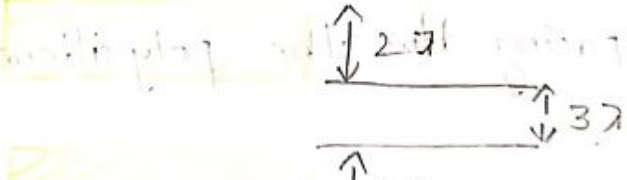
metal 2:-



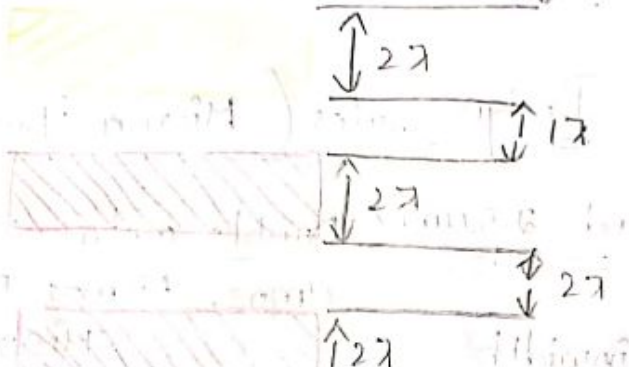
n^+ diffusion:



p^+ diffusion:

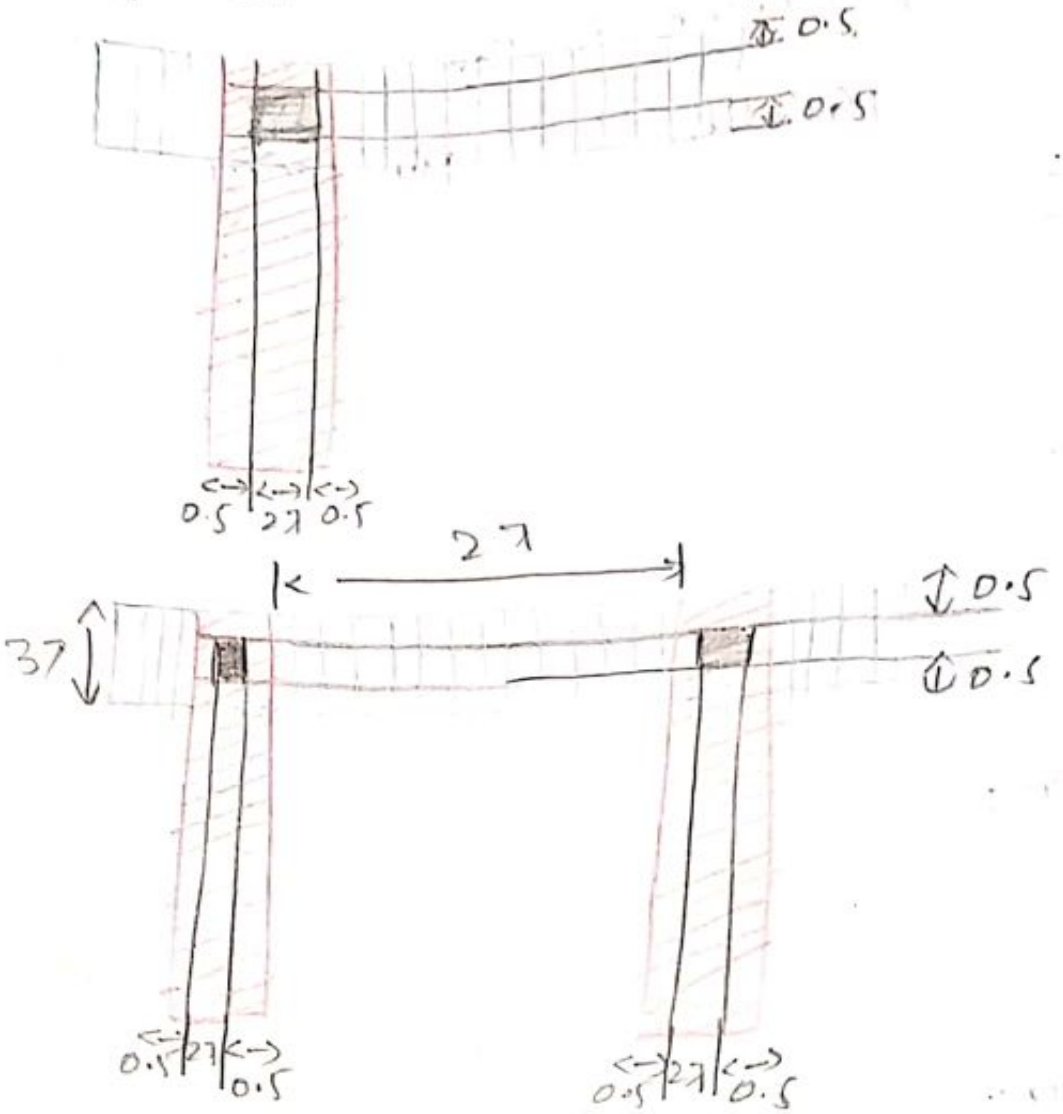


poly silicon:



n^+ diffusion:

Contact cut :-



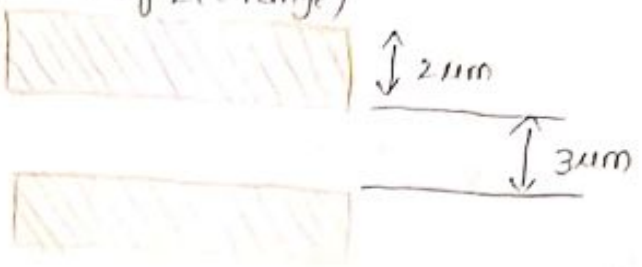
The spacing blw the polysilicon 1 & polysilicon 2 is 2λ.

Absolute Design Rules (Micron Base) :-

1. 2μm and 2.5μm (Double metal ; Double poly) :-
cmos, bicmos processes

Minwidth	Minspacing

Poly 2 (orange)

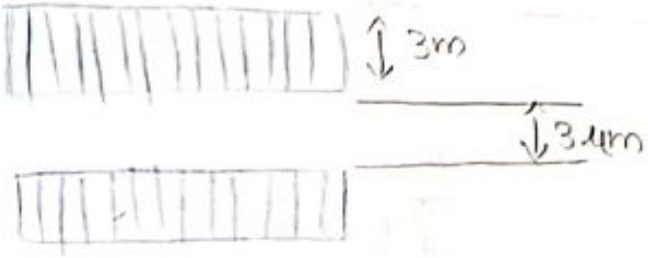


$P^+/n^+ \rightarrow P_1 \rightarrow 1\mu m$

$P^+/n^+ \rightarrow P_2 \rightarrow 1.5\mu m$

$P_1 \rightarrow P_2 \rightarrow 2\mu m$

Metal 2



$P_1 m_1$

$P_1 \rightarrow 2\mu m$ & $2.5\mu m$

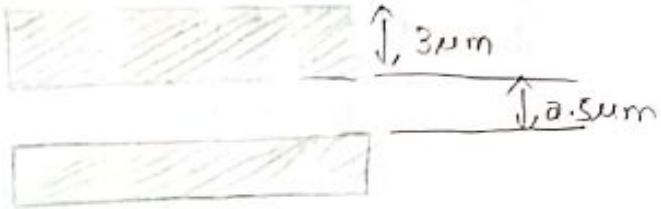
$m_1 \rightarrow 2\mu m$ & $2.5\mu m$

$P_2 \rightarrow 2\mu m$ & $3\mu m$

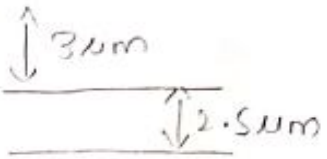
$m_2 \rightarrow 3\mu m, 3\mu m$

$P^+/n^+ \rightarrow 3\mu m$ & $2.5\mu m$

n^+ Diff



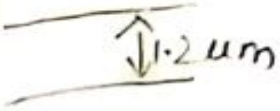
P^+ Diffusion

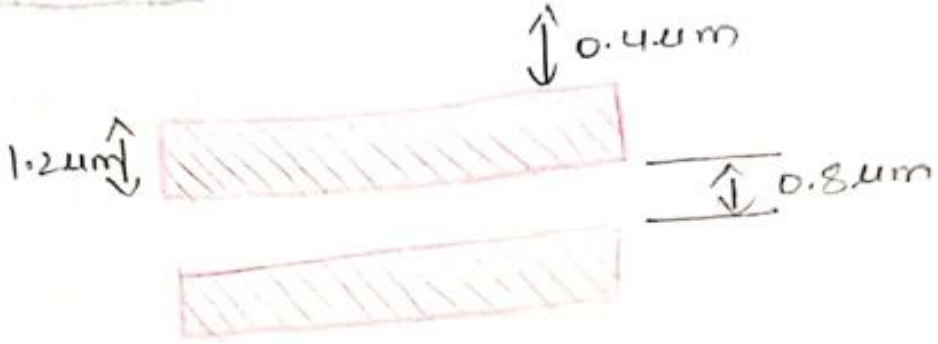


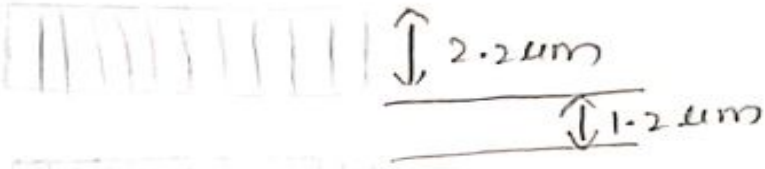
1.2um (Double metal and single poly):-

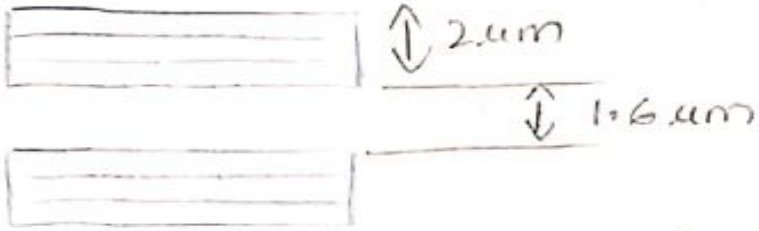
Minwidth

Minspacing

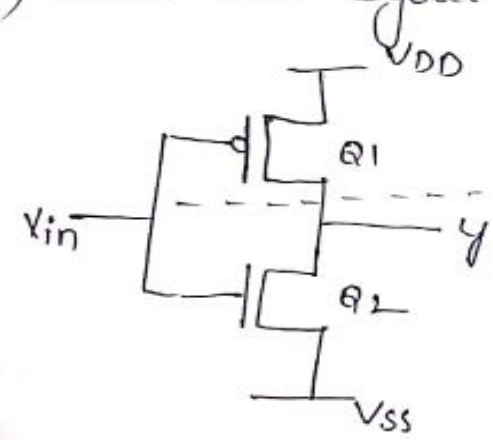


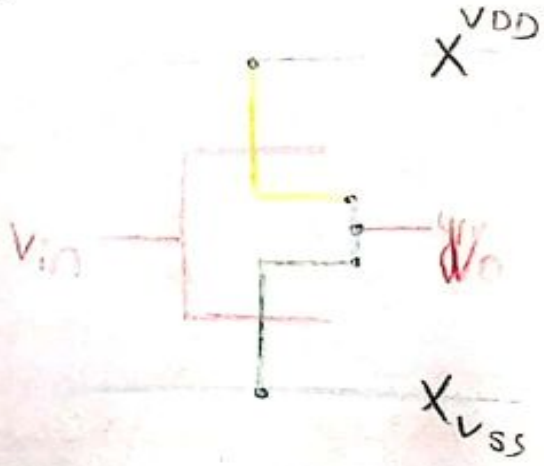






1) Draw the layout for Cmos inverter.

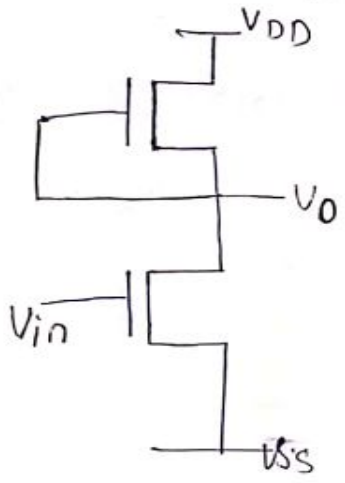


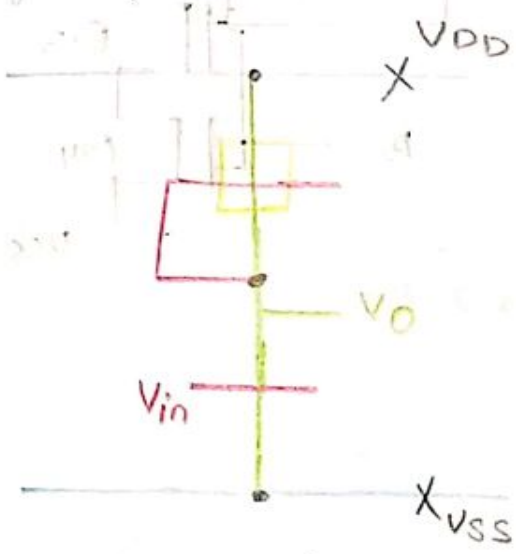


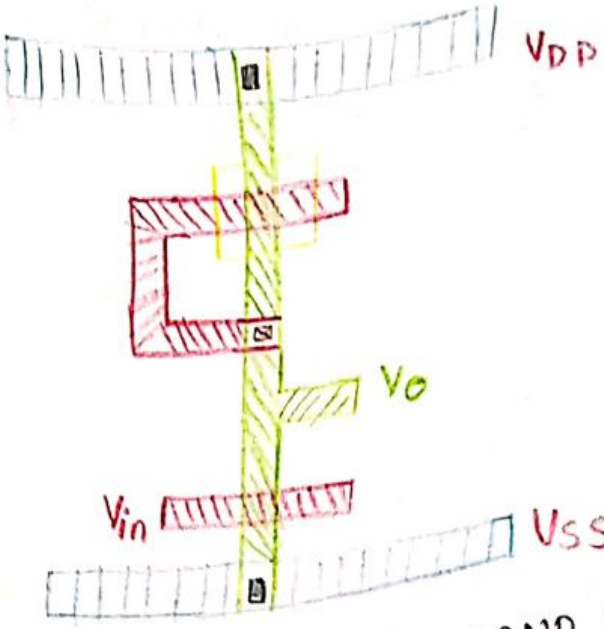
CMOS inverter ckt

2) Draw the layout for nmos inverter.

Nmos inveiter ckt

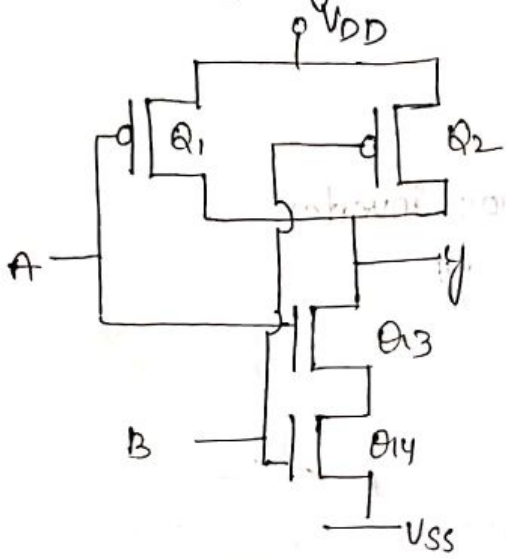




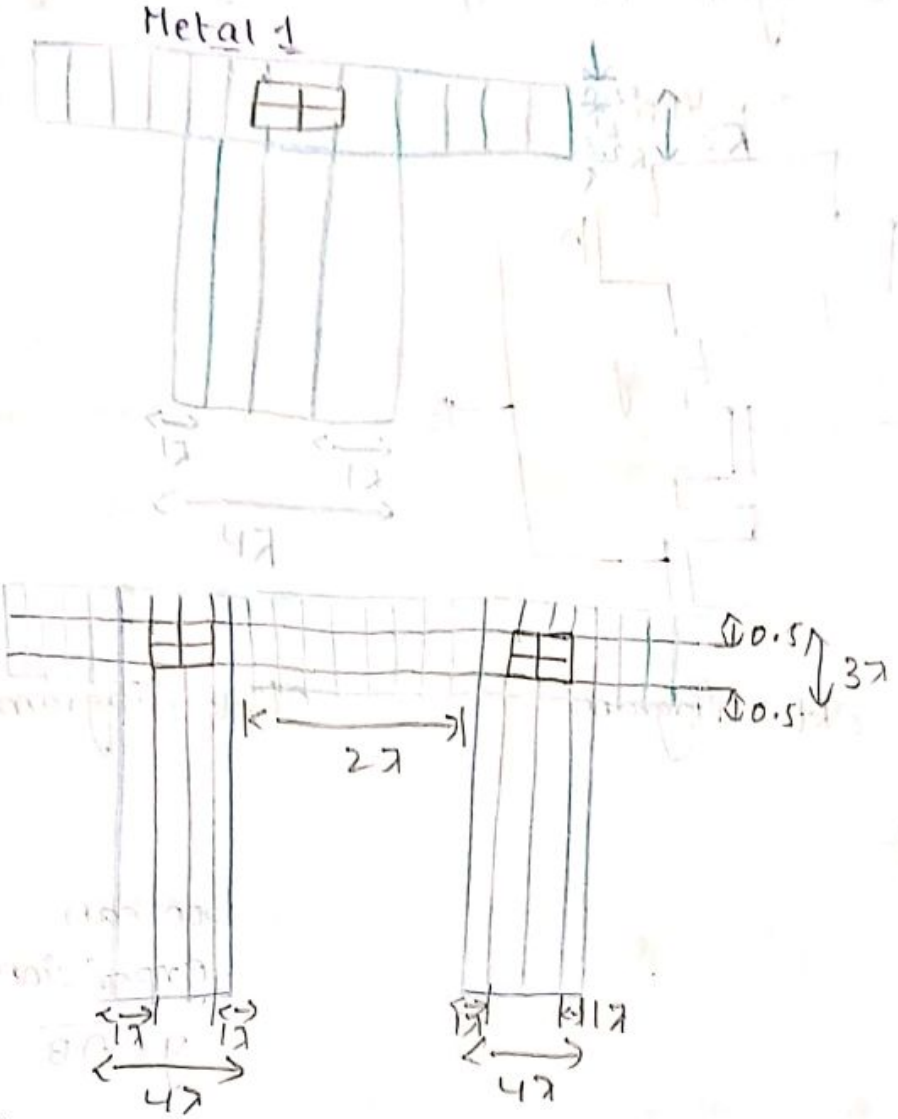


* Draw the layout for 2 i/p NAND gate using Cmos logic.

A. Circuit Diagram



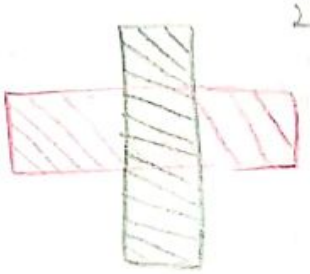
Via



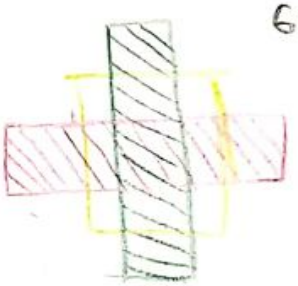
The spacing b/w via 1 & via 2 length is 2λ

Transistor representation:-

nmos enhancement

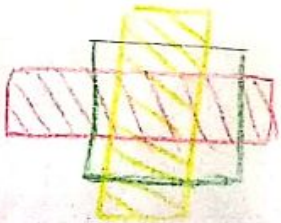


nmos Depletion

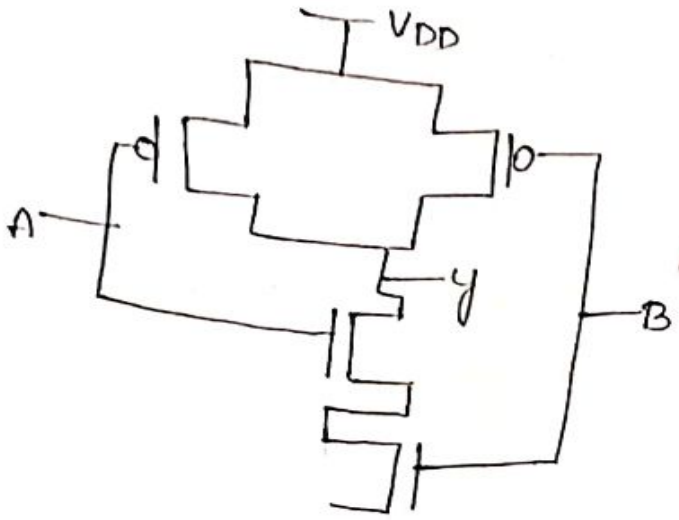


pmos enhancement

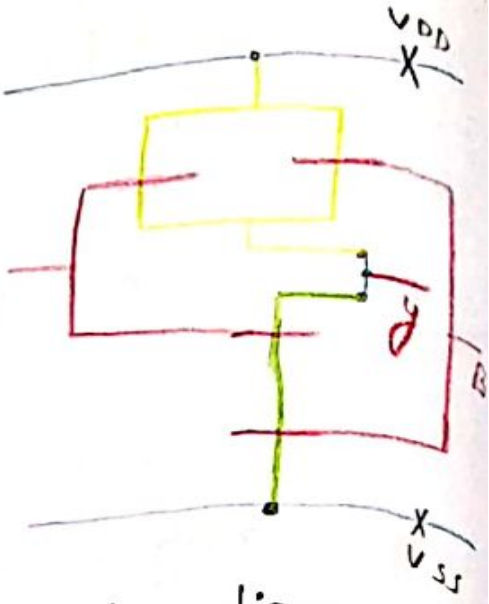
pmos depletion



* Draw the layout for 2 i/p NAND gate using cmos logic.

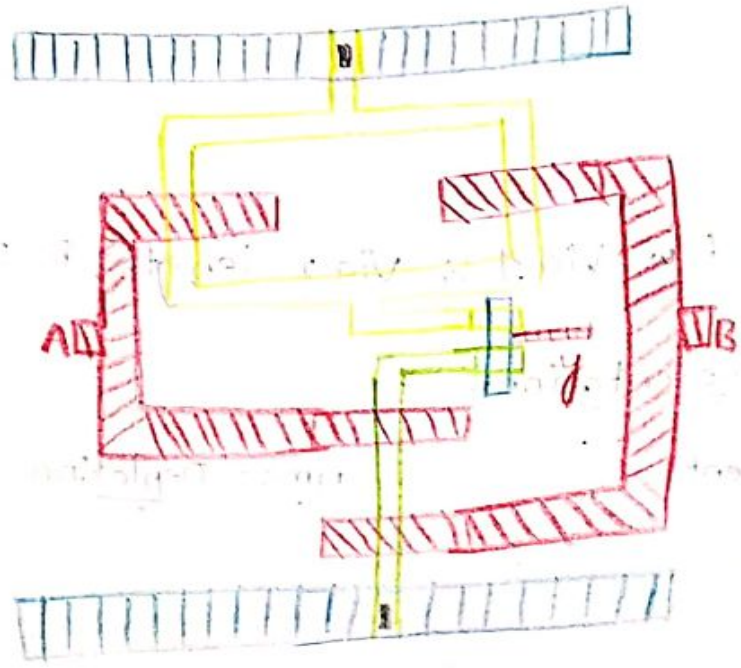


ckt diagram



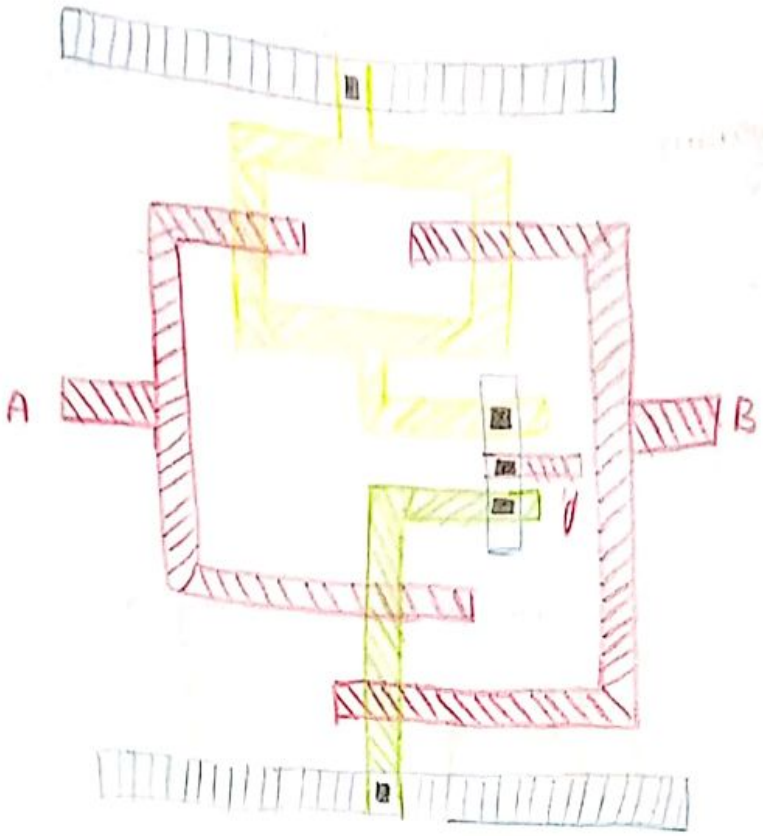
Stick diagram

layout



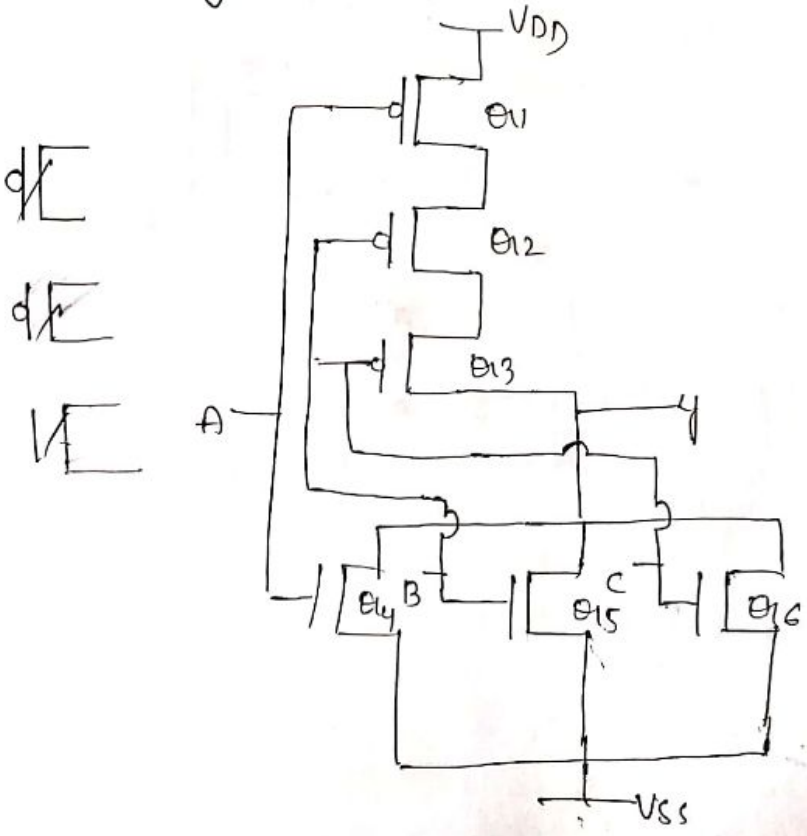
boolean expression

$y = \overline{AB}$



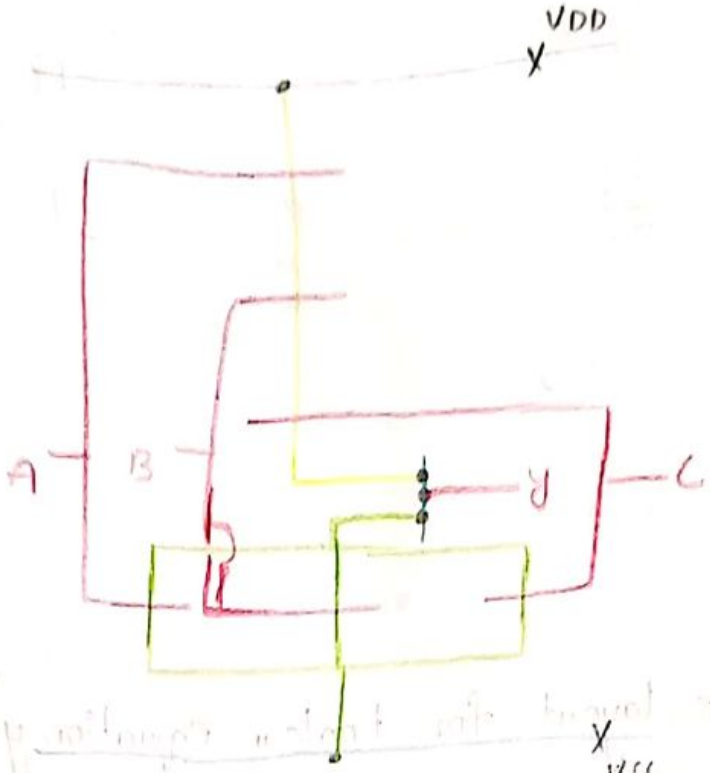
*Draw the layout for boolean equation $y=\overline{(A+B+C)}$ using cmos logic.

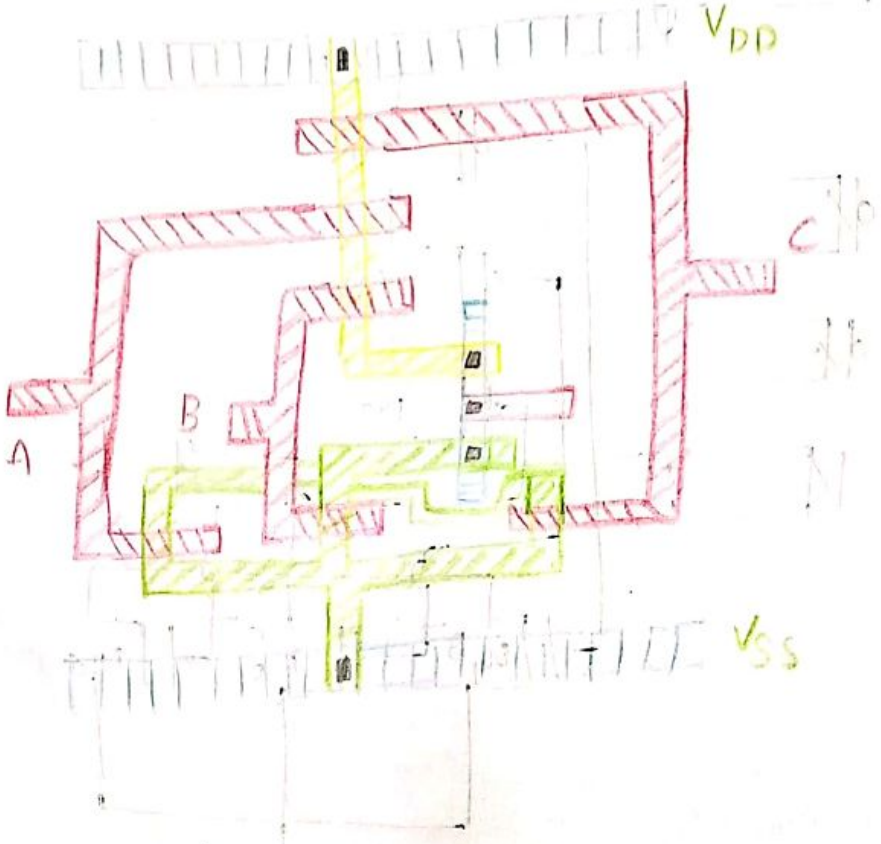
A. Circuit Diagram



General

Stick diagram

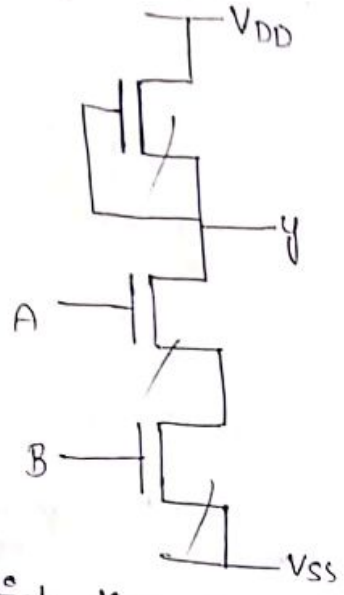


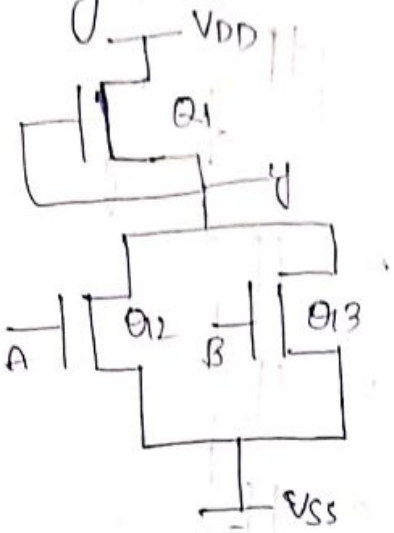


→ 2 i/p NOR gate using nmos logic → $y = \overline{(A+B)}$

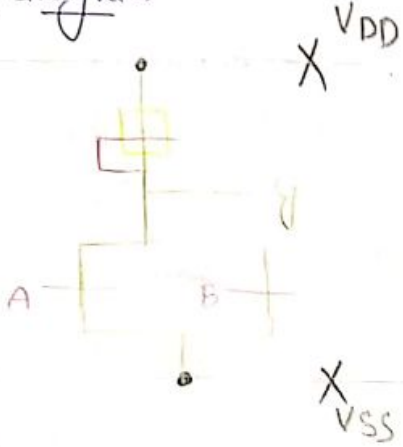
→ 3 i/p NAND gate using nmos logic → $y = \overline{ABC}$

1. 2 i/p NOR gate using nmos logic.

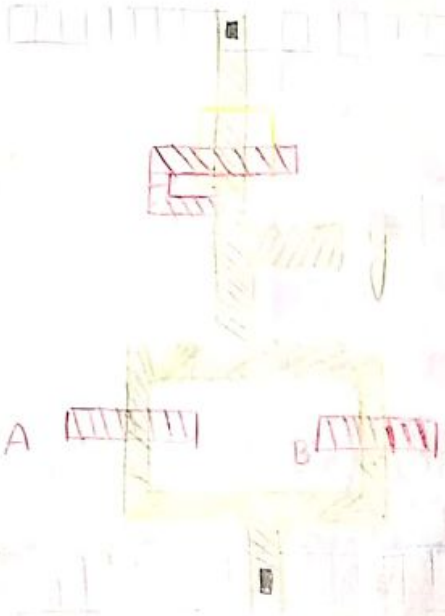




Stick diagram

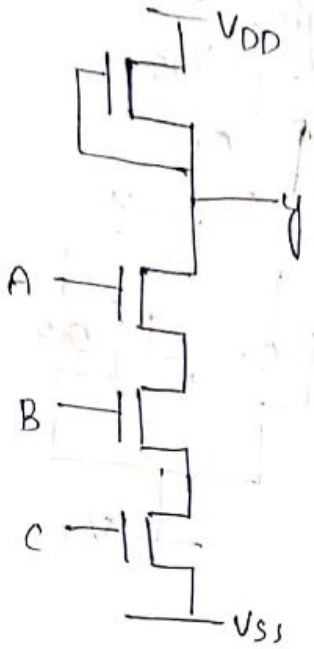


Layout

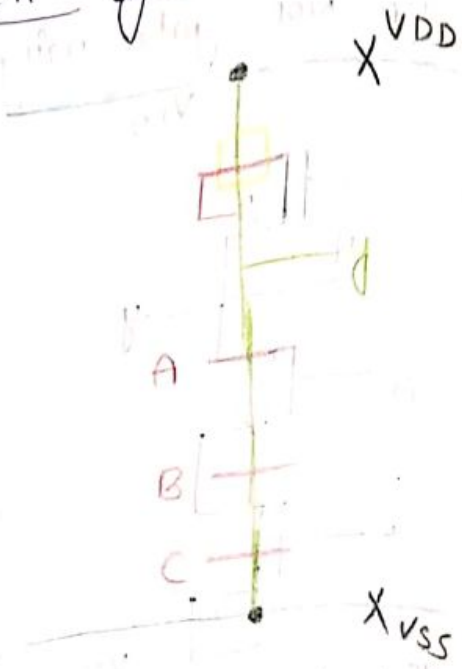


* 3i/p NAND gate using nmos logic. $y = \overline{ABC}$

Circuit diagram



Stick diagram



Layout

General observations for design rules:-

A VLSI designer is dealing with silicon circuits whose dimensions and features are extreamly microscopic in nature.

* If the line widths are to small, the lines so define may tend to be discontinuous case places (or) may accordingly merge at places.

* the main purpose of design rules are

1. provides Communication links between circuit designer and process Engineer responsible for fabrication.
2. The goal of any set of design rules should be optimise yield while keeping the geometry as small as possible without Compromising the realibity of the finished Circuit.
3. Try to exculed poly from the areas of p+mask/ n+ mask that may Effect the resistance of poly at certain paths.
4. Metal is depoisted at the top of all oxide layers, Since it is light reflective, these factors combine poor edge defination.
5. Metal 2 is having even more unevent terriains on which to be depoisled and patterend. Hence metal 2 is wided than metal 1.
6. metal to metal seperation is also large and is brought above mainly by difficulties indefining metal edges.