STATE BOARD OF TECHNICAL EDUCATION & TRAINING::AP, VIJAYAWADA

DIPLOMA IN ELECTRONICS & COMMUNICATIO ENGG.

III SEMESTER

DIGITAL ELECTRONICS LAB (EC-308)

MANUAL (AS PER C-20 CURRICULUM)

1.0 INTRODUCTION

The Curriculum of Technical Education should invariably provide for knowledge, attitudes and skills required by the technicians /technologists in the country. In this context the laboratory courses form a vital portion in the entire curriculum of technician education. The laboratory courses shall therefore be so designed and delivered that they help the students acquire attitudes and motor skills that are essential to function effectively as technicians/technologists.

The planning, organization and implementation of lab courses need a detailed description of tasks to be performed by the students. Well thought out instructional objectives to a large extent give these descriptions. The analysis of tasks (by identifying the activities the students are expected to do) help prepare the objectives meticulously. In other words the objectives would be clearer, when the task analysis is done to spell out the sub tasks for each objective.

A survey of the practices currently followed in the technical/technician education shows an urgent need to plug in gaps in instructional procedures. The reasons for these gaps are ambiguity in the minds of the teachers regarding tasks to be performed, levels of competency to be achieved by the students and the weightage to be allocated for each task. This aids in scientific design of instructional plan (optimizing the resources, budgeting the time & content).

The task analysis, teaching points and the structured scheme of evaluation are very important in focusing the instruction on specific skill of desired outcome and in evaluating the same. The Instruction and evaluation in Laboratory courses are different from that of cognitive lessons in the sense that adequate importance and hence weightage needs to be given for all three domains of learning viz. cognitive, psychomotor and affective. Since both training and evaluation of traits of affective domain are practically difficult, a few traits (called values) most relevant and essential to occupations/professions after the Course may be identified for the purpose. It is imperative to integrate these values during instruction and evaluation and also overtly notify the same to the students.

A technician, in addition to performing a skill needs to prepare a report of testing that includes the description of procedure, details of measurements made, reasoning based inferences and so on.,. The current practice of record writing has failed to achieve this purpose as most of the time students end up with making copies of available material.

Therefore, for sensitizing the need for the changes in laboratory instruction, the present hand book has been prepared to meet the above requirements. As such the hand book comprises four parts that intend to :

- Present task analysis, teaching points which can be used for effective design of instruction
- provide a scheme of evaluation with rationally allocated weightage to each significant skill component
- offer a set of questions designed at different levels of competencies for assessment enabling the teacher to set the question paper with balanced levels of competencies
- present pre set worksheets that cultivate the habit of systematic recording of observations and writing the technical report.
- Provide all important data related to particular laboratory activity at one point in the form of annexure

1.1. STRUCTURE OF THE BOOK

The hand book is presented in four parts viz., Laboratory sheets, Worksheet, Experimental Methodology and Annexure. The description of each part is given in the following sections

Part I. Laboratory Sheet

The information provided in this part is useful for the teacher for designing the instruction, planning & organization of the experiment and for scientific evaluation of the students. The major features of the Laboratory sheet are further explained below.

1. **Objective**

   It indicates the **Task** to be performed and completed by the student during the specified duration of time.

2. **Task Analysis**

It is the process of identifying the component activities (sub tasks) to be carried out by the student in order to achieve the stipulated objective. As the task analysis aim at fitting the instructional objectives into various classes of behaviour, it would help the teacher to determine any particular type of behaviour the student has learnt / failed to perform.

The task analysis would help the teacher in identifying the specific activities to be performed by the students. This could also be used as some kind of check list to compare with activities planned for the laboratory. Further it would give clue to the teacher to make students think originally & act independently. It includes both psychomotor learning and the related cognitive information and hence the task analysis is presented as Knowledge and skill parts.

A. Knowledge Part: That includes the cognitive aspects of the task.

B. Skill Part: That includes Psychomotor & Affective aspects of the task.

3. **Teaching Points:**

This includes the points based on the SKILL identified with suggested duration for each point and total duration which helps the teacher for the time and content budgeting during instruction.

4. **Need and Scope:**

The purpose, application and scope of the task to be performed are normally included in this sub section.

5. Planning and Organisation:

It lists actions to be taken to perform various activities and hence useful in planning the instruction and organizing the resources and equipment

6. **Scheme of Valuation:**

The information provided in this section helps the teacher to devise a tool for rational measurement assessment of the competencies accomplished by the student.

Part II. Work Sheet

It is designed for the student, where in the student enters his personal data of identification, details of the experiment, stepwise procedure, observations made during experiment, a sample calculation, free hand typical graph, graph from experimental data and inference with discussion.

Part III. Experimental Methodology

This section furnishes information with regard to standard procedure to conduct the experiment along with the description of equipment/apparatus and the basic theory/concept involved in the conduct of the experiment. Thus this section is very useful for both teacher and student as well to conduct the experiment systematically. Thus this section is presented in four sub section as described below:

- **Description**

  It gives the detailed description of apparatus / tools / equipment / materials to be used for the task.

- **Theory / Concept**

  It gives the concept of the task to be performed with formulae and units.

- **Procedure**

  It provides the idea of step wise procedure to perform the task.

- **Observation and Calculation**

  It includes sample observation, sample graph, sample calculation for reference

Part IV. Annexure

All important and useful information that may help in accomplishment of tasks like conversion tables for units, technical & scientific data like material properities, standard trend or characteristic curves (graphs) etc are compiled and presented at one place in this section.

1.2. WHO IS TO USE AND HOW TO USE.

The hand book is so designed that it can be beneficially used by different sections of the technical education viz., the teacher, the student, the examiner and the administrator convenient to individual's requirements. A few uses of this hand book each stakeholder could make is outlined in the following sections.

1. Teacher

A. The **laboratory sheet** is designed keeping the teacher in mind for the teacher has key responsibility of imparting the skills to the student and hence the information given in the lab sheets may be useful for planning & organizing the experimental set up and designing an effective instruction. Thus the teacher may

Plan and organize as per *section 4*,

Instruct the students as per *section 2***,**

Demonstrate each sub task as per *section1.B*.and

Evaluate the students as per *section 5***,** according to the level of competency.

Values: The values in a person are an important personality trait that needs to be nurtured in the learning environment. Further it is also a driving component in any individual to deliver the best and hence this component is also included in the evaluation. However only five key dimensions, that are important in the teaching-learning environment, are taken into consideration for nurturing and evaluation. A little information about these five dimensions is given below as a guideline for the teacher while assessing students.

1. Co-operation: It is the voluntary arrangement in which two or more students engage in a mutually beneficial exchange, instead of competition. Cooperation can happen where resources adequate for both students exist or are created by their interaction.

2. Co-ordination: It is the unification, integration, synchronization of the effect of group members so as provide unity of action in the pursuit of common goals. It is an integral element and required in each & every function and at each & every stage & therefore it cannot be separated.

3. Communication; Communication skill is the set of skills that enables a student to convey information so that it is received and understood.

4. Sharing: A part or portion belonging to, distributed to, contributed by, owed by a person or a group **Or** To participate in, use, enjoy or experience jointly or in turns.

5. Leadership: Students with the following leadership qualities are almost always the ones that rise above the crowd.

1. Trustworthiness: This refers to integrity.

2. Inspiration: Guides, leads and inspiring others to want to participate in the process of moving towards the vision.

3. Self awareness: It is the individual awareness of him or her self – their abilities and the impact that they have on others.

4. Acceptance of responsibility: True leaders are accepting responsibility for all that comes their way and taking ownership and responsibilities for getting things back on track. Blaming, justifying and excuse making just is not in their responsibility.

B. The **Experimental methodology** is designed for both teacher and student. The teacher can refer the experimental methodology for the details of equipment/apparatus/ materials/tools, procedure to be followed, observations to be made, graphs to be drawn and calculations to be done for the task to be performed

2. Student

The Worksheet is designed keeping in view the needs, deficiencies and the adolescent characteristics of the student for student.

The students submit the filled in work sheet given by the teacher on the day of experiment after referring to experimental methodology and listening to instructions of teacher. The design of the worksheet is made user friendly and the contents are so logically sequenced that the student finds it easy to understand and develop the skill of recording and report writing skill. It also helps the student to actively participate in skill learning. More importantly the student gets immediate meaningful feedback of his performance since the competency wise assessment is done and that too on the same day.

3. Examiner

The examiner may find this hand book very useful as Laboratory sheets and Scheme of evaluation provides information with regard to various competencies (skills) the students is expected to acquire during the course of study and the relative weightages of each competency. This information helps him to design a well balance question paper/measurement tool for assessment.

LOGIC GATES

1. OBJECTIVE

To verify the truth tables of AND, OR, NOT NAND, NOR, XOR Gates.

2. APPARATUS

1. Digital IC trainer kit
2. ICs 74LS00, 74LS02, 74LS04, 74LS08, 74LS32, 74LS86
3. Breadboard
4. Connecting wires

3. TASK ANALYSIS

A. KNOWLEDGE

1. Definition of logic gates, Basic gates and Universal gates
2. IC names and pin configuration of ICs
3. Truth tables of basic gates and universal gates
4. Applications of logic gates
5. Precautions

B. SKILL

Category of skill	Sub task
Handling of Apparatus	• Identifying the various ICs • Identifying the pins of ICs • Selecting the correct ICs for various functions • Identifying the connection points on the kit • Testing of IC working condition
Manipulation of Apparatus	• Making the connections as per the circuit diagram • Connect the inputs to correct pins of ICs • keeping all the inputs must be low • Checking the connections • Switching on the power supply • Varying the inputs HIGH or LOW as
Precise Activities of operations	• Applying the proper logic input signals • Observing the outputs for different inputs • Interpreting the logic levels for output

4. TEACHING POINTS

S.NO	TEACHING POINT	SUGGESTTED TIME-15min
1	Definition of logic gate, basic and universal gates	2
2	ICs for different logic gates	2
3	Pin configuration of different ICs	2
4	Truth table & logic for all logic gates	4
5	Truth tables of all logic gates	5

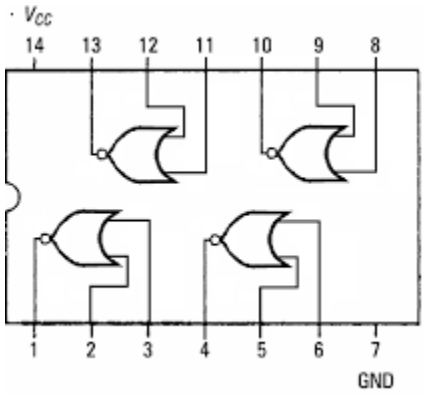
5. PRECAUTIONS

1. Disconnect all the Equipment from Mains before giving connections
2. Ensure Correct ICs were chosen.
3. ICs are to be inserted with great care.
4. Loose connections should be avoided
5. Power supply for ICs should be 5V DC.
6. Switch ON the supply after checking the connections.

6. SCHEME OF EVALUATION

<table>
<tr><th>CATEGORY OF SKILL</th><th>SUB TASK</th><th>WEIGHTAGE WITH COMPETENCY LEVEL INDIVIDUALLY</th><th>TOTAL</th></tr>
<tr><td>Handling of Apparatus</td><td>A. Identifying the various ICs
B. Identifying the pins of ICs
C. Selecting the correct ICs
D. Identifying the connection points on the kit
E. Testing of IC working condition</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>D</td><td>E</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr></table></td><td>5</td></tr>
<tr><td>Manipulation of Apparatus</td><td>A. Making the connections as per the circuit diagram
B. Connect the inputs to correct pins of ICs
C. Checking the connections
D. Keeping all the inputs low
E. Varying the inputs HIGH or LOW as</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>D</td><td>E</td></tr><tr><td>5</td><td>5</td><td>2</td><td>1</td><td>2</td></tr></table></td><td>15</td></tr>
<tr><td>Precise Activities /operations</td><td>A. Applying the proper logic input signals
B. Observing the outputs for different inputs
C. Interpret the logic levels for output</td><td><table><tr><td>A</td><td>B</td><td>C</td></tr><tr><td>5</td><td>10</td><td>10</td></tr></table></td><td>25</td></tr>
<tr><td>Values</td><td>A. Co operation
B. Co-ordination
C. Communication
D. Sharing
E. leadership</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>D</td><td>E</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr></table></td><td>5</td></tr>
</table>

7. ASSESSMENT QUESTIONS
   1. Draw the logic diagram of NOT gate using NAND gate?(middle order)
   2. connect AND gate using universal gates?(middle order)
   3. Identify the different pins of IC 7400(lower order)
   4. Draw the truth table of NOR gate(middle order)
   5. Observe the outputs of OR gate(higher order)
   6 .Observe the output for the given circuit(higher order)



8. VIVA QUESTIONS
   1. Why the NAND and NOR gates are called as universal gates
   2. What happens when only one input is given to the both the inputs of NAND gate
   3. What happens when one of the input of AND gate is connected to 1 and another input is connected to the clock
   4. Which gate will have high or 1 at its output when any one of its input is high
   5. How many NOT circuits are contained in IC 74LS04
   6. Write the Boolean expression for NOR gate

REALISATION OF AND, OR , NOT and XOR GATES USING 2 INPUT NAND GATES

1. Objective: To implement basic gates using NAND gates and verify their truth tables.
2. Apparatus: IC 7400, Digital logic trainer kit, connecting wires.
3. Task analysis:
   A. Knowledge
      1. Basic gates
      2. DeMorgan's theorem
      3. AND gate and its truth table
      4. OR gate and its truth table.
      5. NOT gate and its truth table
      6. Pin configuration of IC 7400(NAND gate)
      7. Construction of basic gates using IC 7400

   B. Skill

Category of Skill	Sub task
1. Handling of apparatus	• Identifying components • Identifying the PINs of ICs • Identifying the connection points on the kit
2. Manipulation of apparatus	• Testing ICs using digital IC tester • Connecting the circuit • Handling ICs
3. Precise activities	• Feeding the logic signals from the logic input switches. • Observing the logic outputs on the logic level LED indicators.

4. Teaching Points:

S. No	Teaching Point	Time allocation
1	Basic gates	5 min
2	DeMorgan's theorem	
3	AND logic operation	3 min
4	OR logic operation	
5	NOT logic operation	
6	Pin configuration of IC 7400(NAND gate)	2 min
7	Construction of basic gates using IC 7400	5 min

5. Precautions:

1. Disconnect all the Equipment from Mains before giving connections
2. Ensure Correct ICs were chosen.
3. ICs are to be inserted with great care.
4. Loose connections should be avoided
5. Power supply for ICs should be 5V DC.
6. Before turning ON the power to the trainer review the wiring for errors

7. Scheme of Evaluation

<table>
<tr><th>Category of Skill</th><th>Sub task</th><th>Weightage with Competency level Individually</th><th>Total</th></tr>
<tr><td>1.Handling of apparatus</td><td>A. Identifying components
B. Identifying the PINs of ICs
C. Identifying the connection points on the kit</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>T</td></tr><tr><td>2</td><td>2</td><td>1</td><td>5</td></tr></table></td><td>5</td></tr>
<tr><td>2.Manipulation of apparatus</td><td>A. Handling ICs
B. Testing ICs
C. Connecting the circuit</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>T</td></tr><tr><td>5</td><td>5</td><td>10</td><td>20</td></tr></table></td><td>20</td></tr>
<tr><td>3.Precise activities</td><td>A. Applying proper logic input signals
B. Observing logic output and interpreting its logic level.</td><td><table><tr><td>A</td><td>B</td><td>T</td></tr><tr><td>10</td><td>10</td><td>20</td></tr></table></td><td>20</td></tr>
<tr><td>4.Values</td><td>A. Co-operation
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</table>

7. Assessment Questions

1. Draw the logic diagram for a two-input NAND gate using one 2-input OR and one NOT gate. Include the pin numbers on the gate inputs and outputs. **(Middle Order)**
2. Build the NAND gate circuit using the 7432 and 7404 ICs on the trainer. Toggle the inputs by using the Level Switches. **(Middle Order)**
3. Draw a circuit to prove Universality of NOR Gate **(Middle Order)**
4. Verify the Truth tables to prove Universality of NAND Gate **(Higher Order)**
5. Given connected circuit, fill the following tabulations.(**Higher Order)**

AND

A	B	Y=(AB)’
0	0	
0	1	
1	0	
1	1	

OR

A	B	Y=(A+B)’
0	0	
0	1	
1	0	
1	1	

8. Viva questions
    1. What happens when both the inputs are low for a NAND gate?
    2. How to place the IC on bread board?
    3. What happens when ground pin and supply pin connections are interchanged?
    4. How do you identify the given IC?
    5. What happens when one of the input pin is left unconnected?
    6. How do you test the IC whether it is working or not?
    7. What happens if you make the logic switches of inputs in off condition?

REALIZATION OF AND, OR, NOT, XOR Gates USING 2 INPUT NOR GATE

1. Objectives:

- To understand the behavior and demonstrate the operation of the NOR gate
- To demonstrate the universality of the NOR gate
- To build a combinational logic circuit using all NOR gates

2. Apparatus Required:

1. Digital Logic Trainer
2. NOR Gate IC 7402
3. Patch cords
4. Single Strand wires

3. Task Analysis

A. Knowledge

1. IC Number of NOR Gate
2. Truth tables of AND,OR, NOT Gates
3. PIN Configuration of NOR Gate IC
4. Working of NOR Gate
5. Precautions during Connections

B. Skill

Handling of Apparatus	• Identifying NOR Gate IC • Selecting NOR Gates in a Quad NOR IC • Testing IC using Digital IC Tester • Inserting the IC on Breadboard of Trainer • Selecting the required patch cords & wires
Manipulation of Apparatus	• Drawing the Circuit Diagram • Making the Connections as per the circuit diagram • Keeping all the data inputs to low • Switching ON the Power Supply • Varying the inputs to HIGH or LOW as required.
Precise Operations/ Activities	• Changing the logic signals from the input switches. • Observing the logic outputs on the LED indicators. • Noting the Logic outputs for corresponding Inputs.

4. Teaching Points:

Sl.No	Teaching Point	Suggested Time – 15 Min
1	IC Number of NOR Gate	1
2	Truth Tables of AND, OR,NOT Gates	3
3	PIN Configuration of NOR Gate IC	5
4	Working of NOR Gate	2
5	Breadboard Connections	2
6	Precautions during Connections	2

5. Precautions:

1. Disconnect all the Equipment from Mains before giving connections
2. Ensure Correct ICs were chosen.
3. ICs are to be inserted with great care.
4. Loose connections should be avoided
5. Power supply for ICs should be 5V DC.
6. Before turning ON the power to the trainer review the wiring for errors.

6. Scheme of Evaluation:

<table>
<tr><th>Category of Skill</th><th>Sub task</th><th>Weightage with Competency level Individually</th><th>Total</th></tr>
<tr><td>1.Handling of apparatus</td><td>A. Identifying NOR Gate IC
B. Selecting NOR Gates in a Quad NOR IC
C. Testing IC whether it is Good or Bad
D. Inserting the IC on Breadboard of Trainer
E. Selecting the required patch cords & wires</td><td><table><tr><th>A</th><th>B</th><th>C</th><th>D</th><th>E</th><th>T</th></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>5</td></tr></table></td><td>5</td></tr>
<tr><td>2.Manipulation of apparatus</td><td>A. Drawing the Circuit Diagram
B. Making the Connections as per circuit diagram
C. Keeping all the data inputs to low
D. Switching ON the Power Supply
E. Varying the inputs to HIGH or LOW as required.</td><td><table><tr><th>A</th><th>B</th><th>C</th><th>D</th><th>E</th><th>T</th></tr><tr><td>5</td><td>10</td><td>1</td><td>1</td><td>3</td><td>20</td></tr></table></td><td>20</td></tr>
<tr><td>3.Precise operations / activities</td><td>A. Applying proper logic input signals
B. Observing logic output and interpreting logic level.
C. Noting the Logic outputs for corresponding Inputs</td><td><table><tr><th>A</th><th>B</th><th>C</th><th>T</th></tr><tr><td>5</td><td>10</td><td>5</td><td>20</td></tr></table></td><td>20</td></tr>
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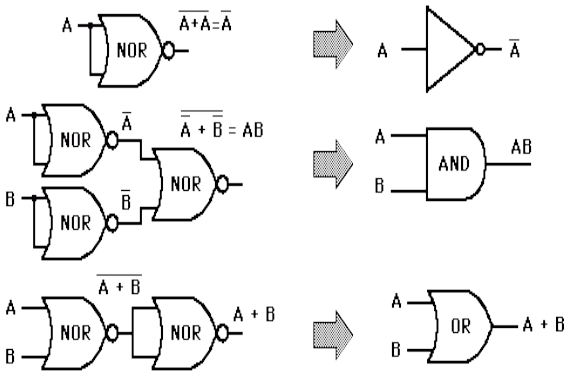
</table>

7. Assessment Questions:

1. Draw the logic diagram for a two-input NOR gate using one 2-input OR and one NOT gate. Include the pin numbers on the gate inputs and outputs. **(Middle Order)**
2. Build the NOR gate circuit using the 7432 and 7404 ICs on the trainer. Toggle the inputs by using the Level Switches. **(Middle Order)**
3. Draw a circuit to prove Universality of NOR Gate **(Middle Order)**
4. Verify the Truth tables to prove Universality of NOR Gate **(Higher Order)**
5. Construct the following circuit using only NOR Gates **(Middle Order)**



6. Given connected circuit, fill the following tabulations.(**Higher Order)**

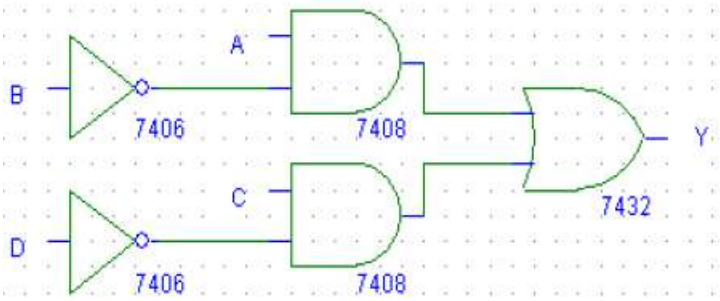
AND

A	B	Y=(AB)'
0	0	
0	1	
1	0	
1	1	

OR

A	B	Y=(A+B)'
0	0	
0	1	
1	0	
1	1	

8. Use the equivalent NOR gate logic to convert the logic diagram below to only contain NOR gates. Redraw the logic diagram with input/output labels. **(Higher Order)**



9. Viva Questions:

1. Why do we short the 2 input terminals of NOR while realizing NOT Gate?
2. What do you do, if results during the experiment do not match the theoretical or expected result?
3. Under what conditions the output of a 2- input AND gate will be one?
4. Can we use AND gate to realize OR Gate?
5. How do we complement the given input?
6. Does the use of 7425 (Dual 4-input NOR gate) in place of 7402 (quad 2-input NOR gate) IC increase or decrease no of ICs?
7. What happens if a power supply of more than +5V is given to any digital IC
8. Name the device/implement to test a given IC

EX-OR GATE USING NAND AND NOR GATES

OBJECTIVE**:** To implement the EX-OR gate using **NAND** and **NOR** gates.

APPARATUS**:** 7400 IC, 7402 IC, Digital Trainer kit, Patch cards.

1. TASK ANALYSIS

A. KNOWLEDGE

1. Universal gates
2. Symbols of gates
3. IC 7400, IC 7402 Pin diagrams
4. EX-OR Gate
5. Truth tables of gates
6. Boolean laws, Demorgan's theorem

B. SKILLS

Category of skill	Sub task
1. Handling of apparatus	• Identifying the IC's • Identification of pins of IC's • Identification of components in the trainer kit
2. Manipulation of apparatus	• Analysing the circuit diagram • Connecting the circuit inputs and outputs properly • Testing of IC's
3. Precise operations/activities	• Give the power supply to the circuit. • By applying the inputs to the circuit and observing the output • Verify the truth tables • Simplify the expressions

2. TEACHING POINTS

SI No	Teaching point	Time allocation (suggestive) 15 min
1.	Functions of NAND and NOR Gates	5 min
2.	Why NAND and NOR gates are called as universal gates	
3.	Function of EX-OR gate	
4.	Truth tables of gates	
4.	Boolean laws	5 min
5.	Demorgan's theorem	
6.	Designing EX-OR Gate using NAND Gate	
7.	Designing EX-OR Gate using NOR Gate	
8.	Applications of EX-OR Gate	2 min
9.	Make the connections according to the circuit diagram.	3 min
10.	The connections should be tight.	
11.	The Vcc and ground should be applied carefully at the specified pins only.	

3. SCHEME OF EVALUATION

<table>
<tr><th>CATEGORY OF SKILL</th><th>SUBTASK</th><th>WEIGHTAGE WITH COMPETENCY LEVEL INDIVIDUALLY</th><th>MARKS AWARDED</th></tr>
<tr><td>1. Handling of apparatus</td><td>A. Identification of IC’s
B. Pin description of IC’s
C. Identification of components in the trainer kit.</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>T</td></tr><tr><td>2</td><td>2</td><td>1</td><td>5</td></tr><tr><td></td><td></td><td></td><td></td></tr></table></td><td></td></tr>
<tr><td>2. Manipulation of apparatus</td><td>A. Drawing the circuit diagram
B. Circuit connections
C. Testing of IC’s</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>T</td></tr><tr><td>5</td><td>5</td><td>10</td><td>20</td></tr><tr><td></td><td></td><td></td><td></td></tr></table></td><td></td></tr>
<tr><td>3. Precise operations/activities</td><td>A. By applying the inputs to the circuit and observing the output
B. Verifying truth tables
C. Simplify the expressions
D. Symbols of gates</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>D</td><td>T</td></tr><tr><td>5</td><td>6</td><td>5</td><td>4</td><td>20</td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr></table></td><td></td></tr>
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C. Communication
D. Sharing
E. Leadership</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>D</td><td>E</td><td>T</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>5</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td></tr></table></td><td></td></tr>
<tr><td colspan="2"></td><td>Total</td><td></td></tr>
<tr><td colspan="3"></td><td>50</td></tr>
</table>

4. ASSESSMENT QUESTIONS

1. Perform an exercise to prove NAND & NOR gates are universal gates.
2. Realize the EX – OR gates using minimum number of NAND gates?
3. Give the truth table for EX-NOR (EX-OR+NOT) and realize using NAND gates.
4. Realize the given logic function using NAND gates?
   f = AB+AB+AB, verify the result by using IC.

5. VIVA-VOCE

1. Does EX-OR gate act as a buffer or inverter? Justify.
2. What happens if the output by connecting extra NAND gate at the output side of fig1?
3. How many minimal number of NAND gates are required to design EX-OR Gate.
4. How many minimal number of NOR gates are required to design EX-OR Gate.
5. Can you construct EX-OR gate without using NAND and NOR?
6. What happens to the output by connecting extra NOR gate at the output side of fig2?
7. What happens to the output when both inputs are short?
8. What happens to the output when one of the inputs is force to triggered clock signal with 1hz?

HALF ADDER AND FULL ADDER

OBJECTIVE: To design and construct the half adder, full adder and verify truth table using logic gates.

APPARATUS:

1. Digital IC Trainer Board
2. Patch chords/connecting wires
3. IC7408
4. IC7486
5. IC7432

1. TASK ANALYSIS

A) KNOWLEDGE:

1) Combinational circuits
2) Half adder and Full adder
3) Truth table for both combinational circuits
4) Understanding of K-Maps
5) Details of IC7408, IC7486, and IC7432

B) SKILL:

Category of Skill	Sub Task
Handling of apparatus	• Identifying the components required. • Identifying the pins of IC7408,IC7486 and IC 7432 • Identifying the input and output sections on the board.
Manipulation of apparatus	• Reading and understanding the circuit diagram. • Selecting channel on IC for connecting circuit. • Selecting appropriate inputs on the board to verify truth table. • Selecting appropriate outputs on the board to verify truth table.
Precise Operations/ Activities	• Drawing the circuit diagrams neatly. • Drawing the truth tables for Half adder and Full adder. • By changing the inputs to get all possible outputs. • Observing truth table for all cases.

2. TEACHING POINTS:

Sl. No	Teaching point	Time allocation (15 mins Suggestive)
1	Half adder	6 mins
2	Full adder	
3	K-map	4 mins
4	Details of ICs	5 mins
5	Precautions	

A. PRECAUTIONS:

- Disconnect all the equipment from mains before making connections.
- Connect the circuit as per circuit diagram.
- Loose connections should be avoided.
- Get the connections checked by the concerned staff member.
- Give required supply voltage to the circuit.

3. NEED AND SCOPE OF EXPERIMENT

- This experiment helps to understand the designing of Half adder and Full adder using EX-OR, AND & OR Logic Gates.
- It also helps to know the addition of two bits by Half adder and addition of three bits by Full adder.

4. PLANNING AND ORGANISATION:

ACTION	ACTIVITY
Check for	• Working of ICs • Loose Connections if any • Functioning of Input switches and output logical Indicators • Student entry behavior
For Design of Instruction	• Half adder and Full adder circuits must be known • Details of ICs must be known

5. SCHEME OF EVALUATION:

<table>
<tr><th>Category of Skill</th><th>SUB TASK</th><th>WEIHTAGE WITH COMPETENCY LEVEL INDIVIDUALLY</th><th>TOTAL (50)</th></tr>
<tr><td>1. Handling of apparatus</td><td>A) Identification of correct components.
B) Identification of input & output sections.</td><td><table><tr><th>A</th><th>B</th><th>T</th></tr><tr><td>3</td><td>2</td><td>5</td></tr></table></td><td>5</td></tr>
<tr><td>2. Manipulation of apparatus</td><td>A) Placement of components
B) Circuit connections.
C) Output Observations.</td><td><table><tr><th>A</th><th>B</th><th>C</th><th>T</th></tr><tr><td>5</td><td>5</td><td>10</td><td>20</td></tr></table></td><td>20</td></tr>
<tr><td>3. Precise Operations Activities</td><td>A) Identification of logic gates.
B) Verifying truth table.</td><td><table><tr><th>A</th><th>B</th><th>T</th></tr><tr><td>10</td><td>10</td><td>20</td></tr></table></td><td>20</td></tr>
<tr><td>4. Values</td><td>A) Co-operation
B) Co-ordination
C) Communication
D) Sharing
E) Leadership</td><td><table><tr><th>A</th><th>B</th><th>C</th><th>D</th><th>E</th><th>T</th></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>5</td></tr></table></td><td>5</td></tr>
</table>

6. ASSESSMENT QUESTIONS:

1. Identify the pins of IC 7408, IC 7486, IC 7432(Lower).
2. Identify the input and output sections on the kit(Lower).
3. Identify the Supply and Ground on the Kit (Lower).
4. Draw Full adder circuit diagram with two half adder circuits(Medium)?
5. Is it possible to design Full adder circuit with alternative ICs(Medium)?
6. How do you know the final result is correct (Higher)?
7. How can you get the result in the form of waveforms(Higher)?
8. How can you fix the the problem of erratic result if any(higher)?

7. VIVA QUESTIONS:

1. What happens if ground of IC is not connected?
2. What happens if supply voltage applied to IC is more than the rated voltage?
3. Suggest an alternative ICs for Half adder and Full adder?
4. What happens if clock signal is applied as one of the inputs for EX-OR Gate in Half adder?
5. What happens if two adjacent wires are short circuited when giving connections on bread board?
6. How can you design 4 bit adder with the same ICs that you used in Full Adder?
7. What happens if one broken wire was used during connecting the circuit diagram?
8. If A,B and C are the inputs of Full adder, then what would be its sum?
9. If A,B and C are the inputs of Full adder, then what would be its carry?
10. What happens to the output of Full adder when one of the three inputs is inverted ?

4-BIT MAGNITUDE COMPARATOR

2.7.1 OBJECTIVE: To verify the function of 4 bit magnitude comparator(IC 7485)

2.7.2 APPARATUS: 1.Comparator IC 7485
2. IC trainer kit
3. Patch cards

2.7.3 TASK ANALYSIS:

A) KNOWLEDGE :

1. What is an I.C
2. What is a comparator
3. What is M.S.B & L.S.B
4. Explain single bit comparator operation

B) SKILL:

CATEGORY OF SKILL	SUBTASK
1. HANDLING OF APPARATUS	• Identify the IC 7485 and major parts in the kit. (Like LEDs, Switches, Power supply) • Identify the test points in the kit
2. MANIPULATION OF APPARATUS	• Connect pin 16 to supply and pin 8 to ground • Connect the inputs and outputs as per the pin diagram • Connect the cascade input (A<B) and (A>B) to ground • Connect the cascade input (A=B) to Vcc
3. PRECISE OPERTAIONS/ ACTIVITIES	• Check the connections • Switch on the supply • Apply different input combinations • Interpreting the results with truth table

2.7.4 TEACHING POINTS:

S.No	TEACHING POINT	TIME ALLOCATION
1	Function of comparator	3 Min.
2	Truth table of 7485 IC	5 Min
3	IC pin diagram Explanation	5 Min
4	Precautions	2 Min

2.7.5 PRECAUTIONS:

1. Ensure that pin 16 connected to supply (5V)
2. Ensure pin 8 connected to ground
3. Avoid loose connections

2.7.6 SCHEME OF EVALUATION:

<table>
<tr><th>CATEGORY OF SKILL</th><th>SUB TASK</th><th>WEIGHTAGE WITH COMPETENCY LEVEL INDIVIDUALLY</th><th>TOTAL(50)</th></tr>
<tr><td>1.HANDLING OF APPARATUS</td><td>A. Identify the IC 7485 and major parts in the kit. (Like LEDs, Switches, Power supply)
B. Identify the test points in the kit</td><td><table><tr><td>A</td><td>B</td><td>T</td></tr><tr><td>3</td><td>2</td><td>5</td></tr><tr><td></td><td></td><td></td></tr></table></td><td>5</td></tr>
<tr><td>2.MANIPULATION OF APPARATUS</td><td>A. Connect pin 16 to supply and pin 8 to ground
B. Connect the inputs and outputs as per the pin diagram
C. Connect the cascade input (A<B) and (A>B) to ground
D. Connect the cascade input (A=B) to Vcc</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>D</td><td>T</td></tr><tr><td>4</td><td>4</td><td>6</td><td>6</td><td>20</td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr></table></td><td>20</td></tr>
<tr><td>3.PRECISE OPERTAIONS/ACTIVITIES</td><td>A. Check the connections
B. Switch on the supply
C. Apply different input combinations
D. Interpreting the results with truth table</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>D</td><td>T</td></tr><tr><td>2</td><td>2</td><td>6</td><td>10</td><td>20</td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr></table></td><td>20</td></tr>
<tr><td>4.Values</td><td>A. cooperation
B. coordination
C. communication
D. sharing
E. leadership</td><td><table><tr><td></td></tr><tr><td>5</td></tr></table></td><td>5</td></tr>
</table>

2.7.7 ASSESSMENT QUESTIONS:

1. Identify the major sections in trainer board and record the IC Nos., (Lower order)
2. Make connections as per circuit diagram of IC 7485 (Middle order)
3. Give the necessity of cascading inputs & pin diagrams of 7485 IC. (Higher order)
4. Verify the truth table of IC7485 (Higher order)
5. Check the voltage levels of Trainer kit (Higher order)

2.7.8 VIVA QUESTIONS:

1. What happens if the cascade inputs are not connected to supply or to the ground
2. What do you do if the IC 7485 is not working properly
3. What happens if the ground is not connected properly
4. How do you test the IC 7485

MULTIPLEXER

Objective : To verify truth table of Multiplexer using IC 74153

Apparatus Required : a) Digital Trainer Board,

b) Patch chords,

c) IC 74153

Task Analysis

A) Knowledge:

6) Multiplexing
7) Truth table of 4:1 MUX
8) Details of IC 74153

B) Skill :

Category of Skill	Sub Task
Handling of apparatus	• Identifying the components required. • Identifying the pins of IC74153. • Identifying the select, input and output sections on the board.
Manipulation of apparatus	• Reading the circuit diagram. • Selecting channel (A or B) on IC for connecting circuit. • Selecting appropriate input and select lines to verify truth table.
Precise Operations Activities	• Varying select lines to get all possible outputs. • Observing the outputs. • Observing all cases of truth table.

C) Teaching points:

Sl. No	Teaching point	Time allocation (15 mins Suggestive)
1	Multiplexing definition	5 mins
2	4:1 MUX Truth Table	5 mins
3	Details of IC 74153	5 mins
4	Precautions	

D) Scheme of Evaluation:

Category of Skill	Sub Task	Weightage with Competency Level Individually	TOTAL (50)
1. Handling of apparatus	C) Identification of correct components. D) Identification of select, input & output sections.	A: 3, B: 2, T: 5	5
2. Manipulation of apparatus	D) Circuit connections. E) Equipment handling.	A: 10, B: 5, T: 15	15
3. Precise Operations Activities	C) Varying Select lines & Enable inputs. D) Output Observations E) Verifying truth table.	A: 10, B: 10, C: 5, T: 25	25
4. Values	F) Co Operation G) Co- Ordination H) Communication I) Sharing J) Leadership	A: 1, B: 1, C: 1, D: 1, E: 1, T: 5	5

E) Assessment Questions:

1. Identify various sections in the trainer board. (Lower order)
2. Make connections as per the circuit diagram. (Middle order)
3. Verify the output for any one of the cases in accordance with the truth table. (Higher order)
4. What happens at the output (Z_B) if we give data lines to A channel and enable pin low in IC74153.
5. What happens if selection line pins (S_1 and S_0) are connected in opposite direction?

F) Viva Questions:

1. Why is MUX called as "Data Selector"? (Middle order)
2. What do you mean by Multiplexing? (Lower order)
3. What is Digital Multiplexer? (Lower order)
4. What is the function of Enable input to any IC? (Lower order)
5. How many 4:1 MUX are available on IC74153? (Lower order)
6. How many select lines are necessary for a 16:1 MUX? (Middle order)
7. What are the applications of Multiplexers? (Middle order)
8. How many 4:1 MUX are required to make 16:1 MUX? (Higher order)
9. What is the Boolean expression for a 2:1 MUX when S is a select line and A0 and A1 are input lines? (Middle order)
10. To perform Multiplexing enable pin should be connected to logic-0, Why is it so? (Higher order)

BCD TO SEVEN SEGMENT DECODER USING IC 7448

OBJECTIVE: To verify the truth table of BCD to Seven Segment Decoder.

APPARATUS: i) IC 7448,
ii) Seven Segment Display,
iii) IK Resistor,
iv) Digital trainer kit,
v) Power supply,
vi) Connecting wires.

1. TASK ANALYSIS:

A. KNOWLEDGE
1. IC 7448 pin diagram.
2. The idea of seven segment display
3. Truth table of Decoder and seven segment display.
4. Working of LED.

B. SKILL

CATEGORY OF SKILL	SUB TASK
1. Handling of apparatus	• Connecting of Input /Output pins of IC 7448 • Connecting of IC 7448to seven segment display through connecting wires • Power supply connections and GND connections
2. Manipulation of apparatus	• By applying different BCD inputs, the seven segment display is observed
3. Precise operations/Activities	• The seven segment display outputs are noted according to the decoder inputs.

2. TEACHING POINTS:

S. No	Teaching Point	Time allocation
1	Pin Diagram of IC 7448	3 min
2	Decoder outputs	2 min
3	Seven Segment Display	4 min
4	Circuit Diagram Connection	4 min
5	Precautions	2 min

3. PRECAUTIONS: 1.Circuit diagram is connected without loose connections.
2. Power supply is switched-off while connecting the circuit diagram.
3. Do not Power ON for long time as ICs may get damaged.

4. SCHEME OF EVALUATION

CATEGORY OF SKILL	SUB TASK	WEIGHTAGE WITH COMPETENCY LEVEL INDIVIDUALLY	TOTAL 50M
1.Handling of apparatus	a) Identification of components b) Identification of correct circuit c) Selecting proper wires	A: 2, B: 2, C: 1	5
2.Manipulation of apparatus	a) Placing the components b) Circuit connections	A: 5, B: 10	15
3.Precise activities	a) Identification of pin no of IC's b) Application of inputs c) Observation of outputs d) Tabulation of Input/output values	A: 10, B: 5, C: 5, D: 5	25
4.Values	a) Co-operation b) Co-ordination c) Communication d) Sharing e) Leadership	A: 1, B: 1, C: 1, D: 1, E: 1	5

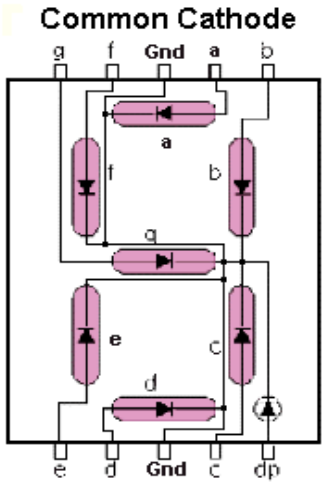
5. ASSESMENT QUESTIONS:

1. Identify various sections in the trainer board. (Lower order)

2. Make connection as per circuit diagram. (Middle order)

3. Verify the output by replacing 7448 with another IC. (Higher order).

4. Conduct the necessary exercise and state diodes in seven segment display are **ON,** when display 7 is shown as output? (Middle order)



5. Write the output by observing the LEDs (Lower order)

a	b	c	d	e	f	g	OUT PUT
OFF	ON	ON	OFF	OFF	ON	ON	?

6. Show the power PIN in IC7448. (Lower order).

5. VIVA QUESTIONS

1. How do you test IC is working or not?
2. Why do we place current limiting resistors?
3. How does the decoder works?
4. Function of seven segment display?
5. Identification of IC pins and their function?
6. Applications of seven segment display?
7. Different colors of LEDs and their purpose?

VERIFY THE TRUTH TABLE OF IC74138 DECODER

1. Objective: To Verify the Truth table of IC 74138 Decoder

2. Apparatus: IC 74138

Digital Trainer Kit with Bread board

Patch card

Power supply

3. Task Analysis:

A. Knowledge:

1. Study of Bread board
2. 3 To 8 Decoder
3. Need of Enable Input
4. Pin Diagram of IC 74138
5. Pin Description of IC 74138

B. Skills:

Categories of skills	Sub task
Handling of Apparatus	A. Identifying the components in the trainer kit B. Identifying the Pin configuration of IC
Manipulation of Apparatus	A. Drawing the logic circuit B. Connecting the logic circuit C. Appling the Enable inputs
Precise operations /Activities	A. Applying Inputs and Observe outputs B. Verify the truth table

4. Teaching Points:

S. No	Teaching point	Time allocation (suggestive) 15 min
1	Decoder	3 min
2	Types of decoder	
3	Enable inputs	
4	Pin diagram	5 min
5	Pin description	
6	Truth table	
7	Identify the different sections in trainer kit Power supply Ground Input logic levels Output logic (LED's)	4 min
8	Applications of decoder	3 min
9	Precautions to be taken while during the Experiment	

Precautions:

1. Ensure that IC 74138 Pin 14 connected to power supply.

2. Ensure that IC 74138 Pin 7 connected to ground.

3. Make connections in proper way.

4. Connect the circuit as per circuit diagram.

5. Loose connections should be avoided.

6. Get the connections checked by the concerned staff member.

5. Scheme of Evaluation:

<table>
<tr><th>Category of skill</th><th>Sub task</th><th>Weightage with computency level individuly</th><th>Marks Awarded</th></tr>
<tr><td>Handling of Apparatus</td><td>A. Identification of IC's
B. Identification of components in the kit</td><td><table><tr><td>A</td><td>B</td><td>T</td></tr><tr><td>2</td><td>3</td><td>5</td></tr></table></td><td></td></tr>
<tr><td>Manipulation of Apparatus</td><td>A. Drawing logic circuit
B. Connecting circuit
C. Appling enable input</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>T</td></tr><tr><td>3</td><td>10</td><td>2</td><td>15</td></tr></table></td><td></td></tr>
<tr><td>Precise operations/activities</td><td>A. Verifying the truth table by applying inputs.
B. Checking the enable inputs.</td><td><table><tr><td>A</td><td>B</td><td>T</td></tr><tr><td>15</td><td>10</td><td>25</td></tr></table></td><td></td></tr>
<tr><td>Values</td><td>A. Co operation
B. Co-ordination
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<tr><td colspan="3">Total</td><td>50</td></tr>
</table>

6. Assessment Questions:

1. Identify various pins in IC 74138? (Low order)

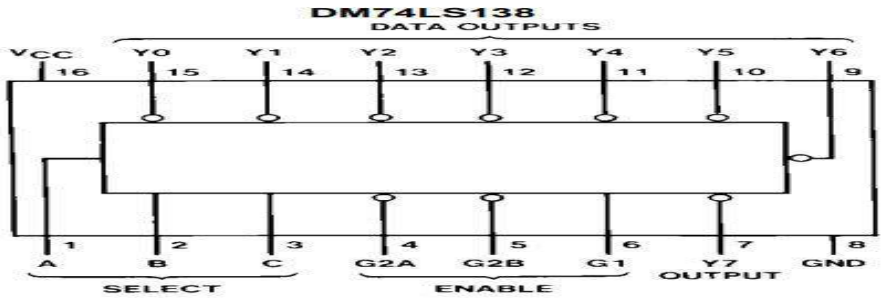
2. Identify major section in Trainer kit? (Low order)

3. Draw the logic diagram of 74138 IC? (Middle order)

4. Give the Enable input G_1 is low and G_{2A}, G_{2B} are X, X then by changing inputs what the outputs is? (Middle order)

G_1	G_{2A}	G_{2B}	A	B	C	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	X	X	X	X	X	?	?	?	?	?	?	?	?

5. Given a readily made circuit to verify truth table of IC 74138 Decoder? (Higher order)



G_1	G_{2A}	G_{2B}	A	B	C	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7

6. Design a De multiplexer circuit by using IC 74138? (Higher order)

7. Design a 3 to 8 Decoder, by change IC 74138 to IC 74156? (Higher order)

7. Viva Question:

1. What happens the Enable input G_1 is low and G_{2A},G_{2B} are X,X then by changing inputs what is the outputs?

2. Suggest the IC 74138 used for De multiplexer what are the connections?

3. What happens the Enable input G_1 is high and $G_{2A,}$ G_{2B} are low then by changing inputs what is the outputs?

4. What happen in 3 to 8 decoder IC 74138 changes to IC 74156?

Function of Encoder Using IC 74148

Objective: To verify the function of Encoder using IC 74148 with truth table

Apparatus: IC 74148, Digital Trainer kit, Bread board, Patch cords, power supply

1. Task Analysis

A.KNOWLEDGE

1. Study of Bread board
2. Encoder
3. Need of enable input
4. Pin diagram of IC 74148
5. Pin description of IC 74148
6. Truth table of encoder

B.SKILLS

Category of skill	Sub task
Handling of apparatus	• Identification of the IC • Identification of components in the trainer kit
Manipulation of apparatus	• Placement of components on breadboard • Circuit connections • Testing of IC
Precise operations/activities	• Identifying the pin numbers of IC • Verify the truth tables • Observing different logic states

2. Teaching Points

Sl No	Teaching point	Time allocation (suggestive) 15 min
1.	Encoder	3 min
2.	Types of encoder	
3.	Enable inputs	
4.	Pin diagram	5 min
4.	Pin description	
5.	Truth table	
6.	Identify the different sections in trainer kit Power supply Ground Input logic levels Output logic (LED's)	4 min
9.	Applications of encoder	3 min
10.	Precautions to be taken while during the experiment	

A. Procedural Precautions:

1. Ensure that pin 14 connected to supply.
2. Ensure that pin 7 connected to ground.
3. All connections should be made properly.
4. IC should not be reversed.

B. Safety precautions:

1. Power supply should not exceed 5V.
2. Never work on a circuit while power is applied.
3. Always keep your work area dry.

3. Need and Scope of Experiment

1. This experiment helps to understand the process of encoding.
2. Encoders are used to translate mechanical motion into a digital signal.

4. Scheme of Evaluation

<table>
<tr><th>CATEGORY OF SKILL</th><th>SUBTASK</th><th>WEIGHTAGE WITH COMPETENCY LEVEL INDIVIDUALLY</th><th>MARKS AWARDED</th></tr>
<tr><td>1. Handling of apparatus</td><td>A. Identification of IC 74148
B. Identification of components in the trainer kit.</td><td><table><tr><td>A</td><td>B</td><td>T</td></tr><tr><td>3</td><td>2</td><td>5</td></tr><tr><td></td><td></td><td></td></tr></table></td><td>5</td></tr>
<tr><td>2. Manipulation of apparatus</td><td>A. Placement of Components
B. Circuit connections
C. Testing of IC</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>T</td></tr><tr><td>5</td><td>5</td><td>10</td><td>20</td></tr><tr><td></td><td></td><td></td><td></td></tr></table></td><td>20</td></tr>
<tr><td>3. Precise operations/activities</td><td>A. Identifying pin numbers of IC’s
B. Verifying truth tables
C. Observing different logic states</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>T</td></tr><tr><td>5</td><td>5</td><td>10</td><td>20</td></tr><tr><td></td><td></td><td></td><td></td></tr></table></td><td>20</td></tr>
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<tr><td colspan="3">Total : 50</td><td>50</td></tr>
</table>

6. Assessment Questions

1. Identify the major sections in a digital trainer kit.
2. Make the connections as per the circuit diagram.
3. Verify the truth tables of encoder.
4. Identify the pin no. of enable inputs in the IC 74148.
5. Draw the logic circuit of 4*2 binary encoder.

7. Viva - Voce

1. What is the purpose of notch on IC?
2. How many pins are there in IC 74148?
3. What is the difference between encoder and decoder?
4. What happens if the enable pin is HIGH in IC 74148?
5. What is the purpose of GS pin in IC74148?
6. How many inputs are there for a 2^n*n encoder?
7. How many 4 * 2 encoders will be required to design a 8 * 3 encoder?
8. What are the applications of encoder?
9. If n=1, n=2, n=3 how many inputs and outputs for encoder?

Construct clocked RS FF using NAND gates and Verify its truth table

1. **OBJECTIVE:** Design and construct a clocked RS flip flop using NAND gates and Verify its Truth table.

2. **APPARATUS:** 7400 IC, Digital Trainer kit, Patch cards

3. **TASK ANALYSIS**

A.KNOWLEDGE

1. Latches ,NAND latch
2. Flip flops, Types of flip flops
3. RS Flip flop and its truth table
4. Need of clock
5. IC 7400 Pin diagram

B.SKILLS

Category of skill	Sub task
1. Handling of apparatus	• Identifying the IC's • Identifying pin numbers of IC's • Identification of components in the trainer kit
2. Manipulation of apparatus	• Analysing the circuit diagram • Connecting the circuit inputs and outputs properly • Testing of IC's
3. Precise operations/activities	• Give power supply to the circuit • By applying the inputs to the circuit and observing the output • Verify the truth tables • Observing different states

4. TEACHING POINTS

Sl No	Teaching point	Time allocation (suggestive) 15 min
1.	Latches and its types	5min
2.	Flip flops and its types	
3.	Difference between latch and flip flop	5 min
4.	RS Flip flop	
5.	Truth table of RS Flip flop	
6.	Need of clock	2 min
7.	Applications of flip flops	
9.	Make the connection s according to the circuit diagram.	3 min
10.	The connections should be tight.	
11.	The Vcc and ground should be applied carefully at the specified pins only	

5. SCHEME OF EVALUATION

<table>
<tr><th>CATEGORY OF SKILL</th><th>SUBTASK</th><th>WEIGHTAGE WITH COMPETENCY LEVEL INDIVIDUALLY</th><th>MARKS AWARDED</th></tr>
<tr><td>1. Handling of apparatus</td><td>F. Identification of IC’s
G. Identifying pin numbers of IC’s
H. Identification of components in the trainer kit.</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>T</td></tr><tr><td>2</td><td>2</td><td>1</td><td>5</td></tr><tr><td></td><td></td><td></td><td></td></tr></table></td><td></td></tr>
<tr><td>2. Manipulation of apparatus</td><td>G. Placement of components
H. Circuit connections
I. Testing of IC’s</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>T</td></tr><tr><td>5</td><td>5</td><td>10</td><td>20</td></tr><tr><td></td><td></td><td></td><td></td></tr></table></td><td></td></tr>
<tr><td>3. Precise operations/activities</td><td>H. By giving clock to the circuit from pulsar.
I. By applying inputs to the circuit and observe the outputs
J. Verifying truth tables
K. Observing different states</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>D</td><td>T</td></tr><tr><td>5</td><td>6</td><td>5</td><td>4</td><td>20</td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr></table></td><td></td></tr>
<tr><td>4. Values</td><td>K. Co operation
L. Co-Ordination
M. Communication
N. Sharing
O. Leadership</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>D</td><td>E</td><td>T</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>5</td></tr><tr><td></td><td></td><td></td><td></td><td></td><td></td></tr></table></td><td></td></tr>
<tr><td colspan="3">Total</td><td></td></tr>
<tr><td colspan="3"></td><td>50</td></tr>
</table>

6. ASSESSMENT QUESTIONS

1. Identify major sections on the Digital trainer Kit.
2. Draw the pin configuration of IC 7400?
3. Perform an exercise to find out the output for SR clocked flip flop if the values for S=0 and R=1, are given.
4. Perform an exercise to find out the output for SR clocked flip flop negative edge triggered clock of 1 H_z is given to the circuit?

7. VIVA - VOCE

1. What happens if a D Flip flop or inverter is placed at input of SR flip flop?
2. What happens when two AND gates are augmented with clocked SR flip flop?
3. How can we call a SR flip flop as a memory device?
4. What happens if both S and R are given 1 as input?
5. When RS flip-flop is said to be in a RESET state?
6. What happens when different frequency clock signal is given to a flip flop?
7. What may be the applications of flip flops?

JK FLIP FLOP USING IC 7476

1. **Objective** : To implement J K flip flop using 7476 and verify their truth tables.
2. **Apparatus** : IC 7476, Digital logic trainer kit, connecting wires.
3. **Task analysis**:

A. Knowledge

1. Truth table
2. Clock signal
3. J-K Flip flop and its truth table.
4. Pin configuration of IC 7476(J-K Flip Flop)

B. Skill:

Category of Skill	Sub task
1. Handling of apparatus	• Identifying components • Identifying the pins of ICs • Identifying the connection points on the kit
2. Manipulation of apparatus	• Testing ICs using digital IC tester • Connecting the circuit • Handling ICs
3. Precise activities	• Feeding the logic signals from the logic input switches. • Observing the logic outputs on the logic level LED indicators.

4. Teaching Points:

S. No	Teaching Point	Time allocation
1	Truth table	5 min
2	Clock signal	
3	J-K Flip flop and its truth table	10 min
4	Pin configuration of IC 7476(J-K Flip Flop)	

5. Scheme of Evaluation

<table>
<tr><th>Category of Skill</th><th>Sub task</th><th>Weightage with Competency level Individually</th><th>Total</th></tr>
<tr><td>1.Handling of apparatus</td><td>A. Identifying components
B. Identifying the pins of ICs
C. Identifying the connection points on the kit</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>T</td></tr><tr><td>2</td><td>2</td><td>1</td><td>5</td></tr></table></td><td>5</td></tr>
<tr><td>2.Manipulation of apparatus</td><td>A. Handling ICs
B. Testing ICs
C. Connecting the circuit</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>T</td></tr><tr><td>5</td><td>5</td><td>10</td><td>20</td></tr></table></td><td>20</td></tr>
<tr><td>3.Precise activities</td><td>A. Applying proper logic input signals
B. Observing logic output and interpreting its logic level.</td><td><table><tr><td>A</td><td>B</td><td>T</td></tr><tr><td>10</td><td>10</td><td>20</td></tr></table></td><td>20</td></tr>
<tr><td>4.Values</td><td>A. Co-operation
B. Co-ordination
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<tr><td colspan="3">TOTAL</td><td>50</td></tr>
</table>

6. Assessment Questions:

1. Identify various sections in the trainer board. (Lower order)
2. Make connections as per the circuit diagram. (Middle order)
3. Verify the output for any one of the cases in accordance with the truth table. (Higher order)

7. Viva questions

1. How can we differentiate latch and flip-flop
2. Where the flip-flops do are used.
3. How do we know the level triggering and edge triggering in flip-flops.
4. How can we identify whether it is +ve edge and -ve edge triggering.
5. Which type of edge triggering is used in IC 7476 J-K Flip-flop?
6. What happens when we give preset and clear inputs to the flip-flop and why are these Called asynchronous Inputs.
7. How can we identify toggle and write its significance
8. Where the D-FF's are used and why it is called a delay flip flop
9. Why JK FF is called as the universal flip flop.

D and T flip flops using IC 7476

1. **Objective**: To implement D and T flip flops using 7476 and verify their truth tables.
2. **Apparatus**: IC 7404, IC 7476, Digital logic trainer kit, connecting wires.
3. **Task analysis**:

A. Knowledge

1. Truth table
2. Clock signal
3. NOT gate and its truth table
4. J-K Flip flop and its truth table.
5. D Flip flop and its truth table.
6. T Flip flop and its truth table.
7. Pin configuration of IC 7404(NOT gate)
8. Pin configuration of IC 7476(J-K Flip Flop)
9. Conversion of JK Flip flop into D Flip flop
10. Conversion of JK Flip flop into T Flip flop

B. Skill

Category of Skill	Sub task
1. Handling of apparatus	• Identifying components • Identifying the pins of ICs • Identifying the connection points on the kit
2. Manipulation of apparatus	• Testing ICs using digital IC tester • Connecting the circuit • Handling ICs
3. Precise activities	• Feeding the logic signals from the logic input switches. • Observing the logic outputs on the logic level LED indicators.

4. Teaching Points:

S. No	Teaching Point	Time allocation
1	Truth table	5 min
2	Clock signal	
3	NOT gate and its truth table	
4	J-K Flip flop and its truth table	
5	D Flip flop and its truth table	5 min
6	T Flip flop and its truth table	
7	Pin configuration of IC 7404(NOT gate)	
8	Pin configuration of IC 7476(J-K Flip Flop)	
9	Conversion of JK Flip flop into T Flip flop	5 min
10	Conversion of JK Flip flop into D Flip flop	

4. Scheme of Evaluation

<table>
<tr><th>Category of Skill</th><th>Sub task</th><th>Weightage with Competency level Individually</th><th>Total</th></tr>
<tr><td>1.Handling of apparatus</td><td>A. Identifying components
B. Identifying the pins of ICs
C. Identifying the connection points on the kit</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>T</td></tr><tr><td>2</td><td>2</td><td>1</td><td>5</td></tr></table></td><td>5</td></tr>
<tr><td>2.Manipulation of apparatus</td><td>A. Handling ICs
B. Testing ICs
C. Connecting the circuit</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>T</td></tr><tr><td>5</td><td>5</td><td>10</td><td>20</td></tr></table></td><td>20</td></tr>
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<tr><td colspan="3">TOTAL</td><td>50</td></tr>
</table>

6. Assessment Questions:

1. Identify various sections in the trainer board. (Lower order)
2. Make connections as per the circuit diagram. (Middle order)
3. Verify the output for any one of the cases in accordance with the truth table. (Higher order)
4. What is the purpose of dual JK flip flop IC7476.

7. Viva questions

1. How can we differentiate latch and flip-flop.
2. Where the flip-flops do are used.
3. How do we know the level triggering and edge triggering in flip-flops.
4. How can we identify whether it is +ve edge and -ve edge triggering.
5. Which type of edge triggering is used in IC 7476 J-K Flip-flop?
6. What happens when we give preset and clear inputs to the flip-flop and why are these Called asynchronous Inputs.
7. How can we identify toggle state and write its significance.
8. Where the D-FF's are used and why it is called a delay flip flop.

RIPPLE COUNTER USING JK FLIP FLOP

OBJECTIVE : Construct a ripple counter using JK flip flop and Obtain its timing waveforms.

APPARATUS: 1. 7476 IC --- 2 no.

2. Digital Trainer Kit with Bread Board

3. Connecting wires

TASK ANALYSIS:

A. KNOWLEDGE

1. Pin description of 7476 IC
2. Truth table of JK flip flop
3. Logic diagram of ripple counter
4. Operation of ripple counter
5. Truth table of ripple counter
6. Precautions

B. SKILL

CATEGORY OF SKILL	SUB TASK
Handling of Apparatus	A. Identifying the components in the trainer kit B. Identifying the Pin configuration of IC C. Checking the IC
Manupulation of Apparatus	A. Drawing the Logic circuit B. Connecting the Logic circuit C. Applying the clock pulse
Precise operations/Activities	A. Observing the output after applying each pulse B. Obtain the timing waveforms

2. TEACHING POINTS

S.no	Teaching point	Suggest time 15 min.
1	Truth table of J K flip flop	3
2	Working of Ripple counter	5
3	Truth table of Ripple counter	3
4	Obtain the waveform	3
5	precautions	1

A. Procedural Precautions:

- Disconnect all the equipment from mains before making connections.
- Connect the circuit as per logic circuit
- Avoid the loose connections
- Get the required supply voltage to the circuit

3. Need and Scope of Experiment:

This experiment helps to understand construction and operation of ripple counter by using

JK flip flop

4. SCHEME OF EVALUATION

<table>
<tr><th>CATEGORY OF SKILL</th><th>SUB TASK</th><th>WEIGHTAGE WITH COMPETENCY LEVEL INDIVIDUALLY</th><th>TOTAL MARKS AWARDED</th></tr>
<tr><td>Handling of Apparatus</td><td>A. Identifying the components in the trainer kit
B. Identifying the Pin configuration of IC
C. Checking the IC</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>T</td></tr><tr><td>1</td><td>2</td><td>2</td><td>5</td></tr><tr><td></td><td></td><td></td><td></td></tr></table></td><td></td></tr>
<tr><td>Manupulation of Apparatus</td><td>A. Drawing the Logic circuit
B. Connecting the Logic circuit
C. Applying the clock pulse</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>T</td></tr><tr><td>4</td><td>10</td><td>1</td><td>15</td></tr><tr><td></td><td></td><td></td><td></td></tr></table></td><td></td></tr>
<tr><td>Precise operations/Activities</td><td>A. Observing the output after applying each pulse
B. Obtain the timing waveforms</td><td><table><tr><td>A</td><td>B</td><td>T</td></tr><tr><td>10</td><td>15</td><td>25</td></tr><tr><td></td><td></td><td></td></tr></table></td><td></td></tr>
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<tr><td colspan="3">TOTAL</td><td>50</td></tr>
</table>

ASSESSMENT QUESTIONS:

1. Identifying the components in the trainer kit. (lower order question)
2. What is the IC used for ripple counter ? (lower order question)
3. Connect the logic circuit and get the output 1110 by applying pulse input. (higher order question)
4. Connect the logic circuit for decade counter by using 7476 IC and AND GATE. (higher order question)
5. Construct the Ripple counter by using 7476 IC.(higher order question)
   Obtain the wave forms of ripple counter for –ve edge triggering. (middle order question)

VIVA QUESTIONS:

1. Why JK flipflop is used in ripple counter application, why not SR flipflop ?
2. Why do you apply logic 1 to J K inputs
3. What happened to the counter if you give preset input is low.
4. What happened to the counter if you give clear input is low.

DECADE COUNTER

1. Objectives:

1. To verify the function of 7490 as decade and modulus counter.
2. To obtain timing waveforms.

2. Apparatus Required:

1. Digital Logic Trainer
2. Decade Counter IC 7490
3. Breadboard
4. Patch cords
5. Single Strand wires

3. Task Analysis

A. Knowledge

1. IC Number of Decade counter
2. PIN Configuration of Decade counter
3. Truth tables of Decade counter
4. Working of Decade counter
5. Precautions during Connections

B. Skill

Handling of Apparatus	• Identifying Decade Counter IC • Identifying the pins of ICs • Testing IC using Digital IC Tester • Inserting the IC on Breadboard of Trainer • Selecting the required patch cords & wires
Manipulation of Apparatus	• Drawing the Circuit Diagram • Making the Connections as per the circuit diagram • keeping all the data inputs to low • Switching ON the Power Supply • Varying the inputs to HIGH or LOW as required.
Precise Operations/ Activities	• Changing the logic signals from the input switches. • Observing the logic outputs on the LED indicators. • Noting the Logic outputs for corresponding Inputs.

4. Teaching Points:

Sl.No	Teaching Point	Suggested Time – 15 Min
1	IC Numbers of Decade Counter	1
2	Count Truth table of Decade Counter	3
3	PIN Configuration of Decade Counter	5
4	Working of Decade Counter	2
5	Breadboard Connections	2
6	Precautions during Connections	2

5. Precautions:

1. Disconnect all the Equipment from Mains before giving connections
2. Ensure Correct IC was chosen.
3. IC has to be inserted with great care.
4. Loose connections should be avoided
5. Power supply for ICs should be 5V DC.
6. Switch ON the supply after checking the connections.

6. Scheme of Evaluation:

<table>
<tr><th>Category of Skill</th><th>Sub task</th><th>Weightage with Competency level Individually</th><th>Total</th></tr>
<tr><td>1.Handling of apparatus</td><td>A. Identifying Decade Counter IC
B. Identifying the pins of ICs
C. Testing IC whether it is Good or Bad
D. Inserting the IC on Breadboard of Trainer
E. Selecting the required patch cords & wires</td><td><table><tr><th>A</th><th>B</th><th>C</th><th>D</th><th>E</th><th>T</th></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>5</td></tr></table></td><td>5</td></tr>
<tr><td>2.Manipulation of apparatus</td><td>A. Drawing the Circuit Diagram
B. Making the Connections as per circuit diagram
C. Keeping all the data inputs to low
D. Switching ON the Power Supply
E. Varying the inputs to HIGH or LOW as required.</td><td><table><tr><th>A</th><th>B</th><th>C</th><th>D</th><th>E</th><th>T</th></tr><tr><td>5</td><td>10</td><td>1</td><td>1</td><td>3</td><td>20</td></tr></table></td><td>20</td></tr>
<tr><td>3.Precise operations / activities</td><td>A. Applying proper logic input signals
B. Observing logic output and interpreting logic level
C. Noting the Logic outputs for corresponding Inputs</td><td><table><tr><th>A</th><th>B</th><th>C</th><th>T</th></tr><tr><td>5</td><td>10</td><td>5</td><td>20</td></tr></table></td><td>20</td></tr>
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</table>

7. **Assessment Questions:**

1. Construct mod-5 counter using decade counter IC 7490.(higher order)
2. Construct mod-2 counter using decade counter IC 7490.(higher order)
3. Verify the functioning of IC 7490 as decade counter. (higher order)
4. Observe the timing waveforms of IC 7490.(higher order)
5. Draw the truth table of IC 7490 as decade counter.(middle order)
6. Identify different pins of IC 7490. (lower order)

8. Viva Questions:

1. How many flipflops are required to construct a decade counter?
2. How can a MOD-16 ripple counter be modified into a decade counter? Can you show it with diagram?
3. What are some devices/applications that uses decade counters?
4. Distinguish between synchronous and asynchronous decade counters.
5. How many different states does a decade counter have?

UP/DOWN COUNTER

OBJECTIVE: To verify the function of UP/DOWN counter using IC 74190/74193.

APPARATUS:

- Digital Trainer Board
- Patch chords
- IC 74190/74193
- Connecting wires(Optional)

TASK ANALYSIS

A) KNOWLEDE:

1) Clock pulse
2) Counter operation
3) Different types of Counters
4) Modulus of a counter

B) SKILL

Category of Skill	Sub Task
Handling of apparatus	• Identifying the components required. • Identifying the pins of IC 74190/ IC 74193. • Identifying the clock pulse, input and output sections on the board.
Manipulation of apparatus	• Reading the circuit diagram. • Selecting up/down and modulus of counter. • Supplying clock pulses. • Observing the outputs.
Precise Operations Activities	• Supplying clock pulses and observing counter stages. • Changing the mode and observing the counting procedure. • Changing the modulus and observing the counting procedure.

TEACHING POINTS:

Sl No.	Teaching point	Time allocation (15 mins Suggestive)
1	Clock Pulse	2 mins
2	Counter Operation	5 mins
3	Types of counters	
4	Modulus	5 mins
5	UP/DOWN mode	
6	Precautions	3 mins

SCHEME OF EVALUATION:

<table>
<tr><th>Category of Skill</th><th>SUB TASK</th><th>WEIHTAGE WITH COMPETENCY LEVEL INDIVIDUALLY</th><th>TOTAL (50)</th></tr>
<tr><td>1. Handling of apparatus</td><td>A) Identification of correct components.
B) Identification of control, clock, input & output sections.</td><td><table><tr><th>A</th><th>B</th><th>T</th></tr><tr><td>2</td><td>3</td><td>5</td></tr></table></td><td>5</td></tr>
<tr><td>2. Manipulation of apparatus</td><td>A) Placing the components
B) Circuit connections.
C) Output Observations.</td><td><table><tr><th>A</th><th>B</th><th>C</th><th>T</th></tr><tr><td>5</td><td>5</td><td>10</td><td>20</td></tr></table></td><td>20</td></tr>
<tr><td>3. Precise Operations Activities</td><td>A) Observing outputs after mode changing.
B) Observing outputs after modulus changing.</td><td><table><tr><th>A</th><th>B</th><th>T</th></tr><tr><td>10</td><td>10</td><td>20</td></tr></table></td><td>20</td></tr>
<tr><td>4. Values</td><td>A) Co Operation
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</table>

ASSESSMENT QUESTIONS:

1 Identify various sections in the trainer board. (Lower order)
2 Make connections as per the circuit diagram. (Middle order)
3 Verify the counting procedure in appropriate (UP or DOWN) mode. (Higher order)

VIVA QUESTIONS:

1. What is the difference between decade counter and 4 bit counter?
2. What is meant by a modulus of a counter?
3. How many Flip Flops are necessary to design a counter with mod-12?
4. Differentiate between synchronous and asynchronous counter?
5. When two counters are cascaded, what is the overall MOD number?
6. How many different states does a 3-bit asynchronous counter have?
7. What is the terminal count of a 3-bit binary counter in the DOWN mode?
8. What does $UP/\overline{DOWN}$ means?

SHIFT REGISTER

OBJECTIVE: To verify the function of shift register (ICs like 7495, 74194).

APPARATUS: IC 7495, Digital trainer kit, Patch cards, Power supply.

1. TASK ANALYSIS:

A. KNOWLEDGE

1) IC 7495 pin diagram.
2) Truth table of IC 7495.

B. SKILL

Category of Skill	Sub task
1. Handling of apparatus	• Identifying the input and output pins of IC 7495 • Identifying the power supply (Vcc) and GND connections.
2. Manipulation of apparatus	• Drawing the circuit diagram. • Making the connections as per circuit. • Connection of Input/output pins of IC 7495 for different modes (SIS0, SIP0, PISO and PIPO). • Checking the connections. • Switch on the supply.
3. Precise operations / Activities	• Applying the data inputs, control inputs and observing the shifting operation.

2. TEACHING POINTS

S. No	Teaching Point	Time allocation
1	Pin Diagram of IC 7495	5 min
2	Configuration of IC for different shifting modes.	10 min

3. PRECAUTIONS:

1. Circuit diagram is connected without loose connections.
2. Power supply is switched-off while connecting the circuit diagram
3. Do not Power ON for long time as ICs may get damaged.

4. SCHEME OF EVALUATION:

<table>
<tr><th>Category of Skill</th><th>Sub task</th><th>Weightage with Competency level Individually</th><th>Total</th></tr>
<tr><td>1.Handling of apparatus</td><td>A. Identifying the input and output pins of IC 7495
B. Identifying the power supply (Vcc) and GND connections.</td><td><table><tr><td>A</td><td>B</td><td>T</td></tr><tr><td>3</td><td>2</td><td>5</td></tr></table></td><td>5</td></tr>
<tr><td>2.Manipulation of apparatus</td><td>A. Placing the components on breadboard
B. Read IC pin diagram
C. Observations</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>T</td></tr><tr><td>8</td><td>10</td><td>5</td><td>20</td></tr></table></td><td>20</td></tr>
<tr><td>3.Precise activities and operations</td><td>A. IC connections for different modes(SISO,SIPO,PISO,PIPO) of shift register
B. Tabulation of values of truth table</td><td><table><tr><td>A</td><td>B</td><td>T</td></tr><tr><td>12</td><td>8</td><td>20</td></tr></table></td><td>20</td></tr>
<tr><td>4.Values</td><td>A. Co-operation
B. Co-ordination
C. Communication
D. Sharing
E. Leadership</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>D</td><td>E</td><td>T</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>5</td></tr></table></td><td>5</td></tr>
</table>

5. ASSESSMENT QUESTIONS:

1. Identify the serial, parallel input and output pins of IC 7495 (Lower level)
2. Draw the PIN diagram of IC 7495 shift register (Middle level)
3. Draw the truth table of shift register (Middle level)
4. Given the pin diagram of IC 7495, connect the IC 7495 in Parallel In Parallel Out (PIPO) mode (Higher Level)
5. Given the pin diagram of IC 7495, connect the IC 7495 in Parallel In Serial Out (PISO) mode (Higher Level)
6. Draw the PIN diagram of IC 7495, connect the IC 7495 in Serial In Parallel Out (SIPO) mode (Higher Level)
7. Draw the PIN diagram of IC 7495, connect the IC 7495 in Serial In Serial Out (SISO) mode (Higher Level)

6. VIVA QUESTIONS

1. How many clock pulses are needed to serially shift a nibble (four bits) of data into a shift register?
2. How many clock cycles are needed in order to have first output in SISO
3. How many clock cycles are needed in order to have all the outputs after feeding the inputs?
4. Mention the IC Numbers used for Shift Register

SIMULATION OF AND, OR, NOT USING 2 INPUT NOR GATE

1. Objectives:

1. To simulate AND, OR , NOT and EXOR Gates using NOR Gates
2. To verify the truth tables of AND, OR,NOT and EXOR Gates

2. Apparatus Required:

1. Personal Computer with Windows OS
2. ORCAD PSPICE 9.2 software package.

3. Task Analysis

A. Knowledge

1. IC Numbers of NOR Gate
2. Truth tables of AND,OR, NOT and EXOR Gates
3. PIN Configuration of NOR Gate IC
4. Working of NOR Gate

B. Skill

Handling of Apparatus	• Knowing how to invoke ORCAD Pspice application S/W • Opening a new project • Selecting proper project for digital simulation • Naming the project and finding the location to save the project • Adding the required libraries to simulate the project
Manipulation of Apparatus	A. Adding the required parts, input and output ports to the work space B. Wiring the circuit as per the circuit diagram C. Apply Pspice stimulus to all input ports as the truth table D. Creating the new simulation profile to the project
Precise Operations/ Activities	A. Running the project and adding input and output traces to the simulation graph B. Observing the output waveforms C. Interpreting the simulation results with truth tables D. Repeating same simulation with selection of proper time periods and ON time of inputs such that the output is clearly understood

4. Teaching Points:

Sl. No	Teaching Point	Suggested Time – 15 Min
1	IC Numbers of NOR Gate	1
2	Truth Tables of AND, OR,NOT Gates	3
3	PIN Configuration of NOR Gate IC	5
4	Working of NOR Gate	2
5	Working with ORCAD Pspice	2
6	Precautions during virtual wiring to avoid overlapping	2

5. Precautions:

1. Disconnect all the Equipment from Mains before giving connections
2. Ensure Correct ICs were chosen.
3. Input ports should be properly selected
4. Overlapping virtual wiring should be avoided
5. Traces should be properly selected

6. Scheme of Evaluation:

<table>
<tr><th>Category of Skill</th><th>Sub task</th><th>Weightage with Competency level Individually</th><th>Total</th></tr>
<tr><td>1.Handling of apparatus</td><td>A. Knowing how to invoke ORCAD Pspice application S/W
B. Opening a new project
C. Selecting proper project for digital simulation
D. Naming the project and finding the location to save the project
E. Adding the required libraries to simulate the project</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>D</td><td>E</td><td>T</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>5</td></tr></table></td><td>5</td></tr>
<tr><td>2.Manipulation of apparatus</td><td>A. Adding the required parts, input and output ports to the work space
B. Wiring the circuit as per the circuit diagram
C. Apply Pspice stimulus to all input ports as the truth table
D. Creating the new simulation profile to the project</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>D</td><td>T</td></tr><tr><td>5</td><td>5</td><td>5</td><td>5</td><td>20</td></tr></table></td><td>20</td></tr>
<tr><td>3.Precise operations / activities</td><td>A. Running the project and adding input and output traces to the simulation graph
B. Observing the output waveforms
C. Interpreting the simulation results with truth tables
D. Repeating same simulation with selection of proper time periods and ON time of inputs such that the output is clearly understood</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>D</td><td>T</td></tr><tr><td>5</td><td>5</td><td>5</td><td>5</td><td>20</td></tr></table></td><td>20</td></tr>
<tr><td>4.Values</td><td>A. Co-operation
B. Co-ordination
C. Communication
D. Sharing
E. Leadership</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>D</td><td>E</td><td>T</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>5</td></tr></table></td><td>5</td></tr>
</table>

7. Viva Questions:

1. Why do we short the 2 input terminals of NOR while realizing NOT Gate?
2. What do you do, if results during the experiment do not match the theoretical or expected result?
3. Under what conditions the output of a 2- input AND gate will be one?
4. Can we use AND gate to realize OR Gate? If Can't, why?
5. How do we complement the given input?
6. Does the use of 7425 (Dual 4-input NOR gate) in place of 7402 (quad 2-input NOR gate) IC increase or decrease no of ICs?
7. What happens if a power supply of more than +5V is given to any digital IC
8. Name the device/implement to test a given IC

HALF ADDER AND FULL ADDER

OBJECTIVE: To design and construct the half adder, full adder and verify truth table using ORCAD Pspice 9.2 software package.

APPARATUS: 1. Personal Computer.

2. OS of Winows 07/XP/10.
3. ORCAD Pspice 9.2 software package.

1. TASK ANALYSIS

A) KNOWLEDGE:

1) Combinational circuits.
2) Half adder and Full adder.
3) Truth table for both combinational circuits.
4) Understanding of K-Maps.
5) Details of IC7408, IC7486, and IC7432.

B) SKILL:

Category of Skill	Sub Task
Handling of Software	A. Knowing how to invoke ORCAD Pspice application S/W B. Opening project and saving the project in appropriate location. C. Selecting proper project for digital simulation. D. Adding the relevant libraries to simulate the project
Manipulation of Software	A. Adding the required parts,input and output ports in the workspace. B. Wiring the circuit as per the circuit diagram. C. Customising the label names of all the inputs and ouputs of logic gates. D. Creating the new simulation profile to the project
Precise Operations/ Activities	A. Running the project and adding input and output traces to the simulation graph B. Observing the output waveforms C. Interpreting the simulation results with truth tables D. Repeating same simulation with selection of proper time periods and ON time of inputs such that the output is clearly understood

3. TEACHING POINTS:

Sl. No	Teaching point	Time allocation (15 mins Suggestive)
1	Half adder	6 mins
2	Full adder	
3	K-map	4 mins
4	Details of ICs	5 mins
5	ORCAD Pspice software package	

4. PRECAUTIONS:

- Install the software by following the instructions carefully.
- Get the installation checked by the concerned staff member.

5. NEED AND SCOPE OF EXPERIMENT

- This experiment helps to understand the designing and implementation of Half adder and Full adder using ORCAD Pspice 9.2 software package.
- It also helps to know the addition of two bits by Half adder and addition of three bits by Full adder.

6. PLANNING AND ORGANISATION:

ACTION	ACTIVITY
Check for	• Working of ORCAD Pspice software package. • Working of Windows OS. • Functioning of Input switches and output logical Indicators • Student entry behavior
For Design of Instruction	• Half adder and Full adder circuits must be known. • ORCAD Pspice must be known.

5. SCHEME OF EVALUATION:

<table>
<tr><th>Category of Skill</th><th>SUB TASK</th><th>WEIHTAGE WITH COMPETENCY LEVEL INDIVIDUALLY</th><th>TOTAL (50)</th></tr>
<tr><td>1. Handling of Software</td><td>A. Knowing how to invoke ORCAD Pspice application S/W
B. Opening project and saving the project in appropriate location.
C. Selecting proper project for digital simulation.
D. Adding the relevant libraries to simulate the project</td><td><table><tr><th>A</th><th>B</th><th>C</th><th>D</th><th>T</th></tr><tr><td>1</td><td>1</td><td>1</td><td>2</td><td>5</td></tr></table></td><td>5</td></tr>
<tr><td>2. Manipulation of Software</td><td>A. Adding the required parts,input and output ports in the workspace.
B. Wiring the circuit as per the circuit diagram.
C. Customising the label names of all the inputs and ouputs of logic gates.
D. Creating the new simulation profile to the project</td><td><table><tr><th>A</th><th>B</th><th>C</th><th>D</th><th>T</th></tr><tr><td>2</td><td>10</td><td>5</td><td>3</td><td>20</td></tr></table></td><td>20</td></tr>
<tr><td>3. Precise Operations Activities</td><td>A. Running the project and adding input and output traces to the simulation graph
B. Observing the output waveforms
C. Interpreting the simulation results with truth tables
D. Repeating same simulation with selection of proper time periods and ON time of inputs such that the output is clearly understood</td><td><table><tr><th>A</th><th>B</th><th>C</th><th>D</th><th>T</th></tr><tr><td>5</td><td>5</td><td>5</td><td>5</td><td>20</td></tr></table></td><td>20</td></tr>
<tr><td>4. Values</td><td>A. Co-operation
B. Co-ordination
C. Communication
D. Sharing
E. Leadership</td><td><table><tr><th>A</th><th>B</th><th>C</th><th>D</th><th>E</th><th>T</th></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>5</td></tr></table></td><td>6</td></tr>
</table>

A. ASSESSMENT QUESTIONS:

1. Identify Menu Bar and various tabs under it when software is opened.(Lower)
2. How do you create a project and save it in appropriate location?(Lower)
3. Identify the various symbols which are used to design circuit(Lower)
4. Draw Full adder circuit diagram with two half adder circuits?(Medium)
5. How can you customise label names for all the inputs/outputs of logic gates?(Medium)
6. How can you edit the logic diagram when it is required ?(Medium)
7. How can you apply clock signals and how can you set Time period & On time for a signal? (Higher)
8. How can you perform simulation of the designed circuits using ORCAD Pspice?(Higher)

B. VIVA QUESTIONS:

1. Where do you see the output waveforms?
2. What happens if the run to time is less than the largest time period ?
3. What do you do if the required library files are not available in the given software ?
4. What happens if you don’t add library files ?
5. What happens if you don’t add traces ?
6. What would happen if input traces are added but ouput traces are not added ?

SIMULATION OF MULTIPLEXER USING PSPICE

1. Objectives:

1. To simulate Multiplexer Using PSPICE
2. To verify the truth table Multiplexer

2. Apparatus Required:

1. Personal Computer with Windows OS
2. ORCAD PSPICE 9.2 software package.

3. Task Analysis

A. Knowledge

1. IC Number of Multiplexer
2. Truth table of Multiplexer
3. PIN Configuration of IC74153
4. Working of Multiplexer

B. Skill

Handling of Software	• Knowing how to invoke ORCAD Pspice application S/W • Opening a new project • Selecting proper project for digital simulation • Naming the project and finding the location to save the project • Adding the required libraries to simulate the project
Manipulation of Software	A. Adding the required parts, input and output ports to the work space B. Wiring the circuit as per the circuit diagram C. Apply PSPICE stimulus to all input ports as the truth table D. Creating the new simulation profile to the project
Precise Operations/ Activities	A. Running the project and adding input and output traces to the simulation graph B. Observing the output waveforms C. Interpreting the simulation results with truth tables D. Repeating same simulation with selection of proper time periods and ON time of inputs such that the output is clearly understood

4. Teaching Points:

Sl.No	Teaching Point	Suggested Time – 15 Min
1	IC Number of Multiplexer	1
2	Truth Table of Multiplexer	3
3	PIN Configuration of IC74153	2
4	Working of Multiplexer	5
5	Working with ORCAD PSPICE	2
6	Precautions during virtual wiring to avoid overlapping	2

5. Precautions:

1. Disconnect all the Equipment from Mains before giving connections
2. Ensure Correct ICs were chosen.
3. Input ports should be properly selected
4. Overlapping virtual wiring should be avoided
5. Traces should be properly selected

6. Scheme of Evaluation:

<table>
<tr><th>Category of Skill</th><th>Sub task</th><th>Weightage with Competency level Individually</th><th>Total</th></tr>
<tr><td>1.Handling of apparatus</td><td>A. Knowing how to invoke ORCAD Pspice application S/W
B. Opening a new project
C. Selecting proper project for digital simulation
D. Naming the project and finding the location to save the project
E. Adding the required libraries to simulate the project</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>D</td><td>E</td><td>T</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>5</td></tr></table></td><td>5</td></tr>
<tr><td>2.Manipulation of apparatus</td><td>A. Adding the required parts, input and output ports to the work space
B. Wiring the circuit as per the circuit diagram
C. Apply Pspice stimulus to all input ports as the truth table
D. Creating the new simulation profile to the project</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>D</td><td>T</td></tr><tr><td>5</td><td>5</td><td>5</td><td>5</td><td>20</td></tr></table></td><td>20</td></tr>
<tr><td>3.Precise operations / activities</td><td>A. Running the project and adding input and output traces to the simulation graph
B. Observing the output waveforms
C. Interpreting the simulation results with truth tables
D. Repeating same simulation with selection of proper time periods and ON time of inputs such that the output is clearly understood</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>D</td><td>T</td></tr><tr><td>5</td><td>5</td><td>5</td><td>5</td><td>20</td></tr></table></td><td>20</td></tr>
<tr><td>4.Values</td><td>A. Co-operation
B. Co-ordination
C. Communication
D. Sharing
E. Leadership</td><td><table><tr><td>A</td><td>B</td><td>C</td><td>D</td><td>E</td><td>T</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>5</td></tr></table></td><td>5</td></tr>
</table>

7. Assessment Questions:

1. List two advantages of Pspice simulation of Digital electronics circuits?(Lower Order)
2. Between Clock period and ON time generally which is higher?(Middle Order)
3. For what Purpose we use **Add Trace** in PSPICE Simulation? (Higher Order)

8. Viva Questions

1. How Many 4:1 Multiplexers available in IC74153?(Lower order)

2. How many select lines are necessary for a 16:1 MUX? (Middle order)

3. How many 8:1 MUX are required to make 32:1 MUX? (Higher order)

WORK SHEET

Name of the student:		Date of experiment:
PIN:	Branch:	
Institution:		Experiment No:

1. Title of the Experiment: _____

2. Objective of the Experiment: _____

3. Equipment Required: _____

_____

_____

4. Circuit Diagram:

5. Procedure

6. Results

NAND gate

S.NO	A INPUT	B INPUT	OUTPUT
1	0	0	
2	0	1	
3	1	0	
4	1	1	

NOR gate

S.NO	A INPUT	B INPUT	OUTPUT
1	0		1
2	0	1	
3	1	0	
4	1	1	

AND gate

S.NO	A INPUT	B INPUT	OUTPUT
1	0	0	
2	0	1	
3	1	0	
4	1		1

OR gate

S.NO	A INPUT	B INPUT	OUTPUT
1	0	0	
2	0	1	
3	1	0	
4	1	1	

NOT gate

S.NO	A INPUT	OUTPUT
1	0	
2	1	

7. Inference and Interpretation:

8. Scheme of Evaluation:

Category of Skill	Sub task	Weightage with Competency level Individually	Total
1.Handling of apparatus	A. Identifying the various ICs B. Identifying the pins of ICs C. Selecting the correct ICs for various functions D. Identifying the connection points on the kit E. Testing of IC working condition	5	
2.Manipulation of apparatus	A. Making the connections as per the circuit diagram B. Connect the inputs to correct pins of ICs C. Checking the connections D. Keeping all the inputs low E. Varying the inputs HIGH or LOW as required	15	
3.Precise activities/operations	A. Applying the proper logic input signals B. Observing the outputs for different inputs C. Interpret the logic levels for output corresponding Inputs	25	
4.Values	A. Co-operation B. Co-ordination C. Communication D. Sharing E. Leadership	5	
		Total	50

Signature of the Staff

Signature of the Student

WORK SHEET

Name of the student:	Date of experiment:
PIN: Branch:	
Institution:	Experiment No:

1. Title of the Experiment:

2. Objective of the Experiment:

3. Equipment Required:

4. Circuit diagram:

5. Procedure:

6. Truth table:

AND Gate:

S. No	Switch 1 condition (For A input)	Switch 2 condition (For B input)	LED Status (For Output)	Interpretation of Readings in terms of logic values		
				A input	B input	Y Output
1	OFF	OFF	Doesn't Glow			
2	OFF	ON	Doesn't Glow			
3	ON	OFF	Doesn't Glow			
4	ON	ON	Glow			

OR Gate:

S.No	Switch 1 condition (For A input)	Switch 2 condition (For B input)	LED Status (For Output)	Interpretation of Readings in terms of logic values		
				A input	B input	Y Output
1	OFF	OFF	Doesn't Glow			
2	OFF	ON	Glow			
3	ON	OFF	Glow			
4	ON	ON	Glow			

AND Gate:

S.No	Switch 1 condition (For A input)	LED Status (For Output)	Interpretation of Readings in terms of logic values	
			A input	Y Output
1	OFF	Glow		
2	ON	Doesn't Glow		

7. Results:

8. Discussion on Results (Mandatory):

9. Scheme of Evaluation:

Category of Skill	Sub task	Weightage with Competency level Individually	Total
1.Handling of apparatus	A. Identifying components B. Identifying the PINs of ICs C. Identifying the connection points on the kit	5	
2.Manipulation of apparatus	A. Handling ICs B. Testing ICs C. Connecting the circuit	20	
3.Precise activities	A. Applying proper logic input signals B. Observing logic output and interpreting its logic level.	20	
4.Values	A. Co-operation B. Co-ordination C. Communication D. Sharing E. Leadership	5	
		Total	50

Signature of the staff Signature of the Student

WORK SHEET

Name of the student:		Date of experiment:
PIN:	Branch:	
Institution:		Experiment No:

1. Title of the Experiment: _____

2. Objective of the Experiment: _____

3. Equipment Required: _____

_____

_____

_____

4. Circuit Diagram:

5. Procedure

6. Readings:

AND Gate

S.No	A input	B input	Y Output
1	0	0	
2	0	1	
3	1	0	
4	1		1

OR Gate

S.No	A input	B input	Y Output
1	0	0	
2	0		1
3		1	1
4	1	1	

NOT GATE

SL.NO	A Input	Y output
1	0	
2		0

7. Inference and Interpretation:

8. Scheme of Evaluation:

Category of Skill	Sub task	Weightage with Competency level Individually	Total
1.Handling of apparatus	A. Identifying NOR Gate IC B. Selecting NOR Gates in a Quad NOR IC C. Testing IC using IC Tester D. Inserting the IC on Breadboard of Trainer E. Selecting the required patch cords & wires	5	
2.Manipulation of apparatus	A. Drawing the Circuit Diagram B. Making the Connections as per circuit diagram C. Keeping all the data inputs to low D. Switching ON the Power Supply E. Varying the inputs to HIGH or LOW as required.	20	
3.Precise activities	A. Applying proper logic input signals B. Observing logic output and interpreting logic level. C. Noting the Logic outputs for corresponding Inputs	20	
4.Values	A. Co-operation B. Co-ordination C. Communication D. Sharing E. Leadership	5	
		Total	50

Signature of the Staff

Signature of the Student

Name of the student:		Date of experiment:
PIN:	Branch:	
Institution:		

1. **Title of the experiment:** **EX-OR gate using NAND and NOR GATES**
2. **Objective of the experiment:** To implement the EX-OR gate using NAND and NOR Gates.
3. **Equipment required:** 7400 IC, 7402 IC, Digital trainer kit, patch cards
4. **Front panel/circuit diagram/block diagram:**

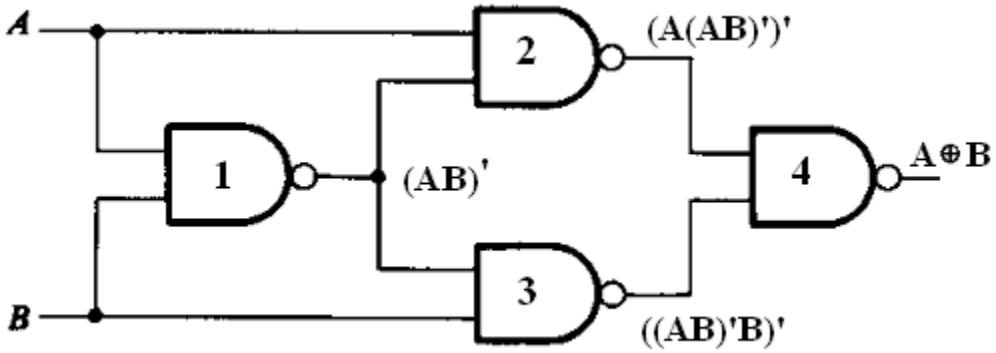


Fig:1 EX-OR GATE USING NAND GATES

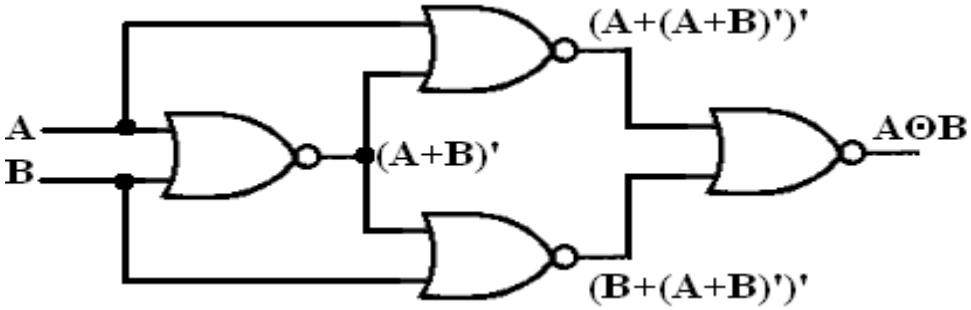
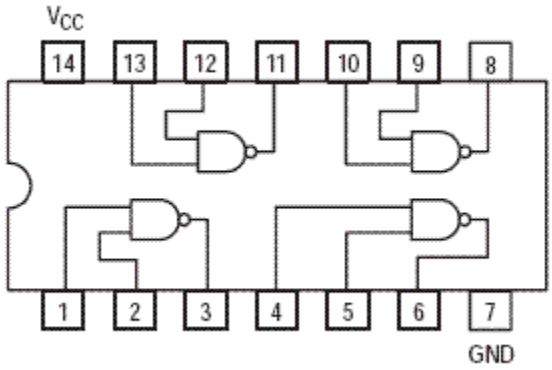


Fig:2 EX-OR GATE USING NOR GATES

Pin diagrams:

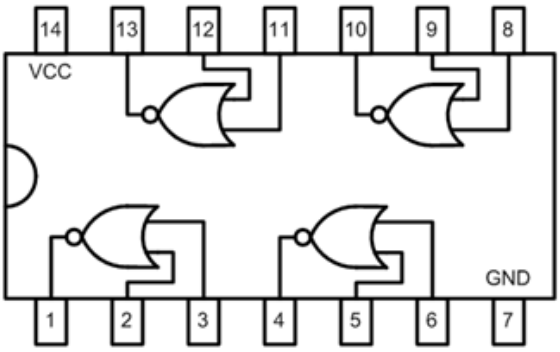
NOR 7400 IC:



Truth table:

A	B	$Y=\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

NOR 7402 IC:



Truth table:

A	B	$Y=\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

Fig:3 Pin Diagram of IC7400 & IC7402

5. Procedure:

1. Take the digital trainer kit and insert the 7400IC at appropriate position on bread board.
2. Connect pin 14 to v_{cc} and pin 7 to ground.
3. Connect the circuit diagram as shown in figure.
4. Switch on the trainer kit.
5. Apply various input combinations and observe output for each one.
6. Verify the truth table of EX-OR gate.
7. Insert the 7402 IC at appropriate position.
8. Connect pin 14 to v_{cc} and pin 7 to ground.
9. Connect the circuit diagram as shown in figure.
10. Switch on the trainer kit.
11. Apply various input combinations and observe output for each one.
12. Verify the truth table of EX-OR gate.

6. Results:

7. Discussion on result:

8. Scheme of evaluation:

CATEGORY OF SKILL	SUBTASK	WEIGHTAGE WITH COMPETENCY LEVEL INDIVIDUALLY	MARKS AWARDED
1. Handling of apparatus	A. Identification of IC's B. Identification of pins of IC's C. Identification of components in the trainer kit.	5	
2. Manipulation of apparatus	A. Circuit connections B. Handling of apparatus C. Testing of IC's	20	
3. Precise operations/activities	A. By applying inputs to the circuit and observe the outputs. B. Verifying truth tables C. Simplify the expressions	20	
4. Values	A. Co operation B. Co-Ordination C. Communication D. Sharing E. Leadership	5	
Total			50

Signature of the staff Signature of the student

WORK SHEET

1. **Title of the Experiment:**

2. **Objective of the experiment:**

Name of the student:		**Date of experiment:**
PIN:	**Branch:**	
Institution:		**Experiment No:**

3. **Equipment:**

4. **Circuit diagrams:**

HALF ADDER:

FULL ADDER:

5. Procedure:

6. Truth table:

Half adder

Input		Output	
A	B	Sum	Carry

Full adder

Input			Output	
A	B	C	Sum	Carry

7. Inference & Interpretation:

8 .Scheme of evaluation:

Category of Skill	SUB TASK	WEIHTAGE WITH COMPETENCY LEVEL INDIVIDUALLY	TOTAL (50)
1. Handling of apparatus	A) Identification of correct components. B) Identification of select, input & output sections.	5	
2. Manipulation of apparatus	A) Circuit connections. B) Equipment handling. C) Output Observations.	20	
3. Precise Operations Activities	A) Varying Select lines & Enable inputs. B) Verifying truth table.	20	
4. Values	A) Co Operation B) Co- Ordination C) Communication D) Sharing E) Leadership	5	
		Total	**50**

Signature of the staff **Signature of the student**

WORK SHEET

Name of the student :		Date of experiment:
PIN :	Branch:	
Institution:		Experiment No:

3.22.1 TITLE OF THE EXPERIMENT: _____

3.22.2 OBJECTIVE OF THE EXPERIMENT: _____

3.22.3 EQUIPMENT REQUIRED: _____

_____

_____

3.22.4 CIRCUIT DIAGRAM:

3.22.5 PROCEDURE:

3.22.6 OBSERVATIONS:

3.22.7 RESULT:

3.22.8 DISCUSSION ON RESULT:

3.22.9 SCHEME OF EVALUATION:

Category of Skill	Sub task	Weightage with Competency level Individually	Total
1. HANDLING OF APPARATUS	A. Knowing how to invoke ORCAD Pspice application S/W B. Opening a new project C. Selecting proper project for digital simulation D. Naming the project and finding the location to save the project E. Adding the required libraries to simulate the project	5	
2. MANIPULATION OF APPARATUS	A. Adding the required parts, input and output ports to the work space B. Wiring the circuit as per the circuit diagram C. Apply Pspice stimulus to all input ports as the truth table D. Creating the new simulation profile to the project	20	
3. PRECISE OPERTAIONS/ ACTIVITIES	A. Running the project and adding input and output traces to the simulation graph B. Observing the output waveforms C. Interpreting the simulation results with truth tables D. Repeating same simulation with selection of proper time periods and ON time of inputs such that the output is clearly understood	20	
4. VALUES	A. Co-operation B. Co-ordination C. Communication D. Sharing E. Leadership	5	
		TOTAL	50

Signature of staff **Signature of student**

WORK SHEET

Name of the student:		**Date:**
PIN:	**Branch:** ECE	
Institution:		**Experiment No:08**

1. Title of the Experiment : Multiplexer

2. Objective of the Experiment : To verify truth table of Multiplexer using IC 74153

3. Equipment Required : Digital Trainer Board,

Patch chords,

IC 74153

4. Block Diagram/ Circuit Diagram:

5. Procedure:

6. Truth Table:

Enable	**Data Input Lines**				**Selection Lines**		**Output**
$\overline{EA}$	I_{0A}	I_{1A}	I_{2A}	I_{3A}	S_1	S_0	Z_A

7. Inference and Interpretation:

8. Scheme of Evaluation:

Category of Skill	Sub Task	Weightage with Competency Level Individually	Marks awarded
1. Handling of apparatus	A) Identification of correct components. B) Identification of select, input & output sections.	5	
2. Manipulation of apparatus	A) Circuit connections. B) Equipment handling.	15	
3. Precise Operations Activities	A) Varying Select lines & Enable inputs. B) Output Observations C) Verifying truth table.	25	
4. Values	A) Co Operation B) Co- Ordination C) Communication D) Sharing E) Leadership	5	
		Total	**50**

Signature of the Staff **Signature of the Student**

BCD TO SEVEN SEGMENT DECODER USING IC 7448

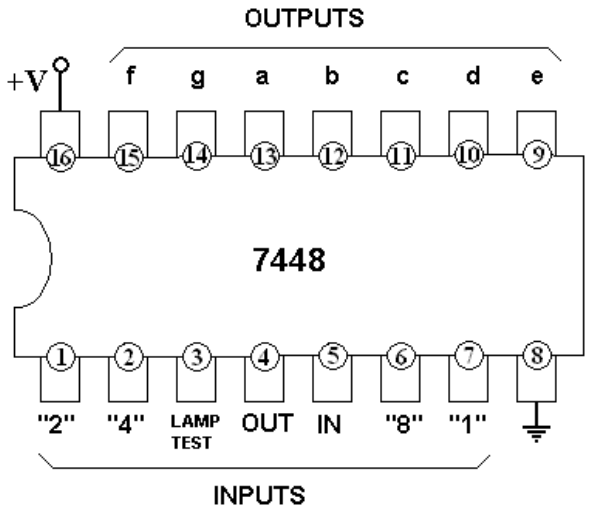
NAME OF THE STUDENT:		DATE:
PIN:	BRANCH: DECE	
POLYTECHNIC NAME:		EXPERIMENT NO: 09

1. TITLE OF EXPERIMENT: BCD to Seven Segment Decoder

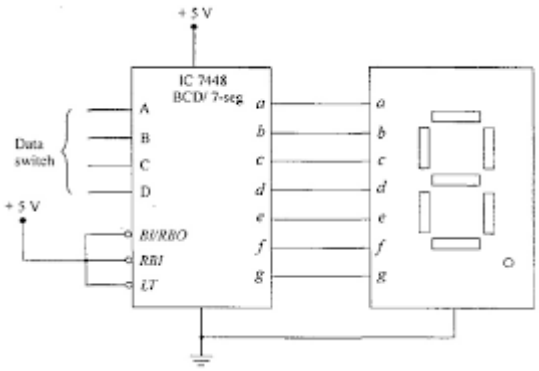
2. OBJECTIVE OF THE EXPERIMENT: To verify the truth table of BCD to Seven Segment Decoder.

3. EQUIPMENT REQUIRED:
   i) IC 7448,
   ii) Seven Segment Display,
   iii) IK Resistor,
   iv) Digital trainer kit,
   v) Power supply,
   vi) Connecting wires.

4. IC 7448 DIAGRAM:



5. CIRCUIT DIAGRAM:



5. PROCEDURE:

1. Connect 5V and ground to their indicated position on digital trainer kit.

2. Connect BCD inputs A, B, C, D to the pin of IC 74LS48 as shown in logic diagram

3. Connect +5V to Pins 3, 4, 5 of IC 74LS48.

4. Connect pins **13-a, 12-b, 11-c, 10-d, 9-e, 15-f, 14-g of** common anode display respectively.

5. Switch on the power supply.

6. Observe decimal output on common anode display given on the experiment board.

6. TRUTH TABLE:

BCD INPUTS				SEGMENT OUTPUTS							DISPLAY
A	**B**	**C**	**D**	**a**	**b**	**c**	**d**	**e**	**f**	**g**	

7. RESULTS: The truth table of BCD to Seven Segment Display is verified.

8. DISCUSSION ON RESULTS: IC7448 is a common anode open collector decoder and IC 7448 is common collector decoder

8. SCHEME OF EVALUATION

CATEGORY OF SKILL	SUB TASK	WEIGHTAGE WITH COMPETENCY LEVEL INDIVIDUALLY	MARKS AWARDED
1.HANDLING OF APPARATUS	a) Identification of components	5	
2.MANIPULATION OF APPARATUS	a) Circuit connections b) Equipment handling	15	
3.PRECISE ACTIVITIES	a) Identification of pin no of IC's b) Application of inputs c) Observation of outputs d) Tabulation of Input/output values	25	
4.VALUES	a) Co-operation b) Co-ordination c) Communication d) Sharing e) Leadership	5	
		Total :	50

SIGNATURE OF THE STUDENT SIGNATURE OF THE STAFF

WORK SHEET

Name of the Student:		Date of Experiment:
PIN :	Branch:	
Institution :		Experiment No:

1. Title of the Experiment : _____

2. Objective of the Experiment: _____

3. Equipment Required : _____

_____

_____

4. Pin Diagram:

5. Procedure:

6. Truth Table:

Inputs						Outputs							
G_1	G_{2A}	G_{2B}	A	B	C	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7

7. Results:

8. Discussion on Results:

9. Scheme of Evaluation:

Category of Skill	Sub Task	Weightage With Competency Level Individually	Marks Awarded
1.Handling of Apparatus	A. Identifying the components in the trainer kit B. Identifying the Pin configuration of IC	5	
2.Manipulation of Apparatus	A. Drawing the logic circuit B. Connecting the logic circuit C. Appling the Enable inputs	15	
3.Precision Operation Activities	A. Applying Inputs and Observe outputs B. Verifying the truth table C. Observing the outputs by changing the enable inputs	25	
4.Values	A. Co operation B. Co-ordination C. Communication D. Sharing E. Leadership	5	
	Total		50

Signature of the Staff

Signature of the Student

WORK SHEET

Name of the student:		Date of experiment:
PIN:	BRANCH:	
Institution:		Experiment No:

1. Title of the experiment : _____

2. Objective of the experiment : _____

3. Equipment required : _____

_____

4. Circuit diagram/block diagram:

Block diagram:

Pin diagram:

5. Procedure:

6. Truth Table:

INPUTS									OUTPUTS		
EI	0	1	2	3	4	5	6	7	A2	A1	A0

7. Results:

8 .Inference and interpretation:

9. Scheme of Evaluation:

CATEGORY OF SKILLS	SUB TASK	WEIGHATAGE WITH COMPETENCY LEVEL INDIVIDUALLY	MARKS AWARDED
1.Handling of apparatus	A. Identification of IC 74148 B. Identification of components in the trainer kit	5	
2.Manipulation of apparatus	A. Circuit connections B. Handling of apparatus C. Testing of IC	20	
3.Precise operations/activities	A. Identifying pin numbers of IC B. Truth table verification C. Observation of different logic states	20	
4.Values	A. Co operation B. Co ordination C. Communication D. Sharing E. leadership	5	
		Total:	
			50

Signature of the staff

signature of the student

WORK SHEET

Name of the student:		Date of experiment:
PIN:	Branch:	
Institution:		

1. **Title of the experiment:** **CLOCKED RS FLIP FLOP**
2. **Objective of the experiment:** Design a clocked RS flip flop using NAND gates and Verify its truth table.
3. **Equipment required:** 7400 IC, Digital trainer kit, patch cards
4. **Front panel/circuit diagram/block diagram:**

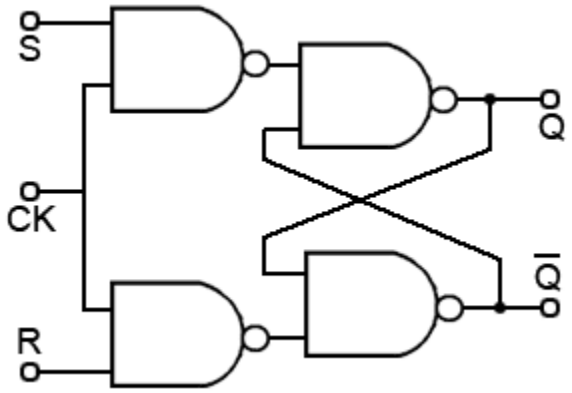


Fig: 1 Clocked RS flip-flop using NAND gates

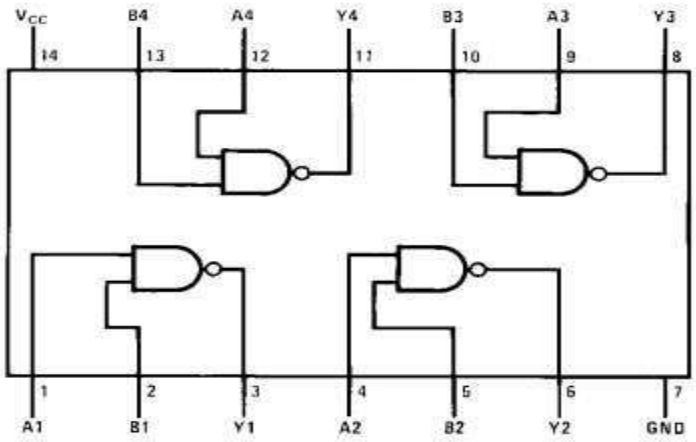


Fig: 2 pin diagram of IC 7400

5. Truth table of RS Flip-flop:

INPUTS			OUTPUT		STATE
CLK	S	R	Q	$\overline{Q}$	
X	0	0	NC	NC	NO CHANGE
↑	0	1	0	1	RESET
↑	1	0	1	0	SET
↑	1	1	-	-	FORBIDDEN

6. Procedure:

13. Take the digital trainer kit and insert the 7400IC at appropriate position.
14. Connect pin 14 to v_{cc} and pin 7 to ground.
15. Connect the circuit diagram as shown in figure
16. Give the clock input from pulser,
17. Switch on the trainer kit,
18. Apply various input combinations and observe output for each one.
19. Verify the truth table of RS Flip-flop.

7. Results:

8. Discussion on result:

9. Scheme of evaluation:

CATEGORY OF SKILL	SUBTASK	WEIGHTAGE WITH COMPETENCY LEVEL INDIVIDUALLY	MARKS AWARDED
1. Handling of apparatus	A. Identification of IC's B. Identification of pins of IC's C. Identification of components in the trainer kit.	5	
2. Manipulation of apparatus	A. Circuit connections B. Handling of apparatus C. Testing of IC's	20	
3. Precise operations/activities	A. By applying inputs to the circuit and observe the outputs B. Verifying truth tables C. Simplify the expressions	20	
4. Values	A. Co operation B. Co-Ordination C. Communication D. Sharing E. Leadership	5	
Total			50

Signature of the staff

Signature of the student

WORK SHEET

Name of the student:	Date of experiment:
PIN: Branch:	
Institution:	Experiment No:

1. **Title of the Experiment**:

2. **Objective of the Experiment**:

3. **Equipment Required**:

4. **Circuit diagram**:

5. **Procedure**:

6. Readings.

S.No	Clock input	Preset	Clear	Switch condition (For J and K inputs)		LED 1 Status (For Q Output)	LED 2 Status (For $\bar{Q}$ Output)

Interpretation of above Observations in terms of logic values.

S.No	Clock input	Preset	Clear	Switch condition (For J and K inputs)		LED 1 Status (For Q Output)	LED 2 Status (For $\bar{Q}$ Output)

7. Results:

8. Discussion on Results:

9. **Scheme of Evaluation**

Category of Skill	Sub task	Weightage with Competency level Individually	Total
1.Handling of apparatus	A. Identifying components B. Identifying the PINs of ICs C. Identifying the connection points on the kit	5	
2.Manipulation of apparatus	A. Handling ICs B. Testing ICs C. Connecting the circuit	20	
3.Precise activities	A. Applying proper logic input signals B. Observing logic output and interpreting its logic level.	20	
4.Values	A. Co-operation B. Co-ordination C. Communication D. Sharing E. Leadership	5	
		Total	50

Signature of the staff Signature of the Student

WORK SHEET

Name of the student:	**Date of experiment:**
PIN: **Branch:**	
Institution:	**Experiment No:**

1. Title of the Experiment:

2. Objective of the Experiment:

3. Equipment Required:

4. Circuit diagram:

5. Procedure:

6. Readings.

S.No	Clock input	Switch condition (For D input)	LED 1 Status (For Q Output)	LED 2 Status (For $\bar{Q}$ Output)
1				
2				
3				

Interpretation of above Observations in terms of logic values.

S.No	Clock input	D input	Q Output	$\bar{Q}$ Output
1				
2				
3				

S.No	Clock input	Switch condition (For T input)	LED 1 Status (For Q Output)	LED 2 Status (For $\bar{Q}$ Output)
1				
2				
3				

Interpretation of above Observations in terms of logic values.

S.No	Clock input	T input	Q Output	$\bar{Q}$ Output
1				
2				
3				

7.Results:

8. Discussion on Results:

9. Scheme of Evaluation

Category of Skill	Sub task	Weightage with Competency level Individually	Total
1.Handling of apparatus	A. Identifying components B. Identifying the PINs of ICs C. Identifying the connection points on the kit	5	
2.Manipulation of apparatus	A. Handling ICs B. Testing ICs C. Connecting the circuit	20	
3.Precise activities	A. Applying proper logic input signals B. Observing logic output and interpreting its logic level.	20	
4.Values	A. Co-operation B. Co-ordination C. Communication D. Sharing E. Leadership	5	
		Total	50

Signature of the staff Signature of the Student

WORK SHEET

Name of the Student:		Date of Experiment:
PIN :	Branch:	
Institution :		Experiment No:

1. Title of the Experiment : _____

2. Objective of the Experiment: _____

3. Equipment Required : _____

_____

_____

4. Pin Diagram:

5. Logic diagram and waveforms:

5. Procedure:

6. Truth Table:

clk	Q_0	Q_1	Q_2	Q_3

7. Results:

8. Discussion on Results:

9. Scheme of Evaluation:

Category of Skill	Sub Task	Weightage With Competency Level Individually	Marks Awarded
1.Handling of Apparatus	A. Identifying the components in the trainer kit B. Identifying the Pin configuration of IC C. Checking the IC	5	
2.Manipulation of Apparatus	A. Drawing the Logic circuit B. Connecting the Logic circuit C. Applying the clock pulse	15	
3.Precision Operation Activities	A. Observing the output after applying each pulse B. Obtain the timing waveforms	25	
4.Values	A. Co operation B. Co-ordination C. Communication D. Sharing E. Leadership	5	
		Total	50
Signature of staff		Signature of student	

WORK SHEET

Name of the student:		Date of experiment:
PIN:	Branch:	
Institution:		Experiment No:

1.Title of the Experiment: _____

2. Objective of the Experiment: _____

3. Equipment Required: _____

_____

_____

_____

4. Circuit Diagram:

5. Procedure

6. Readings:

COUNT TRUTH TABLE:

Inputs				Outputs			
R_1	R_2	S_1	S_2	Q	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

COUNT	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	0	0	0	0

7. Inference and Interpretation:

8. Scheme of Evaluation:

Category of Skill	Sub task	Weightage with Competency level Individually	Total
1.Handling of apparatus	A. Identifying Decade Counter IC B. Identifying the pins of ICs C. Testing IC whether it is Good or Bad D. Inserting the IC on Breadboard of Trainer Selecting the required patch cords & wires	5	
2.Manipulation of apparatus	A. Drawing the Circuit Diagram B. Making the Connections as per circuit diagram C. keeping all the data inputs to low D. Switching ON the Power Supply E. Varying the inputs to HIGH or LOW as required.	20	
3.Precise activities	A. Applying proper logic input signals B. Observing logic output and interpreting logic level. C. Noting the Logic outputs for corresponding Inputs	20	
4.Values	A. Co-operation B. Co-ordination C. Communication D. Sharing E. Leadership	5	
		Total	50
Signature of the Staff			Signature of the Student

WORK SHEET

Name of the student :		Date of experiment:
PIN :	Branch:	
Institution:		Experiment No.

1. **Title of the Experiment:**
2. **Objective of the Experiment:**
3. **Equipment Required :**
4. **Pin Diagram & Pin Description:**
5. **Procedure:**

6. **Readings :**

Count-UP Mode:

Clock pulse	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Count-Down mode:

Clock pulse	Q_3	Q_2	Q_1	Q_0
0	1	1	1	1
1	1	1	1	0
2	1	1	0	1
3	1	1	0	0
4	1	0	1	1
5	1	0	1	0
6	1	0	0	1
7	1	0	0	0
8	0	1	1	1
9	0	1	1	0
10	0	1	0	1
11	0	1	0	0
12	0	0	1	1
13	0	0	1	0
14	0	0	0	1
15	0	0	0	0

7. **Inference and Interpretation:**

8. Scheme of Evaluation:

CATEGORY OF SKILL	SUB TASK	WEIGHTAGE WITH COMPETENCY LEVEL INDIVIDUALLY	MARKS AWARDED
1.Handling of Apparatus	A. Identifying the various ICs B. Identifying the pins of ICs C. Selecting the correct ICs for various functions D. Identifying the connection points on the kit E. Testing of IC working condition	5	
2.Manipulation of Apparatus	A. Making the connections as per the circuit diagram B. Connect the inputs to correct pins of ICs C. Checking the connections D. Keeping all the inputs low E. Varying the inputs HIGH or LOW as required	20	
3.Precise operations/Activities	A. Applying the proper logic input signals B. Observing the outputs for different inputs C. Interpret the logic levels for output corresponding Inputs	20	
4.Values	a) Co-operation b) Co-Ordination c) Communication d) Sharing	5	
		Total	50

Signature of the Staff Signature of the Student

3.18 WORK SHEET

Name of the student :		Date of experiment:
PIN :	Branch:	
Institution:		Experiment No:

3.18.1 TITLE OF THE EXPERIMENT: _____

3.18.2 OBJECTIVE OF THE EXPERIMENT: _____

_____

3.18.3 EQUIPMENT REQUIRED: _____

_____

_____

3.18.4 CIRCUIT DIAGRAM:

3.18.5 PROCEDURE:

3.18.6 TRUTH TABLE:

3.18.18 RESULT:

3.18.8 DISCUSSION ON RESULT:

3.18.9 SCHEME OF EVALUATION:

CATEGORY OF SKILL	SUB TASK	WEIGHTAGE WITH COMPETENCY LEVEL INDIVIDUALLY	TOTAL
1.HANDLING OF APPARATUS	A. Identify the major parts in the kit.(like LEDs, switches, Clock) B. Identify the input and output pins of IC	5	
2.MANIPULATION OF APPARATUS	A. Read IC pin diagram B. Equipment handling C. Observations	20	
3.PRECISE OPERTAIONS / ACTIVITIES	A. IC connections for different modes(SISO,SIPO,PISO,PIPO) of shift register B. Tabulation of values of truth table	20	
4.VALUES	A. Cooperation B. Coordination C. Communication D. Sharing E. Leadership	5	
		TOTAL	50

Signature of staff **Signature of student**

WORK SHEET

Name of the student:		Date of experiment:
PIN:	Branch:	
Institution:		Experiment No:

1. Title of the Experiment: _____

2. Objective of the Experiment: _____

3. Equipment Required: _____

_____

_____

_____

4. Circuit Diagram:

5. Procedure

6. Readings:

AND Gate

S.No	A input	B input	Y Output
1			
2			
3			
4			

OR Gate

S.No	A input	B input	Y Output
1			
2			
3			
4			

NOT GATE

SL.NO	A Input	Y output
1		
2		

EXOR GATE

S.No	A input	B input	Y Output
1			
2			
3			
4			

7. Inference and Interpretation:

8. Scheme of Evaluation:

Category of Skill	Sub task	Weightage with Competency level Individually	Total
1.Handling of apparatus	A. Knowing how to invoke ORCAD PSPICE application S/W B. Opening a new project C. Selecting proper project for digital simulation D. Naming the project and finding the location to save the project E. Adding the required libraries to simulate the project	5	
2.Manipulation of apparatus	A. Adding the required parts, input and output ports to the work space B. Wiring the circuit as per the circuit diagram C. Apply PSPICE stimulus to all input ports as the truth table D. Creating the new simulation profile to the project	20	
3.Precise activities/operations	A. Running the project and adding input and output traces to the simulation graph B. Observing the output waveforms C. Interpreting the simulation results with truth tables D. Repeating same simulation with selection of proper time periods and ON time of inputs such that the output is clearly understood	20	
4.Values	A. Co-operation B. Co-ordination C. Communication D. Sharing E. Leadership	5	

Signature of the staff Signature of the student

WORK SHEET

Name of the student:		Date of experiment:
PIN:	Branch:	
Institution:		Experiment No:

1. Title of the Experiment: _____

2. Objective of the Experiment: _____

3. Equipment Required: _____

_____

_____

_____

4. Circuit Diagram:

5. Procedure

6. Readings:

AND Gate

S.No	A input	B input	Y Output
1			
2			
3			
4			

OR Gate

S.No	A input	B input	Y Output
1			
2			
3			
4			

NOT GATE

SL.NO	A Input	Y output
1		
2		

EXOR GATE

S.No	A input	B input	Y Output
1			
2			
3			
4			

7. Inference and Interpretation:

8. Scheme of Evaluation:

Category of Skill	Sub task	Weightage with Competency level Individually	Total
1.Handling of apparatus	• Knowing how to invoke ORCAD Pspice application S/W • Opening a new project • Selecting proper project for digital simulation • Naming the project and finding the location to save the project • Adding the required libraries to simulate the project	5	
2.Manipulation of apparatus	A. Adding the required parts, input and output ports to the work space B. Wiring the circuit as per the circuit diagram C. Apply Pspice stimulus to all input ports as the truth table D. Creating the new simulation profile to the project	20	
3.Precise activities/ operations	A. Running the project and adding input and output traces to the simulation graph B. Observing the output waveforms C. Interpreting the simulation results with truth tables D. Repeating same simulation with selection of proper time periods and ON time of inputs such that the output is clearly understood	20	
4.Values	A. Co-operation B. Co-ordination C. Communication D. Sharing E. Leadership	5	

Signature of the staff Signature of the student

WORK SHEET

Name of the student:		Date of experiment:
PIN:	Branch:	
Institution:		Experiment No:

1. Title of the Experiment: _____

2. Objective of the Experiment: _____

3. Equipment Required: _____

_____

_____

_____

4. Circuit Diagrams:

Half adder :

Full adder :

5. Procedure

6. Truth table:

Half adder:

Input		Output	
A	B	Sum	Carry

Full adder:

Input			Output	
A	B	C	Sum	Carry

7. Inference and Interpretation:

8. Scheme of Evaluation:

Category of Skill	Sub task	Weightage with Competency level Individually	Total
1.Handling of software	A. Knowing how to invoke ORCAD Pspice application S/W B. Opening project and saving the project in appropriate location. C. Selecting proper project for digital simulation. D. Adding the relevant libraries to simulate the project	5	
2.Manipulation of software	A. Adding the required parts,input and output ports in the workspace. B. Wiring the circuit as per the circuit diagram. C. Customising the label names of all the inputs and ouputs of logic gates. D. Creating the new simulation profile to the project	20	
3.Precise activities/operations	A. Running the project and adding input and output traces to the simulation graph B. Observing the output waveforms C. Interpreting the simulation results with truth tables D. Repeating same simulation with selection of proper time periods and ON time of inputs such that the output is clearly understood	20	
4.Values	A. Co-operation B. Co-ordination C. Communication D. Sharing E. Leadership	5	

Signature of the staff Signature of the student

WORK SHEET

Name of the student:		Date of experiment:
PIN:	Branch:	
Institution:		Experiment No:

1. Title of the Experiment: _____

2. Objective of the Experiment: _____

3. Equipment Required: _____

_____

_____

_____

4. Circuit Diagram:

5. Procedure

6. Readings:

MULTIPLEXER:

Enable	Data Input Lines				Selection Lines		Output
$\overline{EA}$	I_{0A}	I_{1A}	I_{2A}	I_{3A}	S_1	S_0	Z_A

7. Inference and Interpretation:

8. Scheme of Evaluation:

Category of Skill	Sub task	Weightage with Competency level Individually	Total
1.Handling of apparatus	A. Knowing how to invoke ORCAD Pspice application S/W B. Opening a new project C. Selecting proper project for digital simulation D. Naming the project and finding the location to save the project E. Adding the required libraries to simulate the project	5	
2.Manipulation of apparatus	A. Adding the required parts, input and output ports to the work space B. Wiring the circuit as per the circuit diagram C. Apply Pspice stimulus to all input ports as the truth table D. Creating the new simulation profile to the project	20	
3.Precise activities/operations	A. Running the project and adding input and output traces to the simulation graph B. Observing the output waveforms C. Interpreting the simulation results with truth tables D. Repeating same simulation with selection of proper time periods and ON time of inputs such that the output is clearly understood	20	
4.Values	A. Co-operation B. Co-ordination C. Communication D. Sharing E. Leadership	5	

Signature of the staff Signature of the student

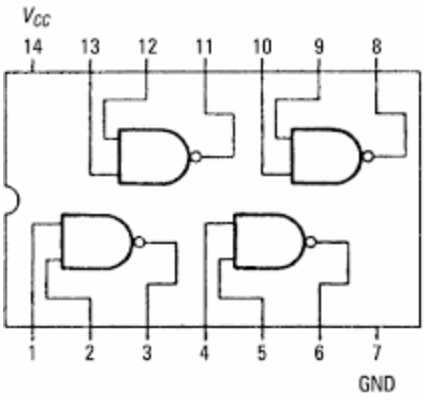
LOGIC GATES

1. Description

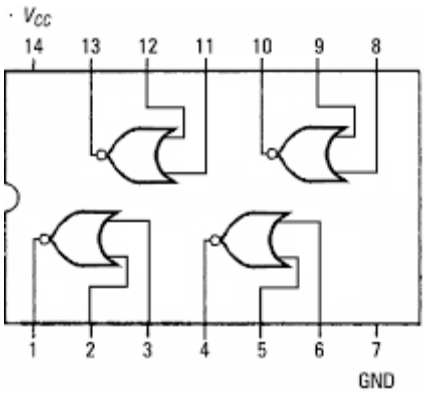
This experiment requires the following equipment

Name	Specifications	No	Purpose
Digital IC trainer kit	Power supply	1	To verify the truth tables of basic & universal gates
Quad 2 input NAND gate(74LS00)	Supply voltage 5v	1	To verify the truth table of NAND gate
Quad 2 input NOR gate(74LS02)	Supply voltage 5v	1	To verify the truth table of NOR gate
Quad 2 input AND gate(74LS08)	Supply voltage 5v	1	To verify the truth table of AND gate
Quad 2 input OR gate(74LS32)	Supply voltage 5v	1	To verify the truth table of OR gate
Quad 2 input NOT gate(74LS04)	Supply voltage 5v	1	To verify the truth table of NOT gate
Bread board		1	To make connections
Connecting wires		As per required	To make connections

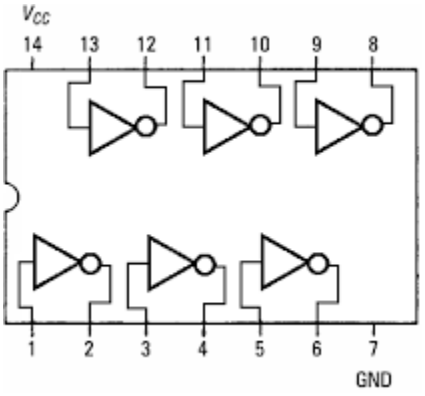
2. Circuit diagram



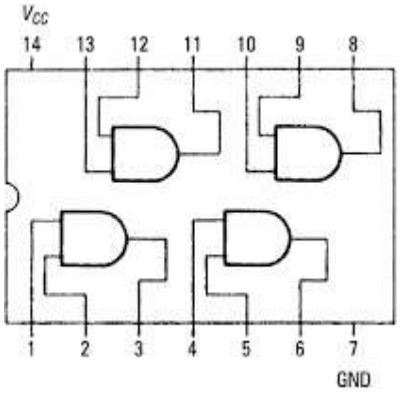
Quad 2 input NAND gate(74LS00)



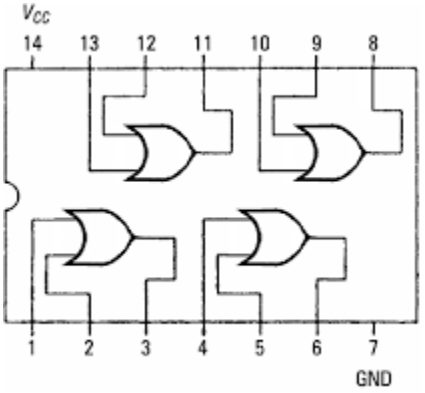
Quad 2 input NOR gate(74LS02)



Quad 2 input NOT gate(74LS04)



Quad 2 input AND gate(74LS08)



Quad 2 input OR gate(74LS32)

3. Theory

Logic gates are electronic circuits which perform logical functions on one or more inputs to produce one output. There are seven logic gates. When all the input combinations of a logic gate are written in a series and their corresponding outputs written along them, then this input/ output combination is called **Truth Table**. Various gates and their working is explained here.

AND gate produces an output as 1, when all its inputs are 1; otherwise the output is 0. This gate can have minimum 2 inputs but output is always one. Its output is 0 when any input is 0.

OR gate produces an output as 1, when any or all its inputs are 1; otherwise the output is 0. This gate can have minimum 2 inputs but output is always one. Its output is 0 when all input are 0.

NOT gate produces the complement of its input. This gate is also called an INVERTER. It always has one input and one output. Its output is 0 when input is 1 and output is 1 when input is 0.

NAND gate is actually a series of AND gate with NOT gateIts output is 1 when any or all inputs are 0, otherwise output is 1.

NOR gate is actually a series of OR gate with NOT gate. Its output is 0 when any or all inputs are 1, otherwise output is 1.

4. Procedure

1. **Connect** the **trainer kit** to ac power supply.
2. **Place** the **IC** ON breadboard
3. **Connect** the **inputs** of any one logic gate to the **logic sources** and its **output** to the **logic indicator**.
4. **Apply** various **input combinations** and **observe output** for each one.
5. **Verify** the **truth table** for each input/ output combination.
6. **Repeat** the process for all other logic gates.

7. **Switch off** the ac power supply.

5. Observations

S.No	Switch 1 condition (for A input)	Switch 2 condition (for b input)	LED status for output
1	Off	Off	Glow
2	Off	On	Glow
3	On	Off	Glow
4	On	on	Does not glow

Interpretation of above Observations in terms of logic values.

S.NO	A INPUT	B INPUT	OUTPUT
1	0	0	1
2	0	1	1
3	1	0	1
4	1	1	0

NOR GATE

S.No	Switch 1 condition (for A input)	Switch 2 condition (for b input)	LED status for output
1	Off	Off	Glow
2	Off	On	Does not glow
3	On	Off	Does not glow
4	On	on	Does not glow

Interpretation of above Observations in terms of logic values.

S.NO	A INPUT	B INPUT	OUTPUT
1	0	0	1
2	0	1	0
3	1	0	0
4	1	1	1

AND GATE

S.No	Switch 1 condition (for A input)	Switch 2 condition (for b input)	LED status for output
1	Off	Off	Does not glow
2	Off	On	Does not glow
3	On	Off	Does not glow
4	On	on	glow

Interpretation of above Observations in terms of logic values.

S.NO	A INPUT	B INPUT	OUTPUT
1	0	0	0
2	0	1	0
3	1	0	0
4	1	1	1

OR GATE

S.No	Switch 1 condition (for A input)	Switch 2 condition (for b input)	LED status for output
1	Off	Off	glow
2	Off	On	glow
3	On	Off	glow
4	On	on	Does not glow

Interpretation of above Observations in terms of logic values.

S.NO	A INPUT	B INPUT	OUTPUT
1	0	0	1
2	0	1	1
3	1	0	1
4	1	1	0

NOT GATE

S.No	Switch 1 condition (for A input)	LED status for output
1	Off	glow
4	On	Does not glow

Interpretation of above Observations in terms of logic values.

S.NO	A INPUT	OUTPUT
1	0	1
2	1	0

REALISATION OF AND, OR, NOT GATES USING 2 INPUT NAND GATES

1. Description:

1. The setup for this experiment requires IC 7400 and Digital logic trainer kit.
2. IC 7400 is a DIP 14-Pin Quad 2-input NAND gate IC.
3. We can use any one of the multiple gates available in an IC.
4. Digital logic trainer kit provides logic input switches for applying logic inputs and logic output LED indicators for observing output logic.

2. Circuit diagram:

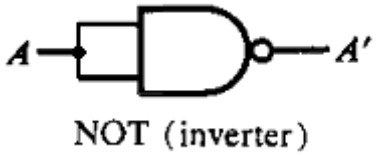


Figure: NOT gate using NAND gate

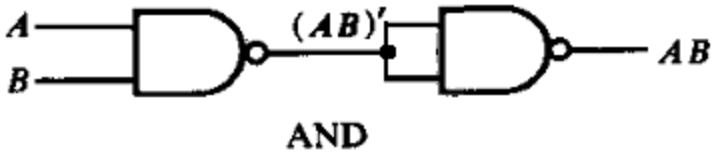


Figure: AND gate using NAND gate

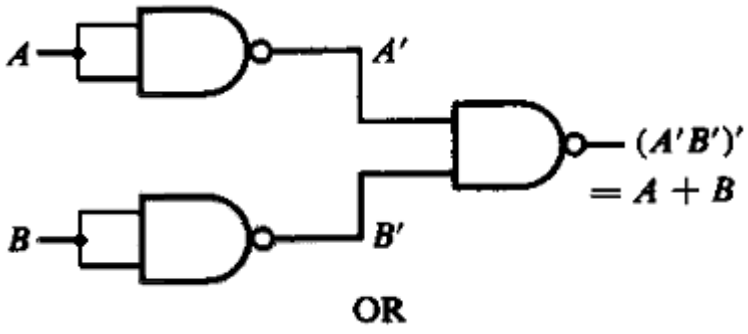
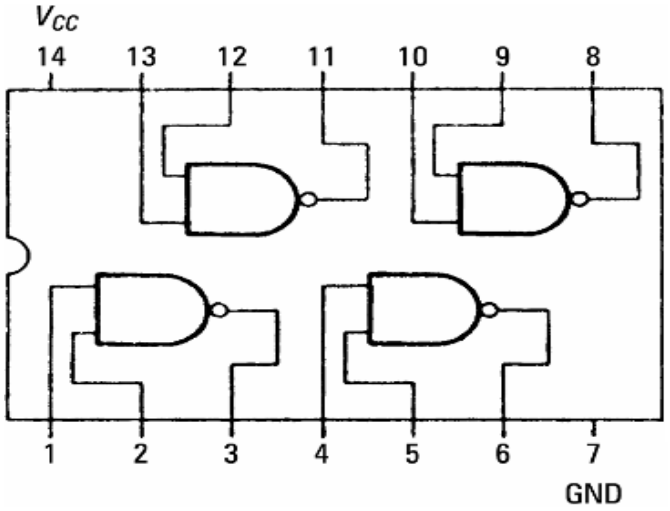


Figure: OR gate using NAND gate

Pin diagram:

NAND 7400 IC:



$Y=\overline{A.B}$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

3. Theory:

NAND gate is actually a combination of two logic gates: AND gate followed by NOT gate. So its output is complement of the output of an AND gate.

This gate can have minimum two inputs, output is always one. By using only NAND gates, we can realize all logic functions: AND, OR, NOT, X-OR, X-NOR, NOR. So this gate is also called universal gate.

4. Procedure:

1. **Make** the **connections** as shown in the **circuit diagram**.
2. **Feed** the logic signal from the **logic input** switches.
3. **Observe** the logic **outputs** on the logic level LED indicators.
4. Observe the output for all possible input combinations.
5. **Verify** the corresponding **truth table.**

5. Observations:

AND Gate:

S.No	Switch 1 condition (For A input)	Switch 2 condition (For B input)	LED Status (For Output)	Interpretation of Readings in terms of logic values		
				A input	B input	Y Output
1	OFF	OFF	Doesn't Glow	0	0	0
2	OFF	ON	Doesn't Glow	0	1	0
3	ON	OFF	Doesn't Glow	1	0	0
4	ON	ON	Glow	1	1	1

OR Gate:

S.No	Switch 1 condition (For A input)	Switch 2 condition (For B input)	LED Status (For Output)	Interpretation of Readings in terms of logic values		
				A input	B input	Y Output
1	OFF	OFF	Doesn't Glow	0	0	0
2	OFF	ON	Glow	0	1	1
3	ON	OFF	Glow	1	0	1
4	ON	ON	Glow	1	1	1

NOT Gate:

S.No	Switch 1 condition (For A input)	LED Status (For Output)	Interpretation of Readings in terms of logic values	
			A input	Y Output
1	OFF	Glow	0	1
2	ON	Doesn't Glow	1	0

REALIZATION OF AND, OR, NOT USING 2 INPUT NOR GATE

1. Description

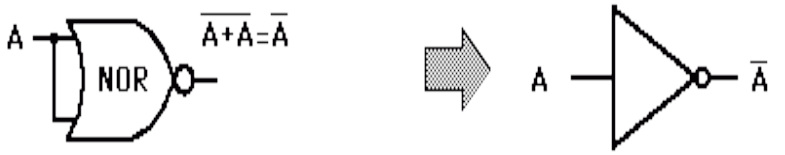
The setup for this experiment requires the following Equipment

Name	Specifications	No	Purpose
Digital Logic Trainer		1	To insert IC
NOR Gate IC 7402	DIP 14 PIN Quad 2-input IC	1	To realize basic gates
Patch cords		As per need	To make connections
Single Strand wires		As per need	To make connections

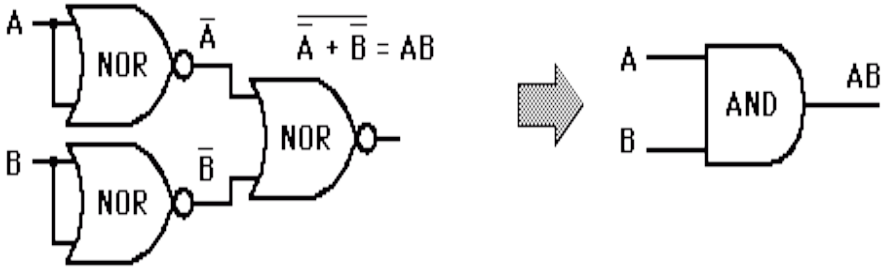
2. Circuit Diagram

Realization of NOT, AND, OR using NOR Gates

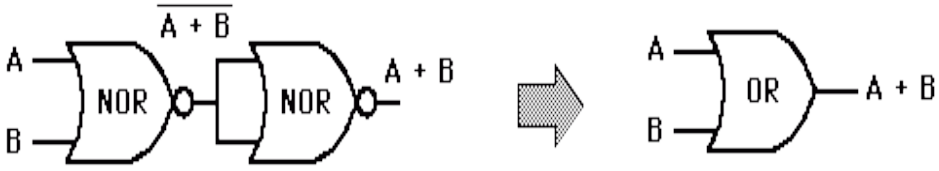
NOT Gate



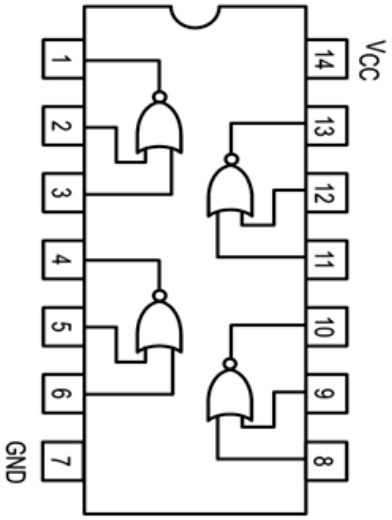
AND Gate

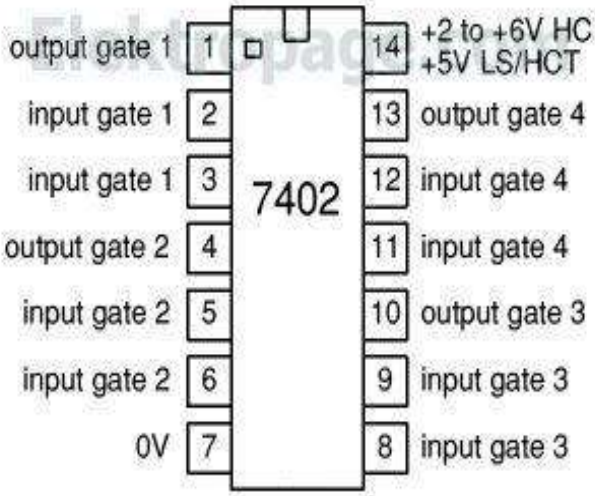


OR Gate



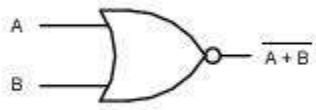
Pin Diagram of IC 7402





3. Theory

- The basic logic gates AND, OR and NOT can be combined to realize any other logic circuit. The NOR gate is a derived gate and is special since it is considered a universal gate. It is a NOT OR gate and the logic symbol is the OR gate with an invert bubble on its output.



- Like the AND and OR gates the NOR gate can more than two inputs. The universality of the NOR gate means any Boolean expression may be implemented with all NOR gates without the use of any other logic type gate.
- To realize NOT Gate using NOR Gate both the inputs have been shorted since NOT Gate has only one input. When binary HIGH signal (1) is given at the input, binary LOW (0) is the output and vice-versa.
- To realize OR Gate using NOR Gate, the output of NOR Gate is connected to NOT Gate.
- To realize AND Gate using NOR Gate, the inputs are complemented using 2 NOR gates and their outputs are given as inputs to the other NOR gate.

4. Procedure

1. Make the connections as shown in circuit diagram.
2. Feed the logic signal from the logic input switches.
3. Observe the logic outputs on the logic level LED indicators.
4. Observe the output for all possible input combinations.
5. Verify the corresponding truth table.

5. Truth Tables

NOT GATE:

INPUT	OUTPUT
A	Y=A
0	1
1	0

AND GATE:

INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

OR GATE:

INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

6. Precautions:

1. Disconnect all the Equipment from Mains before giving connections
2. Ensure Correct ICs were chosen.
3. ICs are to be inserted with great care.
4. Loose connections should be avoided
5. Power supply for ICs should be 5V DC.
6. Before turning ON the power to the trainer review the wiring for errors.

EX-OR GATE USING NAND AND NOR GATES

1. **Description**
   i. The set up this experiment requires a 7400 IC,7402 IC, Digital trainer kit
   ii. IC's are available in laboratory and by using these IC'S we can verify the truth tables

2. **Circuit diagram**

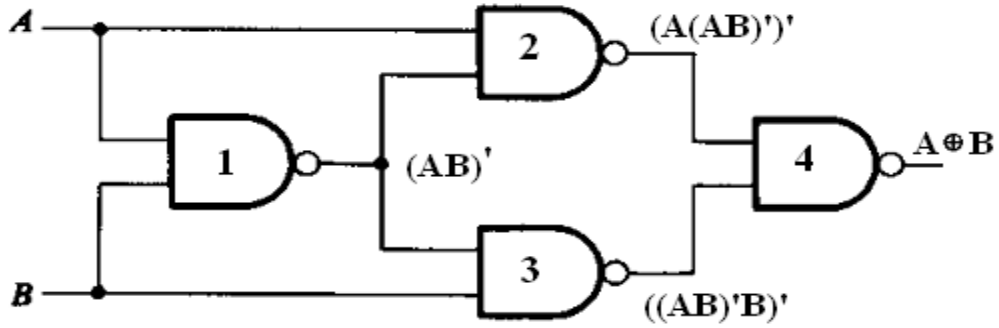


Fig:1 EX-OR GATE USING NAND GATES

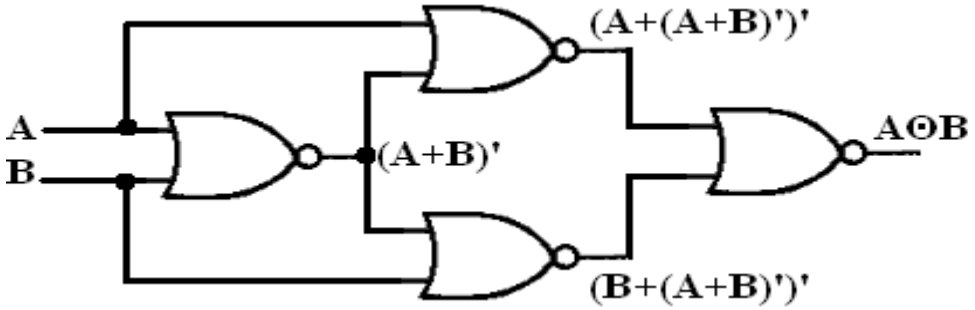
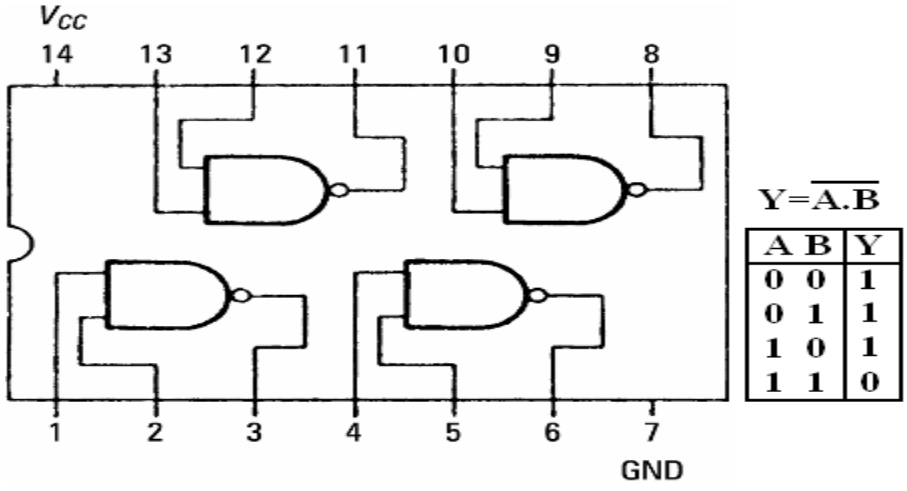


Fig:2 EX-OR GATE USING NOR GATES

PIN DIAGRAM:

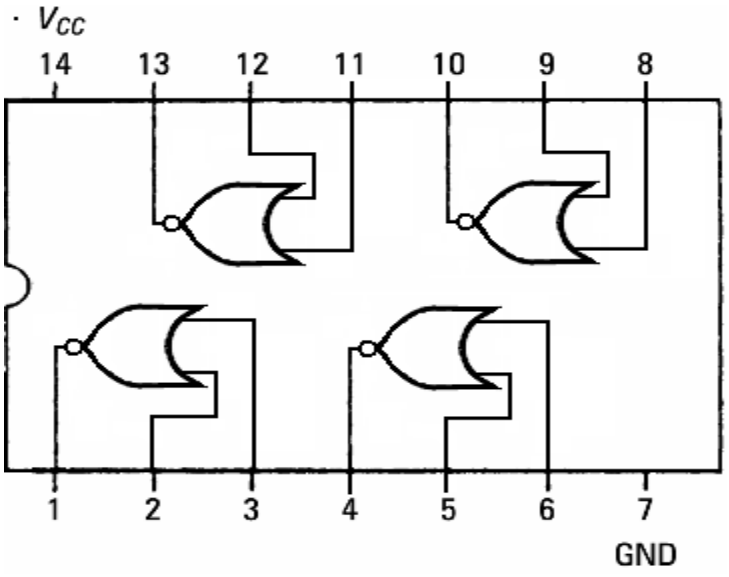
NAND 7400 IC:



$Y=\overline{A.B}$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NOR 7402 IC:



$Y=\overline{A+B}$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

3. Theory

1. The NAND or NOR Gates can be used to develop any one of the logic gates. It means that one can use only NAND Gates or only NOR Gates to realize any basic gates. Hence these two gates are called as universal gates.
2. The NOT-AND operation is known as NAND operation. If all inputs are 1 then output produced is 0. NAND gate is inverted AND gate.
   Y = (A. B)'
3. The NOT- OR operation is known as NOR operation. If all the inputs are 0 then the O/P is 1. NOR gate is inverted OR gate. Y = (A+B)'
4. The NOR gate has two or more input signals but only one output signal.
5. An EX-OR Gate is a gate with two or more inputs and one output. The output is a logic 1 only when there are odd number of 1's at the input.

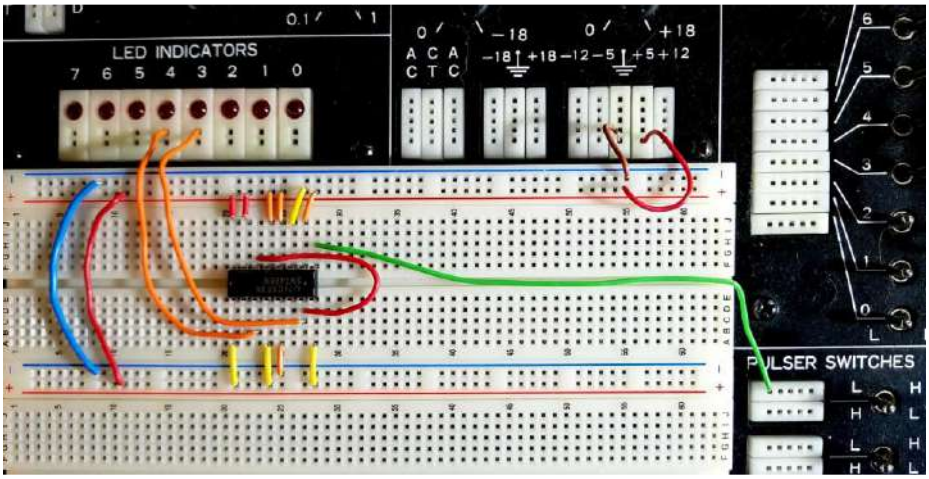
Y=A'B+AB'

4. Procedure

1. Take the digital trainer kit and insert the 7400IC at appropriate position.
2. Connect pin no 14 to v_{cc} and pin no 7 to ground.
3. Connect the circuit diagram as shown in figure
4. Switch on the trainer kit,
5. Apply various input combinations and observe output for each one.
6. Verify the truth table of EX-OR gate.
7. Insert the 7402 IC at appropriate position.
8. Connect pin no 14 to v_{cc} and pin no 7 to ground.
9. Connect the circuit diagram as shown in figure
10. Switch on the trainer kit,
11. Apply various input combinations and observe output for each one.
12. Verify the truth table of EX-OR gate.

5. Precautions

1. IC should not be reversed.
2. Make the connections according to the IC pin diagram.
3. The connections should be tight.
4. The VCC and ground should be applied carefully at the specified pins only.
5. Before making changes in the circuit turn off or disconnect the power.
6. When hooking up a circuit, connect to the power source last, while power is off.
7. Always keep your work area should be dry.
8. Insert ICs in the middle of bread board as shown below carefully to avoid short circuits between IC pins.



HALF ADDER AND FULL ADDER

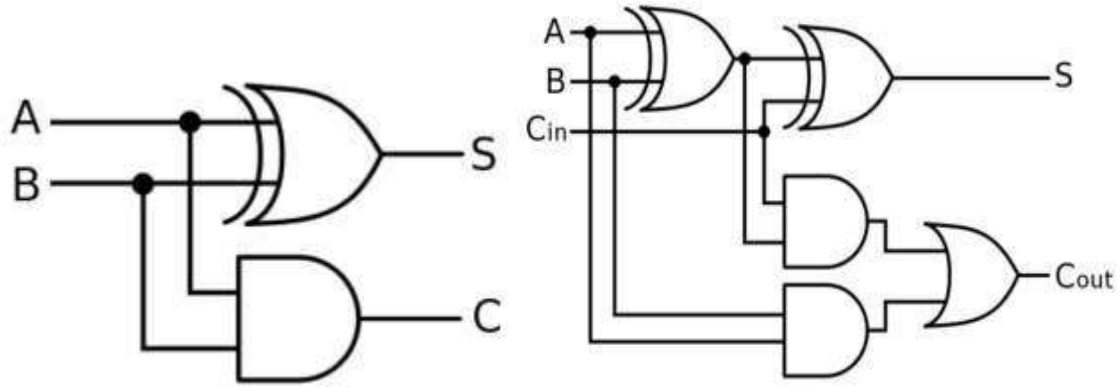
Description:

1. The setup for this experiment requires the following equipment:

SNo.	Name	No.	Purpose
1	Digital IC Trainer Kit	1	To provide inputs, outputs, bread board, supply, ground, etc
2	IC 7408 (AND Gate)	1	Provides Four two input AND gates
3	IC 7432 (OR Gate)	1	Provides Four two input OR gates
4	IC 7486 (EX-OR Gate)	1	Provides Four two input EX-OR gates
5	Patch Chords/Connecting Wires		For giving connections

Circuit diagram:

Half adder : Full adder:



Theory:

1. A Half adder can add two bits at a time.

2. Its outputs are SUM and CARRY.

3. For two bit addition- SUM will be 1, if only one input is 1(X-OR operation).

4. CARRY will be one, when both inputs are 1 (AND operation).

5. So, by using one AND gate and one X-OR gate, a half adder circuit can be constructed.

SUM = AB' + A'B

CARRY = AB

6. A full adder is a combinational circuit that performs the arithmetic sum of three inputs and gives two outputs.

7. A full adder is useful to add three bits at a time but a half adder cannot do so.

8. In full adder sum output will be taken from X-OR Gate, carry output will be taken from OR Gate.

Procedure:

1. Connect the trainer kit to ac power supply.

2. Connect logic sources to the inputs of the adder.

3. Connect output from SUM and CARRY to logic indicators.

4. Apply various input combinations to the adder.

5. Observe the SUM and CARRY outputs, verify the truth table for each input/ output combination.

6. Switch off the ac power supply.

Truth tables:

Half adder **:**

Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

full adder:

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

PRECAUTIONS :

- Disconnect all the equipment from mains before making connections.
- Connect the circuit as per circuit diagram.
- Loose connections should be avoided.
- Get the connections checked by the concerned staff member.
- Give required supply voltage to the circuit.

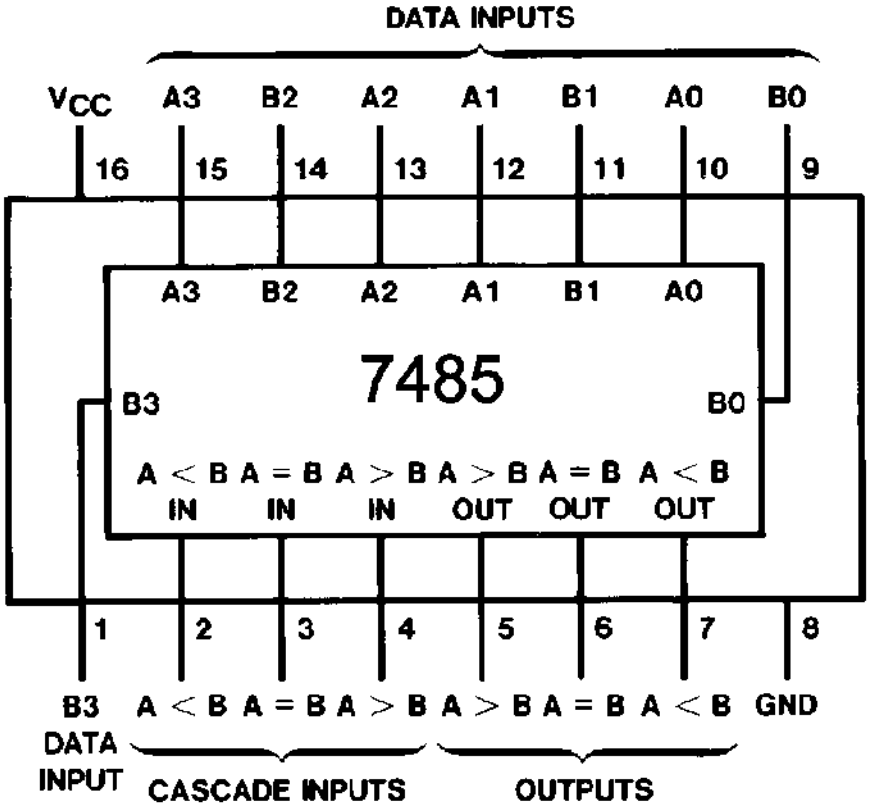
4-Bit MAGNITUDE COMPARATOR (IC 7485)

4.7.1 DESCRIPTION:

The setup for this experiment requires the following equipment

NAME	SPECIFICATIONS/ RANGE	NO	PURPOSE
Comparator IC	7485	1	To compare 4-Bit numbers
IC trainer kit	Minimum of 10 logic inputs and 3 logic outputs, power supply 0-5V	1	To connect the circuit on kit as per circuit
Patch cards	Different colors	As per need	To make the connections

4.7.2 CIRCUIT DIAGRAM:



4.7.3 THEORY:

A digital comparator or magnitude comparator is a hardware electronic device that takes two numbers as input in binary form and determines whether one number is greater than, less than or equal to the other number.

The 4-bit magnitude comparators perform comparison of straight binary or BCD codes. The two 4-bit numbers are A=A3A2A1A0 and B3B2B1B0 where A3 and B3 are the most significant bits. Three fully-decoded decisions about two, 4-bit words (A, B) are made and are externally available at three outputs, one each for equality (A=B), greater than (A>B) and less than (A<B).

The 4-bit comparator is mostly available in IC form and common type of this IC is 7485. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding inputs of the next stage handling more-significant bits. The stage handling the least significant bits must have a high-level voltage applied to the A = B input.

4.7.4 PROCEDURE:

1. Connections are made as per pin diagram
2. Connect Vcc and ground pins of IC at 5V and ground points respectively
3. Connect the inputs A0 B0 A1B1 A2 B2 A3 B3 to the concerned inputs
4. Connect the outputs to LEDs
5. Switch ON the power supply
6. Apply inputs and observe the outputs by supporting of truth table

4.7.4 OBSERVATIONS:

Comparing inputs								Cascading inputs			Outputs		
A_3,	B_3	A_2,	B_2	A_1,	B_1	A_0,	B_0	$A>B$	$A<B$	$A=B$	$A>B$	$A<B$	$A=B$
$A_3 > B_3$		×		×		×		×	×	×	1	0	0
$A_3 < B_3$		×		×		×		×	×	×	0	1	0
$A_3 = B_3$		$A_2 > B_2$		×		×		×	×	×	1	0	0
$A_3 = B_3$		$A_2 < B_2$		×		×		×	×	×	0	1	0
$A_3 = B_3$		$A_2 = B_2$		$A_1 > B_1$		×		×	×	×	1	0	0
$A_3 = B_3$		$A_2 = B_2$		$A_1 < B_1$		×		×	×	×	0	1	0
$A_3 = B_3$		$A_2 = B_2$		$A_1 = B_1$		$A_0 > B_0$		×	×	×	1	0	0
$A_3 = B_3$		$A_2 = B_2$		$A_1 = B_1$		$A_0 < B_0$		×	×	×	0	1	0
$A_3 = B_3$		$A_2 = B_2$		$A_1 = B_1$		$A_0 = B_0$		1	0	0	1	0	0
$A_3 = B_3$		$A_2 = B_2$		$A_1 = B_1$		$A_0 = B_0$		0	1	0	0	1	0
$A_3 = B_3$		$A_2 = B_2$		$A_1 = B_1$		$A_0 = B_0$		0	0	1	0	0	1
$A_3 = B_3$		$A_2 = B_2$		$A_1 = B_1$		$A_0 = B_0$		×	×	1	0	0	1
$A_3 = B_3$		$A_2 = B_2$		$A_1 = B_1$		$A_0 = B_0$		1	1	0	0	0	0
$A_3 = B_3$		$A_2 = B_2$		$A_1 = B_1$		$A_0 = B_0$		0	0	0	1	1	0

4.7.5 PRECAUTIONS:

1. Ensure that pin 16 and 3 connected to supply(5V)
2. Ensure pin 8, 2 and 4 connected to ground
3. Avoid loose connections
4. While connect the circuit on board power should be off
5. Power should be off before change the connections

MULTIPLEXER

Description:

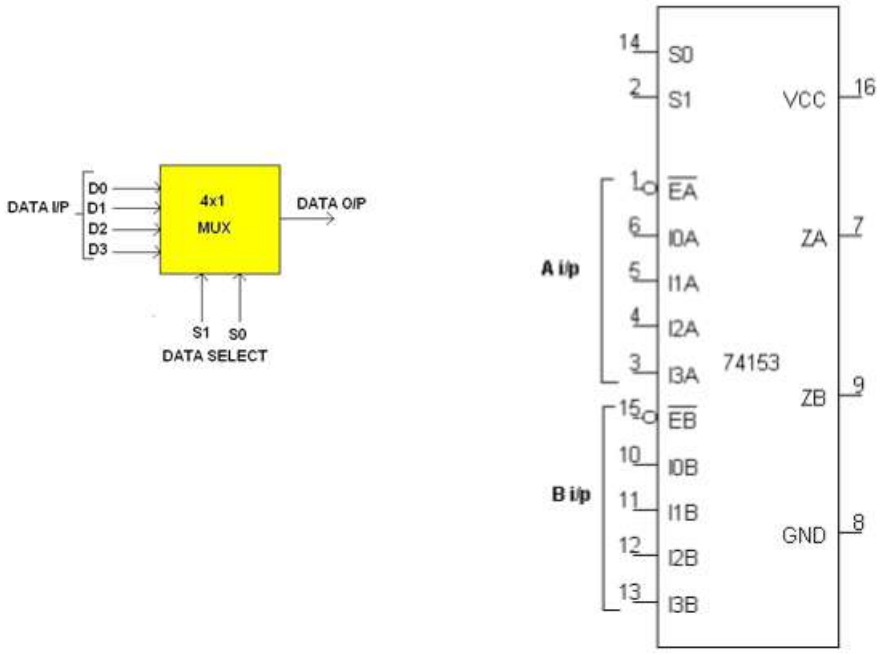
1. The experiment setup requires Digital trainer board and Multiplexer IC 74153.

2. Digital Trainer is a general-purpose digital experiment board equipped with Breadboard, Logic Level Inputs, and LEDs for output indication, built-in fixed 5V DC power supply and clock sections.

3. Inputs can be applied to by changing the position (logic level) of switches.

4. Truth table can be verified by varying possible inputs and observing the illuminated output LEDs.

Circuit Diagram:



Truth table:

Enable	Data Input Lines				Selection Lines		Output
$\overline{EA}$	I_{0A}	I_{1A}	I_{2A}	I_{3A}	S_1	S_0	Z_A
1	X	X	X	X	X	X	0
0	0	X	X	X	0	0	0
0	1	X	X	X	0	0	1
0	X	0	X	X	0	1	0
0	X	1	X	X	0	1	1
0	X	X	0	X	1	0	0
0	X	X	1	X	1	0	1
0	X	X	X	0	1	1	0
0	X	X	X	1	1	1	1

Theory:

1. The multiplexer, shortened to "**MUX**" or "MPX", is a combinational logic circuit designed to switch one of several input lines through to a single common output line by the application of a control signal.
2. Multiplexers are also known as data selectors because they can "select" each input data line.
3. The selection of each input line in a multiplexer is controlled by an additional set of inputs called **Select line**s.
4. A multiplexer has an even number of 2^n **data input** lines where n is number of "select" inputs

Procedure:

1. Fix the IC on the bread board.

2. Make connection according to the circuit.

3. Connect select lines and data input lines to toggle switches (either channel A or B).

4. Connect +5V (V_{cc}) supply at pin no 16 & GND at pin no 8.

5. Apply various combinations of input according to truth table.

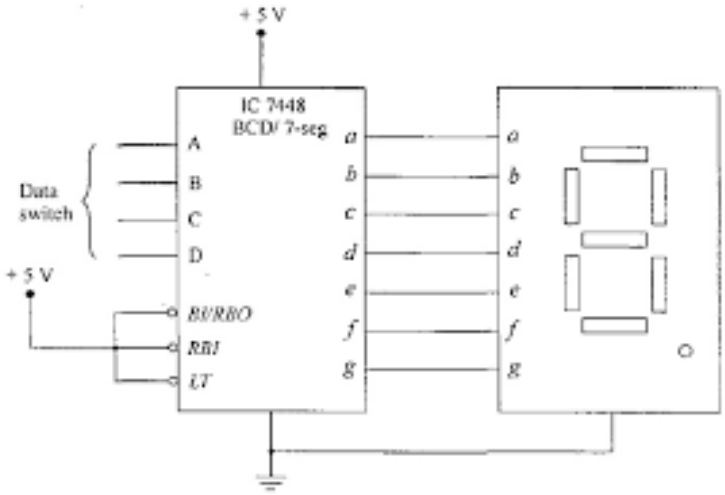
6. For all input combinations observe the outputs and verify with the truth table.

BCD TO SEVEN SEGMENT DECODER USING IC 7448

1. DESCRIPTION:

1. The set up for this experiment requires digital trainer kit along with bread board.
2. IC 7448 is used.
3. Common anode seven segment display is used.

2. CIRCUIT DIAGRAM:



3. THEORY:

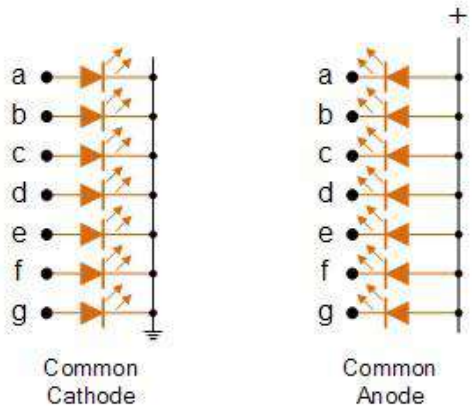
A **Digital Decoder** IC, is a device which converts one digital format into another and one of the most commonly used devices for doing this is called the Binary Coded Decimal (BCD) to 7-Segment Display Decoder.

Typically 7 segment decoder consist of seven individual colored LED's (called the segments), within one single display package. In order to produce the required numbers or HEX characters from 0 to 9 and A to F respectively, on the display the correct combination of LED segments need to be illuminated and **BCD to 7-segment Display Decoders** such as the 74LS48 do just that.

A standard 7-segment LED display generally has 8 input connections, one for each LED segment and one that acts as a common terminal or connection for all the internal display segments. Some single displays have also have an additional input pin to display a decimal point in their lower right or left hand corner.

In electronics there are two important types of 7-segment LED digital display.

- 1. THE COMMON CATHODE DISPLAY (CCD) – In the common cathode display, all the cathode connections of the LED's are joined together to logic "0" or ground. The individual segments are illuminated by application of a "HIGH", logic "1" signal to the individual Anode terminals.
- 2. THE COMMON ANODE DISPLAY (CAD) – In the common anode display, all the anode connections of the LED's are joined together to logic "1" and the individual segments are illuminated by connecting the individual Cathode terminals to a "LOW", logic "0" signal.



4. PROCEDURE:

1. Connect 5V and ground to their indicated position on digital trainer kit.

2. Connect BCD inputs A, B, C, D to the pin of IC 74LS48 as shown in logic diagram

3. Connect +5V to Pins 3, 4, 5 of IC 74LS48.

4. Connect pins 13-a, 12-b, 11-c, 10-d, 9-e, 15-f, 14-g of common anode display respectively.

4. Switch on the power supply.

5. Observe decimal output on common anode display given on the experiment board.

5. OBSERVATIONS:

4.7(a) Experimental Methodology IC 74138 Decoder

BCD Inputs				Segment Outputs							Display
A	B	C	D	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	1	1	0	1	0	0	1
0	0	1	0	1	1	0	1	1	0	1	2
0	0	1	1	1	1	1	1	0	0	1	3
0	1	0	0	0	1	1	0	0	1	1	4
0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	1	1	0	0	1	1	9

VERIFY THE TRUTH TABLE OF 74138 DECODER IC

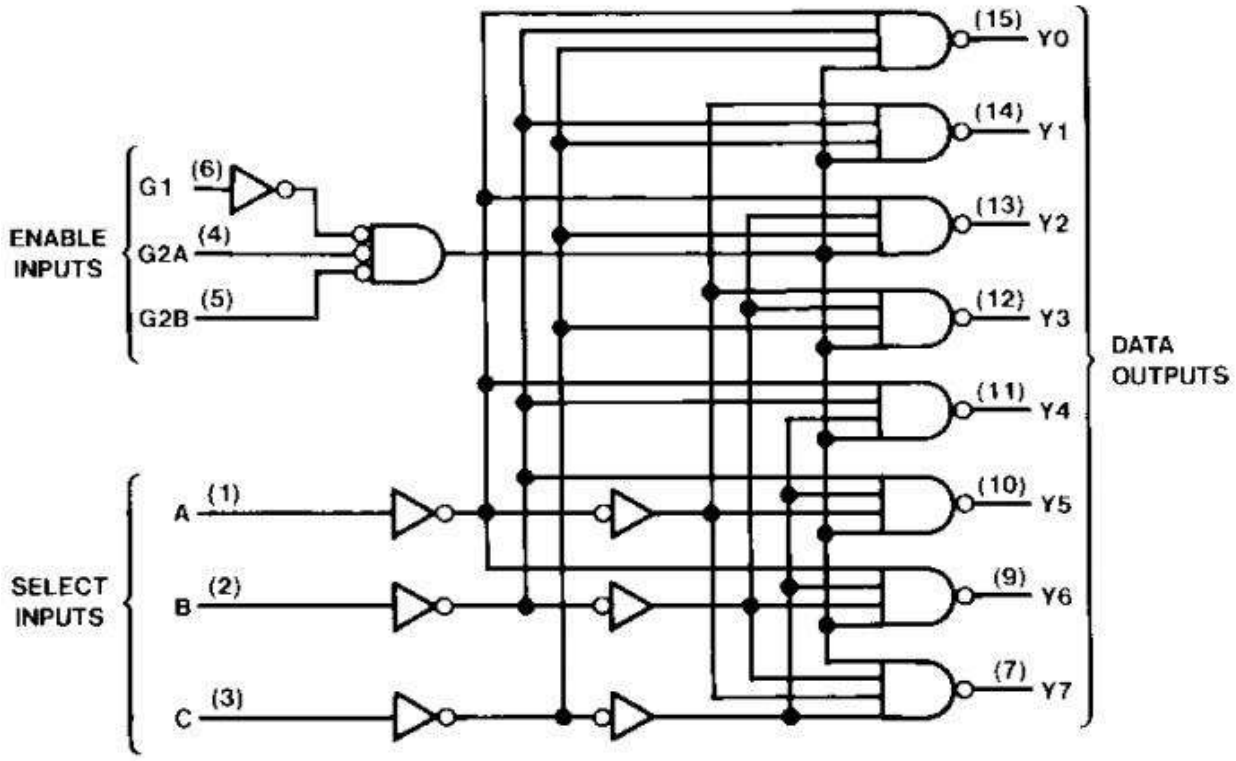
1. Description:

The setup for this experiment requires the following equipments

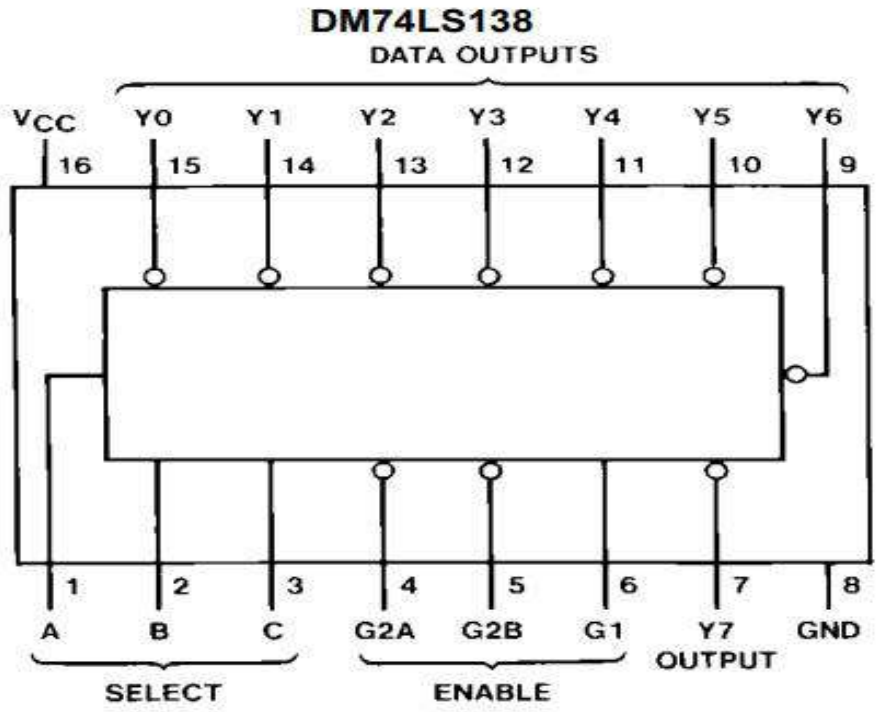
1. This experiment requires IC trainer kit, and counter IC.
2. IC number is 74138.
3. Learn the pin description of integrated circuit.
4. Always inputs are given in the form of 0's and 1's

2. Theory:

The 74138 circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.



3. Pin diagram:



The decoder accepts three binary weighted inputs (A, B, C) and when enabled provides eight mutually exclusive active LOW Outputs (Y_0–Y_7). The 74LS138 features three Enable inputs, two active LOW (G_{2A}, G_{2B}) and one active HIGH (G_1). All outputs will be HIGH unless G_{2A} and G_{2B} are LOW and G_1 is HIGH.

As shown in table first three rows the enable pins needed to be connected appropriately or irrespective Of input lines all outputs will be high. After connecting the enable pins as shown in circuit diagram you Can use the input line to get the output.

4. Procedure:

1. Connections are made as per the logic circuits.

2. Connect V_{CC} and GND (ground) pins of ICs at +5V and ground points of IC Trainer Kit respectively.

3. Connect inputs A, B, C on the IC trainer kit.

4. Connect enable inputs G_1, G2A, G2B on the IC trainer kit.

5. Connect the outputs Y_0, Y1, Y2, Y3, Y4, Y5, Y6, and Y7 to output LEDs.

6. Switch ON the power supply.

7. Apply G_1 is logic High and G_{2A} and G_{2B} are logic low

8. Apply different combination of inputs and observe the outputs.

9. Hence, verify the truth table.

5. Truth table:

Inputs					Outputs							
Enable		Select										
G1	G2 (Note 1)	C	B	A	YO	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Here we have used a single device so the connections of **G2A, as well as G2B pins, are connected to GND** followed by linking G1-to-VCC for activating the chip. Here three buttons signify three i/p lines for this device. For a better understanding of this concept, let us understand the following truth table. In the above tabular form, the H-HIGH, L-LOW and X- don't care. The enable pins G1, G2A, and G2B, where G2=G2A + G2B.In the above tabular form, the first rows namely G1, G2 are the enable pins required to be connected correctly otherwise irrespective of all i/p, as well as o/p lines, will be high. Once the enable pins are connected, then the input line can be connected for getting the output.

Applications: Decoder used applications are

1. Line decoders
2. Servers
3. Digital systems
4. Line De-multiplexing
5. Telecom circuits
5. Memory circuits

Precautions:

1. Ensure the correct IC .
2. Ensure that IC 74138 Pin 14 connected to power supply..
3. Ensure that IC 74138 Pin 7 connected to ground.
4. Connect the circuit as per circuit diagram.
5. Loose connections should be avoided.
6. Get the connections checked by the concerned staff member.

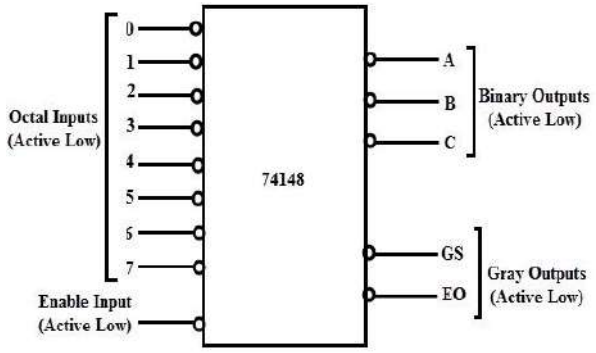
Function of Encoder using IC 74148

1. Description

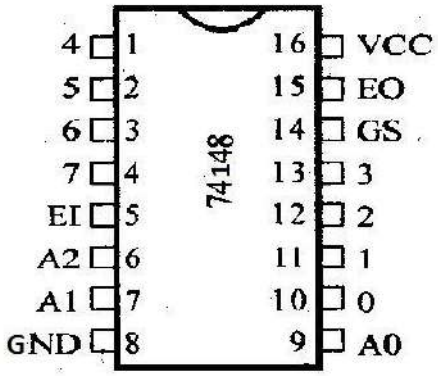
i. The set up for this experiment requires a **74148 IC, Digital logic trainer kit**

ii. IC's are available in laboratory and by using these IC'S we can verify the truth tables

2. Circuit diagram/Pin diagram



a. Circuit diagram



b. Pin diagram

3. Theory

1. An encoder is a combinational **digital logic circuit.**
2. A digital encoder has commonly called as a **binary encoder.**
3. It accepts an active level on one of its input represents a **digit** (decimal or octal) and converts into **a coded output** (binary or BCD).
4. These encoders is used as a **code converters.**
5. Encoder has a $\mathbf{2^n}$ inputs and **n** outputs.

4. Procedure

20. Take the digital trainer kit and insert **the 74148IC** at appropriate position.
21. Connect pin no **16 to v_{cc}** and pin no **8 to ground**.
22. Connect the circuit diagram as shown in figure.
23. Switch on the **trainer kit**.
24. The **octal inputs** are given at the corresponding **pins.**
25. The outputs are verified at the corresponding **output pins**.

5. Truth table for Encoder:

INPUTS									OUTPUTS		
EI	0	1	2	3	4	5	6	7	A2	A1	A0
H	X	X	X	X	X	X	X	X	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H
L	X	X	X	X	X	X	X	L	L	L	L
L	X	X	X	X	X	X	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	H	L
L	X	X	X	X	L	H	H	H	L	H	H
L	X	X	X	L	H	H	H	H	H	L	L
L	X	X	L	H	H	H	H	H	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L
L	L	H	H	H	H	H	H	H	H	H	H

6. Precautions:

1. Ensure that pin 14 connected to supply.
2. Ensure that pin 7 connected to ground.
3. All connections should be made properly.
4. IC should not be reversed.
5. Power supply should not exceed 5V.
6. Never work on a circuit while power is applied.
7. Always keep your work area should be dry.

CLOCKED RS FLIP FLOP

1. Description

i. The set up of this experiment requires a **7400 IC**, Digital **trainer kit**

ii. The digital trainer kit consists of bread board, power supply, toggle switches, LED's, Pulses.

iii. Observing the **pin** description of **IC**'s.

2. Circuit diagram

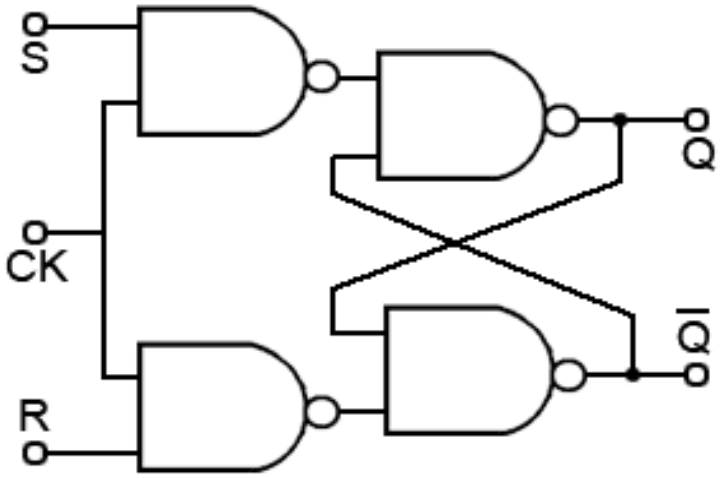


Fig:1 Clocked RS flip-flop using NAND gates

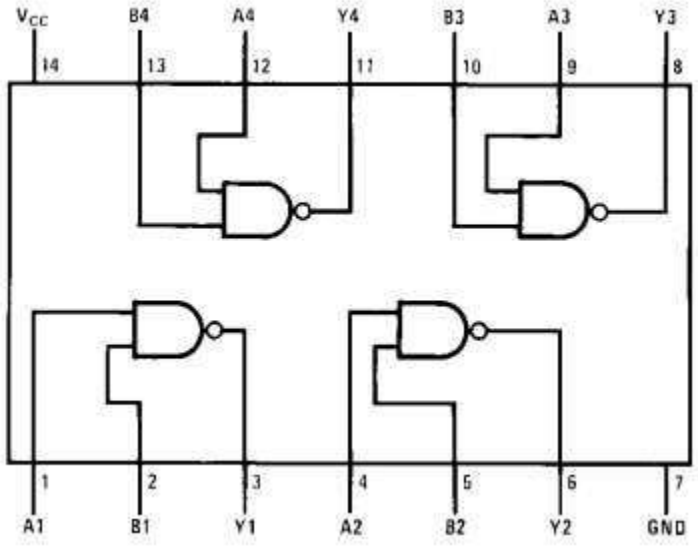


Fig: 2 pin diagram of IC 7400

3. Truth table of RS Flip-flop:

INPUTS			OUTPUT		STATE
CLK	S	R	Q	$\overline{Q}$	
X	0	0	NC	NC	NO CHANGE
↑	0	1	0	1	RESET
↑	1	0	1	0	SET
↑	1	1	-	-	FORBIDDEN

4. Theory

1. There are two inputs to the flip-flop defined as **R** and **S**.
2. When inputs R = 0 and S = 0 then O/P remains **unchanged.**
3. When inputs R = 0 and S = 1 the flip-flop is switches to the stable state where O/P is 1 i.e. **SET.**
4. The input condition is R = 1 and S = 0 the flip-flop is switched to the stable state where output is 0 i.e. **RESET**.
5. The input condition is R = 1 and S = 1 the flip-flop is switched to the stable state where output is **FORBIDDEN**

5. Procedure

1. Take the digital trainer kit and insert the **7400IC** at appropriate position.
2. Connect pin **14** to $\mathbf{V_{cc}}$ and pin **7** to **ground**.
3. Connect the circuit diagram as shown in figure
4. Give the clock input from **pulser**.
5. Switch on the trainer kit,
6. Apply various input combinations and observe output for each one.

6. Verify the truth table of RS Flip-flop.

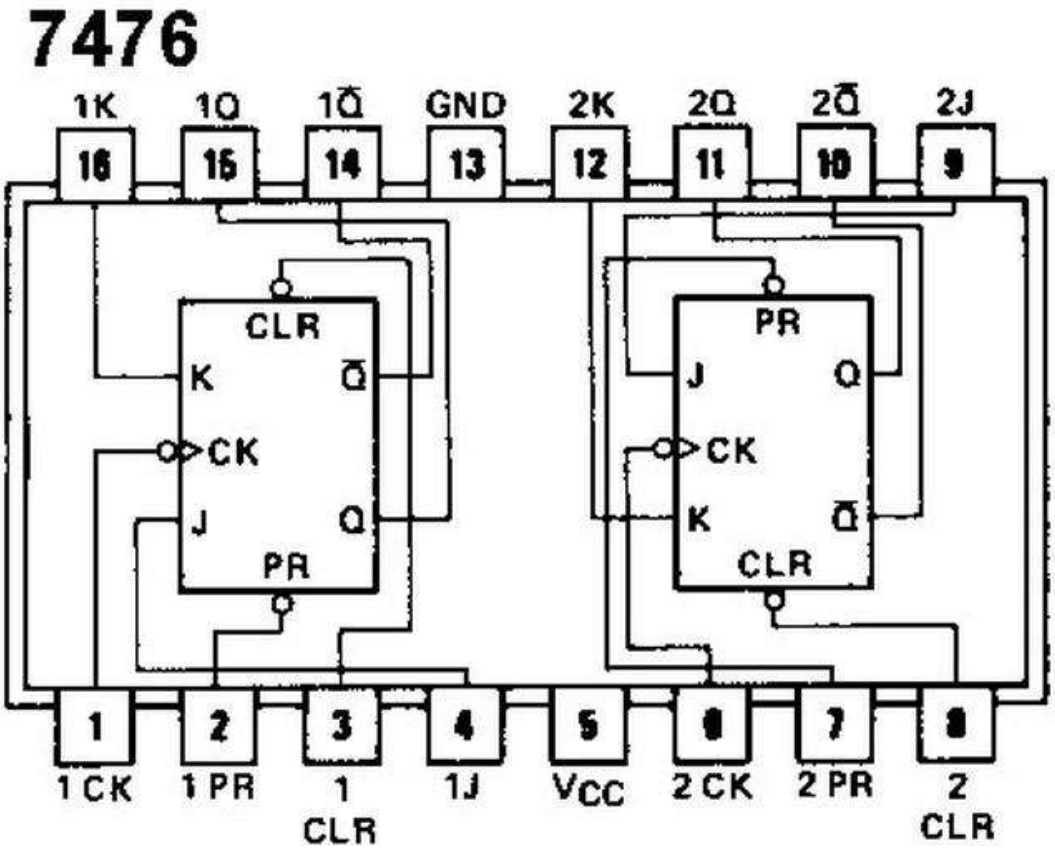
INPUTS			OUTPUT		STATE
CLK	S	R	Q	$\overline{Q}$	
X	0	0	NC	NC	NO CHANGE
↑	0	1	0	1	RESET
↑	1	0	1	0	SET
↑	1	1	-	-	FORBIDDEN

7. Precautions:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The Vcc and ground should be applied carefully at the specified pin only.
4) Before making changes in a circuit, turn off or disconnect the power first.
5) When hooking up a circuit, connect to the power source last, while power is off.

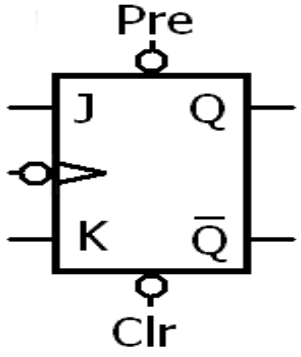
J K FLIP FLOP USING IC 7476

1. **Description:**
   1. The setup for this experiment requires IC 7476 and Digital logic trainer kit.
   2. IC 7476 is a DIP 16-Pin Dual J_K flip flop with Preset and clear.
   3. Digital logic trainer kit provides logic input switches for applying logic inputs and logic output LED indicators for observing output logic.
2. **Circuit diagram**:



a) J K Flip flop

Symbol:



b) symbol

3. **Theory**:
    1. IC 7476 is a **Dual JK flip flop**.
    2. This simple **JK flip Flop** is the most widely used of all the flip-flop designs and is considered to be a universal flip-flop circuit.
    3. When both J and K are 0, the clock pulse has no effect on the output and the output of the flip-flop is the same as its previous value.
    4. When J=0, K=1, Therefore Q becomes 0. This condition will reset the flip-flop. This represents the RESET state of Flip-flop.
    5. When J=1, K=0, Therefore Q becomes 1. This condition will set the flip-flop. This represents the SET state of Flip-flop.
    6. when both the J and the K inputs are at logic level "1" at the same time, and the clock input is pulsed "HIGH", the circuit will "toggle" from its SET state to a RESET state, or visa-versa. This results in the JK flip flop acting more like a T-type toggle flip-flop when both terminals are "HIGH".

4. **Procedure**:
    1. Make the connections as shown in circuit diagram.
    2. Feed the logic signal from the logic input switches.
    3. Observe the logic outputs on the logic level LED indicators.
    4. Observe the output for all possible input combinations.
    5. Verify the corresponding truth table.

5. Truth table of Negative edge triggered JK flip-flop

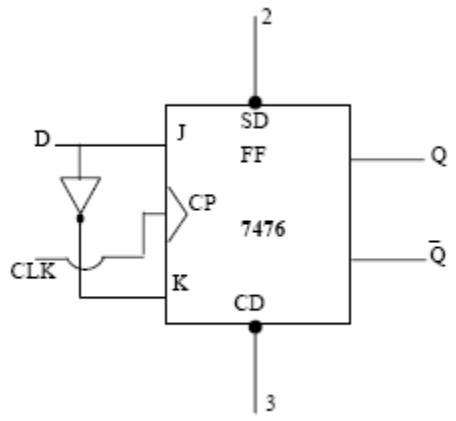
Mode of operation	INPUTS					OUTPUTS	
	Asynchronous		Synchronous				
	PS	*CLR*	*CLK*	*J*	*K*	*Q*	$\overline{Q}$
Asynchronous set	0	1	X	X	X	1	0
Asynchronous reset	1	0	X	X	X	0	1
Prohibited	0	0	X	X	X	1	1
Hold	1	1	↓	0	0	No change	
Reset	1	1	↓	0	1	0	1
Set	1	1	↓	1	0	1	0
Toggle	1	1	↓	1	1	Opposite state	

0 = LOW
1 = HIGH
X = Irrelevant
↓ = HIGH-to-LOW clock transition

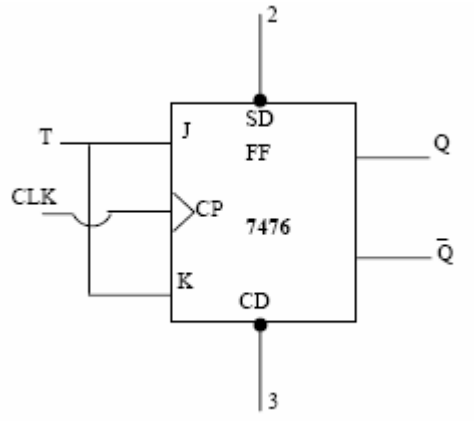
(c)

D and T flip flops using IC 7476

1. **Description**:
   1. The setup for this experiment requires IC 7404, IC 7476 and Digital logic trainer kit.
   2. IC 7404 is a DIP 14-PIN NOT gate IC which provides Hex inverting gates.
   3. We can use any one of the Hex inverting gates.
   4. IC 7476 is a DIP 16-Pin Dual J_K flip flop with Preset and clear.
   5. Digital logic trainer kit provides logic input switches for applying logic inputs and logic output LED indicators for observing output logic.
2. **Circuit diagram**:



D Flip flop



T Flip flop

3. **Theory**:
   1. IC 7476 is a **Dual JK flip flop**.
   2. By connecting D input to J input and inverting of D input to K input of JK flip flop, we get D flip flop operation.
   3. By connecting T input to both J and K inputs of JK flip flop, we get T flip flop operation.
   4. The D flip-flop is widely used. It is also known as a "**data" or "delay" flip-flop.**
   5. The D flip-flop captures the value of the D-input at a definite portion of the clock cycle (such as the rising edge of the clock). That captured value becomes the Q output. At other times, the output Q does not change.
   6. The D flip-flop can be viewed as a **memory cell**.
   7. Most D-type flip-flops in ICs have the capability to be forced to the **set or reset state.**
   8. These flip-flops are very useful, as they form the basis for shift registers.
   9. If the T input is high, the T flip-flop changes **state ("toggles")** whenever the clock input is **strobed.**
   10. If the T input is low, the flip-flop holds the previous value.
   11. When T is held high, the toggle flip-flop divides the clock frequency by two.
   12. This "divide by" feature has application in various types of **digital counters**.

4. **Procedure**:

1. Make the connections as shown in circuit diagram.
2. Feed the logic signal from the logic input switches.
3. Observe the logic outputs on the logic level LED indicators.
4. Observe the output for all possible input combinations.
5. Verify the corresponding truth table.

5. Observations:

S.No	Clock input	Switch condition (For D input)	LED 1 Status (For Q Output)	LED 2 Status (For $\bar{Q}$ Output)
1	0	X	Q	$\bar{Q}$
2	↑	OFF	Doesn't Glow	Glow
3	↑	ON	Glow	Doesn't Glow

Interpretation of above Observations in terms of logic values.

S.No	Clock input	D input	Q Output	$\bar{Q}$ Output
1	0	X	Q	$\bar{Q}$
2	↑	0	0	1
3	↑	1	1	0

S.No	Clock input	Switch condition (For T input)	LED 1 Status (For Q Output)	LED 2 Status (For $\bar{Q}$ Output)
1	0	X	No change	No change
2	↑	OFF	No change	No change
3	↑	ON	Toggles	Toggles

Interpretation of above Observations in terms of logic values.

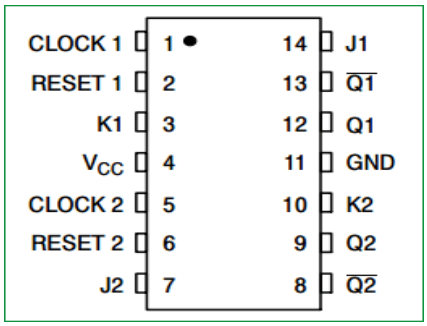
S.No	Clock input	T input	Q Output	$\bar{Q}$ Output
1	0	X	Q	$\bar{Q}$
2	↑	0	Q	$\bar{Q}$
3	↑	1	$\bar{Q}$	Q

RIPPLE COUNTER USING JK FLIPFLOP

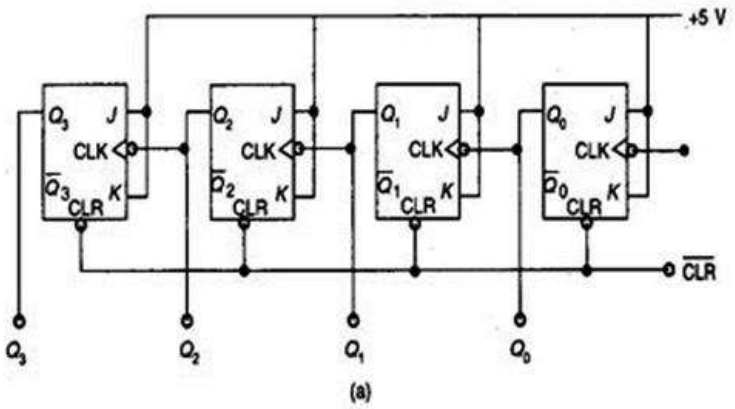
1. Description:

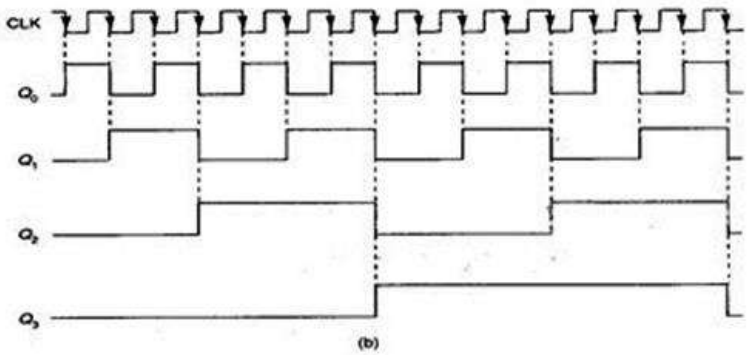
A. This experiment requires IC trainer kit, and counter IC.
B. IC number is 7476.
C. Learn the pin description of integrated circuit.
D. it is used to count the 16 values(0to 15).

2. Pin diagram of 7476 IC:



3. LOGIC DIAGRAM and WAVEFORMS:





Theory:

A counter is a sequential circuit that counts in a cyclic sequence. It is essentially a register that goes through a predetermined sequence of states upon the application of input pulses. There are two types of counters – Synchronous Counter & Asynchronous Counter.

Synchronous Counter:

In a synchronous counter, the input pulses are applied to all clock pulse inputs of all flip flops simultaneously (directly). Synchronous counter is also known as **parallel sequential circuit.**

Asynchronous Counter:

In an asynchronous counter, the flip flop output transition serves as a source for triggering other flip flops. In other words, the clock pulse inputs of all flip flops, except the first, are triggered not by the incoming pulses, but rather by the transition that occurs in previous flip flop's output.Asynchronous counter is also known as **serial sequential circuit**.

Procedure :

1. Connections are made as per the logic circuit.
2. Connect V and GND (ground) pins of ICs at +5V and ground points of IC Trainer Kit respectively.
3. Connect clock input (CLK) to clock pulse on the IC trainer kit.
4. Connect the outputs Q_0, Q_1, Q2,Q3 . to output LEDs.
5. Switch ON the power supply.
6. Apply logic 1 to JK inputs of four flipflops.
8. Apply clock pulse one by one and observe the outputs.
9. Hence, verify the truth table.
10. Obtain the wave forms.

Truth table:

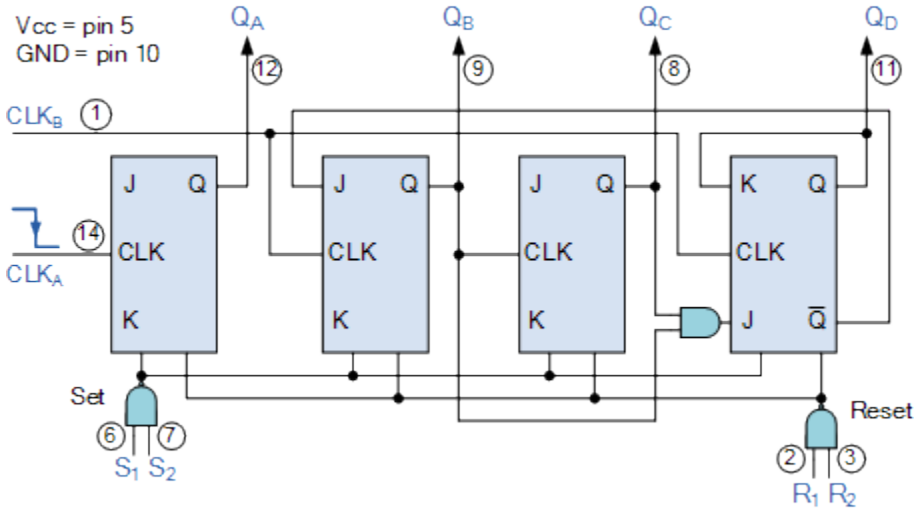
clk	Q_0	Q_1	Q_2	Q_3
1	0	0	0	0
2	0	0	0	1
3	0	0	1	0
4	0	0	1	1
5	0	1	0	0
6	0	1	0	1
7	0	1	1	0
8	0	1	1	1
9	1	0	0	0
10	1	0	0	1
11	1	0	1	0
12	1	0	1	1
13	1	1	0	0
14	1	1	0	1
15	1	1	1	0
16	1	1	1	1

DECADE COUNTER

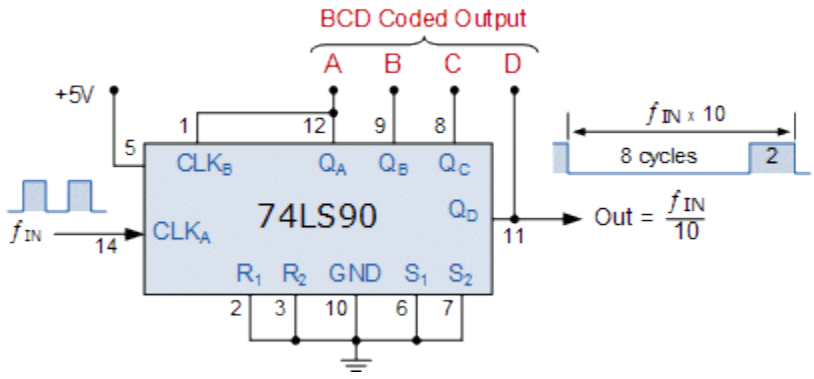
1. Description:

Name	Specifications	No	Purpose
Digital IC trainer kit	Power supply 230V 50Hz	1	To verify the function of 7490 as decade and modulus counter
IC 7490	Supply voltage 5V	1	To verify the function of 7490 as decade and modulus counter
Connecting wires		As per need	To make connections

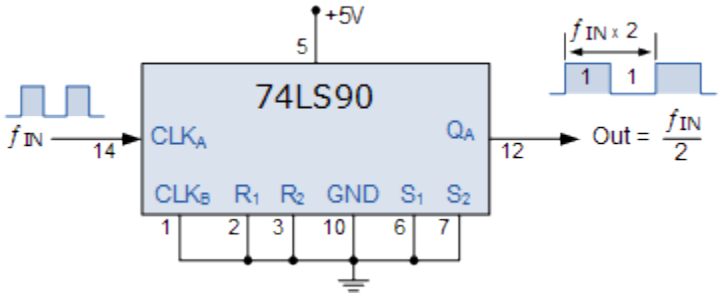
2. Circuit diagram:



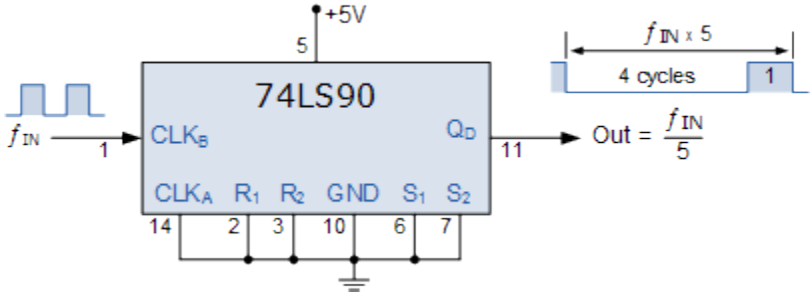
7490 Decade Counter:



7490 Divide-by-2 Counter:



74LS90 Divide-by-5 Counter:



3. Theory::

The 74LS90 integrated circuit is basically a MOD-10 decade counter that produces a BCD output code. The 74LS90 consists of four master-slave JK flip-flops internally connected to provide a MOD-2 (count-to-2) counter and a MOD-5 (count-to-5) counter. The 74LS90 has one independent toggle JK flip-flop driven by the CLK A input and three toggle JK flip-flops that form an asynchronous counter driven by the CLK B input as shown.

74LS90 counter consists of a divide-by-2 counter and a divide-by-5 counter within the same package. Then we can use either counter to produce a divide-by-2 frequency counter only, a divide-by-5 frequency counter only or the two together to produce our desired divide-by-10 BCD counter.

With the four flip-flops making up the divide-by-5 counter section disabled, if a clock signal is applied to input pin 14 (CLKA) and the output taken from pin 12 (QA), we can produce a standard divide-by-2 binary counter for use in frequency dividing circuits as shown.

To produce a standard divide-by-5 counter, we can disable the first flip-flop above, and apply the clock input signal directly to pin 1 (CLKB) with the output signal being taken from pin 11 (QD) as shown.

4. Procedure:

1. **Place** the IC 7490 on the breadboard.

2. **Connect** V_{cc} and GND (ground) pins of ICs to +5V and ground points of IC Trainer Kit respectively.

3. **Connect** the clock input (CLK) to clock pulse on the IC trainer kit.

4. **Connect** the outputs Q_A Q_B,Q_C Q_D to **output LEDs**.

5. **Switch** on the power supply.

6. When connected to logic 1, **the Reset inputs** R1 and R2 reset the counter back to zero, 0 (0000).

7. When the **Set inputs** S1 and S2 are connected to logic 1, they Set the counter to maximum or 9 (1001) regardless of the actual count number or position.

8. **Count** operation starts when atleast one of the reset inputs and atleast one of the set inputs is connected to logic 0

9. A single stage BCD counter such as the 74LS90 counts from decimal 0 to decimal 9 and is therefore capable of counting up to a maximum of **nine pulses**

9. **Verify** the truth table for all the states of a decade counter.

5. Observations

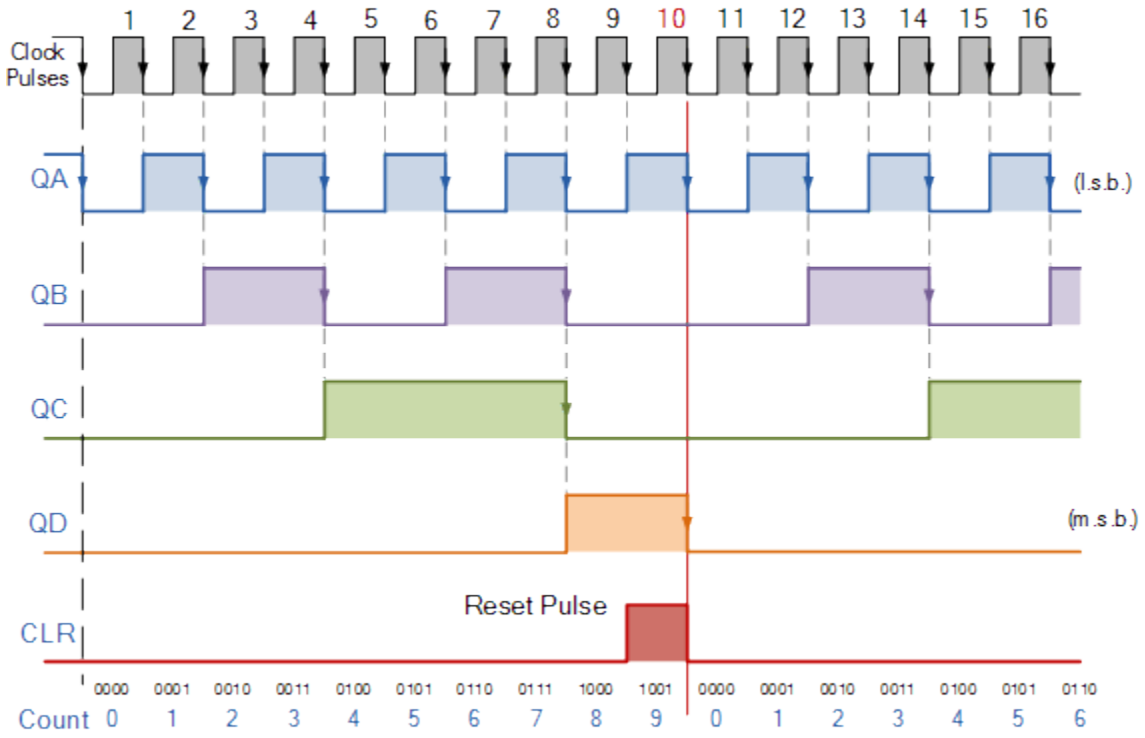
Count Truthtable:

Inputs				**Outputs**			
R_1	R_2	S_1	S_2	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

Count sequence:

COUNT	**Q_D**	**Q_C**	**Q_B**	**Q_A**
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	0	0	0	0

6. Timing Diagrams

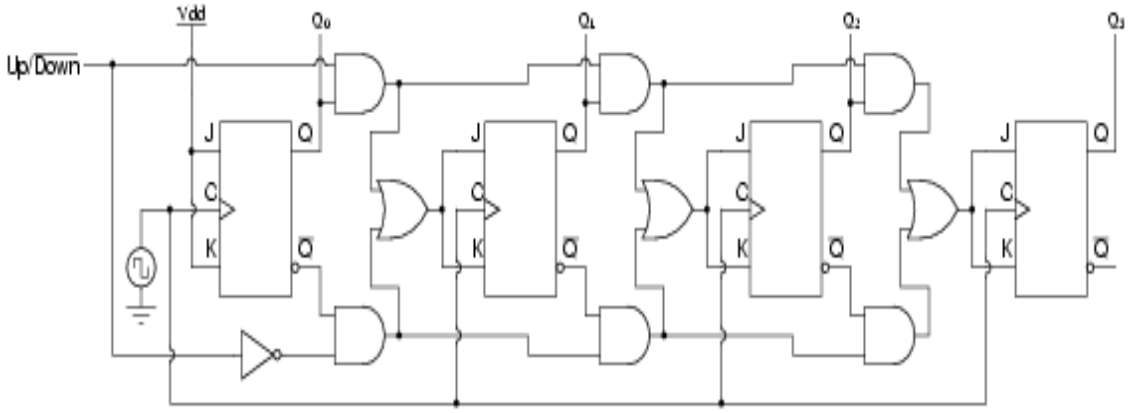


UP/DOWN COUNTER

1. **Description**

NAME	Specifications/Range	No	Purpose
Digital IC trainer kit	Equipped with Breadboard, Logic Level Inputs, LEDs for output indication, built-in fixed 5V DC power supply and clock sections	1	To conduct experiment on it
IC 74193	5V DC Supply	1	4 bit binary up/down counter
Patch chords		As per needed	To make connections
Connecting Wires		As per needed	To make connections

2. **Circuit Diagram:**



3. **Pin Diagram &Pin Description:**

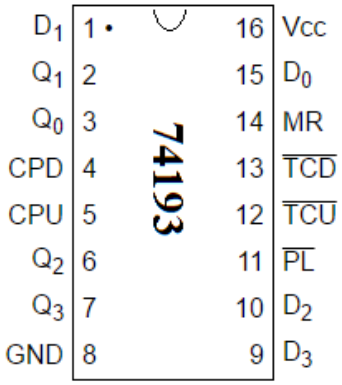


Figure: Pin Diagram of IC 74193

Pin Description:

Pin	Symbol	Description
1	D_1	data input
2	Q_1	counter output
3	Q_0	counter output
4	CPD	count down clock input (low-to-high, edge-triggered)
5	CPU	count up clock input (low-to-high, edge-triggered)
6	Q_2	counter output
7	Q_3	counter output
8	GND	ground
9	D_3	data input
10	D_2	data input
11	$\overline{PL}$	parallel load input (active low)
12	$\overline{TCU}$	terminal count up (carry) output (active low)
13	$\overline{TCD}$	terminal count down (borrow) output (active low)
14	MR	asynchronous master reset (active high)
15	D_0	data input
16	Vcc	supply voltage

4. **Theory:**

a) A counter is a circuit consisting of a number of Flip Flop and gates working together to count the number of clock pulses applied to its input.

b) Such counters are used in digital clocks, frequency counters, digital voltmeters, digital computers, and numerous other applications. The basic binary counter is probably the simplest to construct and form the basis for more advanced types of counters.

c) The 74193 is a synchronous up-down 4-bit binary counter. It has a master reset (MR), and it can be reset to any desired count with the parallel load inputs. Basically, it functions like any binary counter, except that is has two clock inputs, one for UP counting, and the other for DOWN counting.

d) Placing the clock on UP will cause the counter to count UP, and placing the clock on DOWN will cause the counter to count DOWN. Note that the clock should be connected to either UP or DOWN, but not both and the unused inputs should be held HIGH.

5. **Procedure:**

a) Locate IC 74193 on the trainer board.

b) Make connections as in the circuit diagram.

c) Take MR input to logic-1 and return it to Logic-0, this clears the counter.

d) Select appropriate mode (UP or DOWN) by connecting clock pulse to the corresponding pin.

e) Apply individual pulses and observe the change of states of a counter.

f) Take the readings.

6. **Observations**

Count-UP Mode:

Clock pulse	**Q_3**	**Q_2**	**Q_1**	**Q_0**
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Count-Down mode:

Clock pulse	**Q_3**	**Q_2**	**Q_1**	**Q_0**
0	1	1	1	1
1	1	1	1	0
2	1	1	0	1
3	1	1	0	0
4	1	0	1	1
5	1	0	1	0
6	1	0	0	1
7	1	0	0	0
8	0	1	1	1
9	0	1	1	0
10	0	1	0	1
11	0	1	0	0
12	0	0	1	1
13	0	0	1	0
14	0	0	0	1
15	0	0	0	0

SHIFT REGISTER

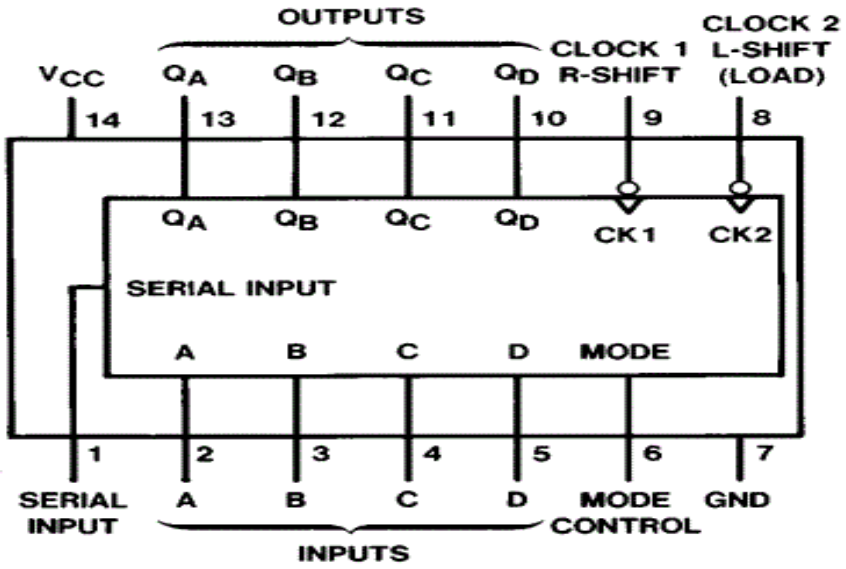
4.18.1. DESCRIPTION:

The setup for this experiment requires the following equipment

Name	Specifications/ Range	No	Purpose
Shift Register IC	7495	1	For shift operation
Digital trainer kit	Minimum of 10 logic inputs and 3 logic outputs	1	To connect input and output to IC
Patch cards	Different colors	15	To connect input and output to IC

4.18.2. CIRCUIT DIAGRAM:

PIN DIAGRAM of IC 7495:



4.18.3. THEORY:

Shift registers are a type of sequential logic circuit, mainly for storage of digital data. The 7495 IC is a 4-Bit Shift Register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel inputs to the Q outputs synchronous with the HIGH to LOW transition of the appropriate clock input.

The Serial In Serial Out (SISO) shift register accepts data serially – that is, one bit at a time on a single line. It produces the stored information on its output also in serial form.

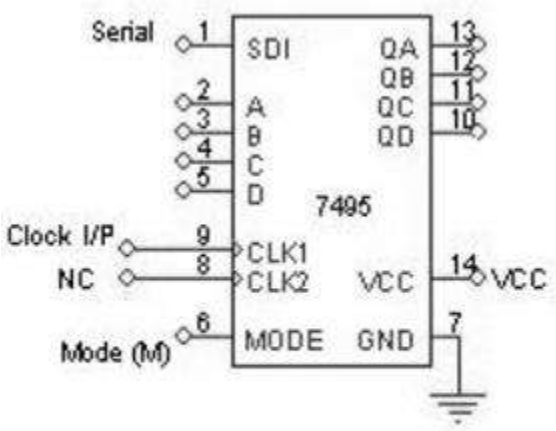
The Serial In Parallel Out (SIPO) shift register accepts data serially – that is, one bit at a time on a single line. It produces the stored information on its output in parallel form.

The Parallel In Serial Out (PISO) shift register accepts data in parallel. It produces the stored information on its output also in serial form.

The Parallel In Parallel Out (PIPO) shift register accepts data in parallel. It produces the stored information on its output in parallel form.

4.18.4. PROCEDURE:

4.18.4.1 Serial In Serial Out (SISO):



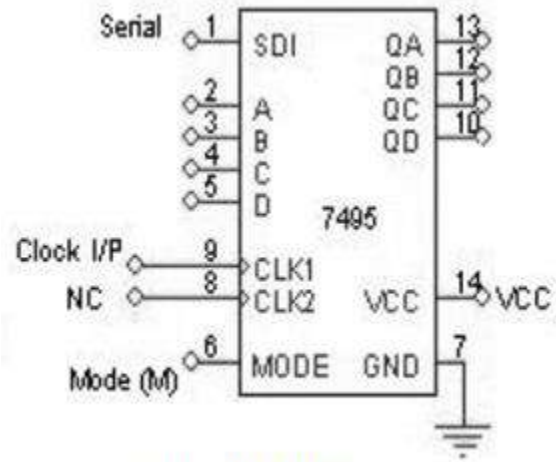
Circuit diagram

Clock	Serial i/p	QA	QB	QC	QD
1	do=0	0	X	X	X
2	d1=1	1	0	X	X
3	d2=1	1	1	0	X
4	d3=1	1	1	1	0=do
5	X	X	1	1	1=d1
6	X	X	X	1	1=d2
7	X	X	X	X	1=d3

Truth Table:

1. Connections are made as per circuit diagram.
2. Keep the mode control in logic 0
3. Load the shift register with 4 bits of data one by one serially.
4. At the end of 4th clock pulse the first data ‘d0’ appears at QD.
5. Apply another clock pulse; the second data ‘d1’ appears at QD and so on.
6. Thus the data applied serially at the input comes out serially at QD

4.18.4.2 Serial In Parallel Out (SIPO):



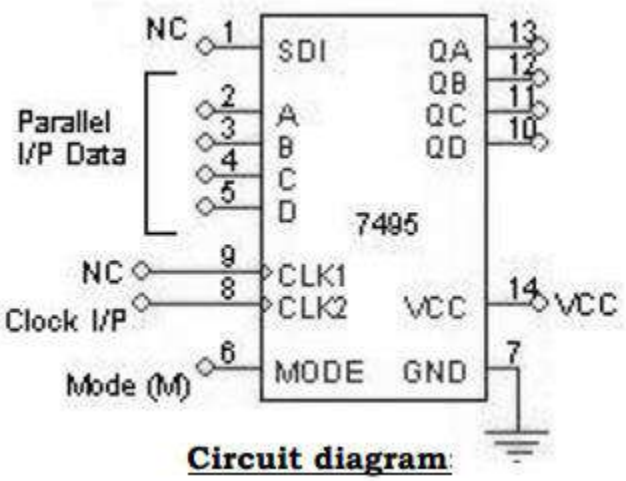
Circuit diagram

Clock	Serial i/p	QA	QB	QC	QD
1	0	0	X	X	X
2	1	1	0	X	X
3	1	1	1	0	X
4	1	1	1	1	0

Truth Table

1. Connections are made as per circuit diagram.
2. Keep the mode control in logic 0
3. Apply the data at serial input.
4. Apply one clock pulse at clock 1 observe this data at QA.
5. Apply the next data at serial input.
6. Apply one clock pulse at clock 2, observe that the data on QA will shift to QB and the new data applied will appear at QA.
7. Repeat steps 2 and 3 till all the 4 bits data appear at the output of shift register.

4.18.4.3 Parallel In Serial Out (PISO):



Circuit diagram

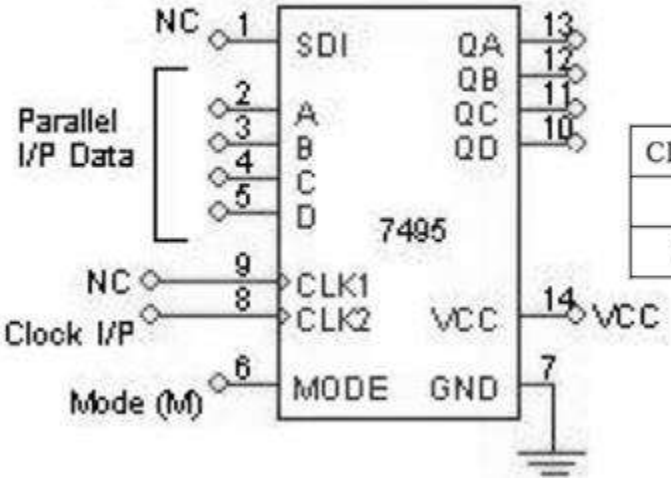
Mode	Clock	Parallel i/p				Parallel o/p			
		A	B	C	D	QA	QB	QC	QD
1	1	1	0	1	1	1	0	1	1
0	2	X	X	X	X	X	1	0	1
0	3	X	X	X	X	X	X	1	0
0	4	X	X	X	X	X	X	X	1

Truth Table

1. Connections are made as per circuit diagram.
2. Apply the desired 4 bit data at A, B, C and D.
3. Keeping the mode control M=1 apply one clock pulse. The data applied at A, B, C and D will appear at QA, QB, QC and QD respectively.
4. Now mode control M=0. Apply clock pulses one by one and observe the Data coming out serially at QD

4.18.4.4 Parallel In Parallel Out (PIPO):

Circuit diagram



Truth Table

Clock	Parallel i/p				Parallel o/p			
	A	B	C	D	QA	QB	QC	QD
1	1	0	1	1	1	0	1	1

1. Connections are made as per circuit diagram.
2. Apply the 4 bit data at A, B, C and D.
3. Apply one clock pulse at Clock 2 (Note: Mode control M=1).
4. The 4 bit data at A, B, C and D appears at QA, QB, QC and QD respectively.

4.18.5. OBSERVATIONS:

1. Shift registers hold the data in their memory which is moved or "shifted" to their required positions on each clock pulse.
2. Each clock pulse shifts the contents of the register one bit position to either the left or the right.
3. The data bits can be loaded one bit at a time in a series input (SI) configuration or be loaded simultaneously in a parallel configuration (PI).
4. Data may be removed from the register one bit at a time for a series output (SO) or removed all at the same time from a parallel output (PO).
5. One application of shift registers is in the conversion of data between serial and parallel, or parallel to serial.
6. Shift registers are identified individually as SIPO, SISO, PISO, PIPO, or as a Universal Shift Register with all the functions combined within a single device.

4.18.6 PRECAUSTIONS

- The circuit should be off before change the connections.
- While making connections main voltage should be kept switched off.
- After completing the experiment switch off the supply to apparatus.
- Digital lab kits should be handled with utmost care.

SIMULATION OF AND,OR ,NOT and EXOR GATES USING NAND GATES	Experimental methodology

SIMULATION OF AND, OR, NOT and EXOR GATES USING NAND GATES USING PSPICE

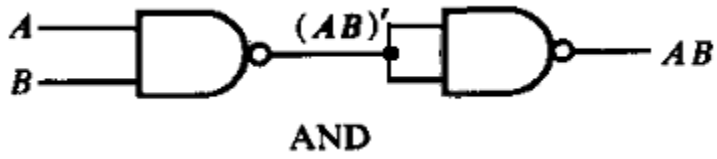
Description:

1. This experiment requires personal computer with Windows OS and ORCAD PSPICE 9.2 software package.
2. ORCAD PSPICE is Analog and Digital circuit simulation software
3. PSPICE contains both analog and digital circuit component library
4. The required components for an analog/digital circuit can be picked from the library
5. The circuit can be built by wiring the selected components, analog or digital sources
6. Circuit simulation can be done by applying required inputs. Then, the resulting outputs can be observed

7. AND, OR & NOT gates are basic gates with one or two inputs and one output. Can construct these gates by using universal gates (NAND&NOR).

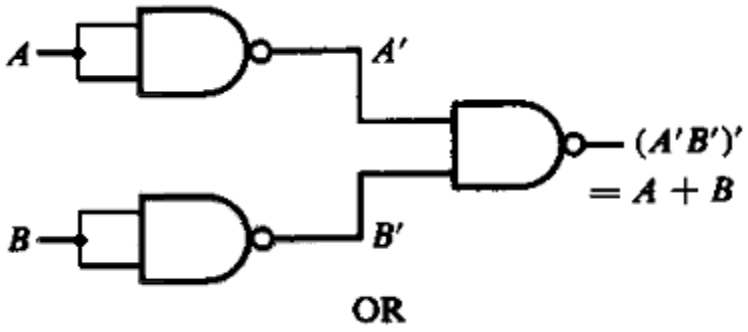
8. EX-OR gate produces an output as 1at its inputs is odd, otherwise output is 0.It has two inputs and one output.

Circuit diagram:

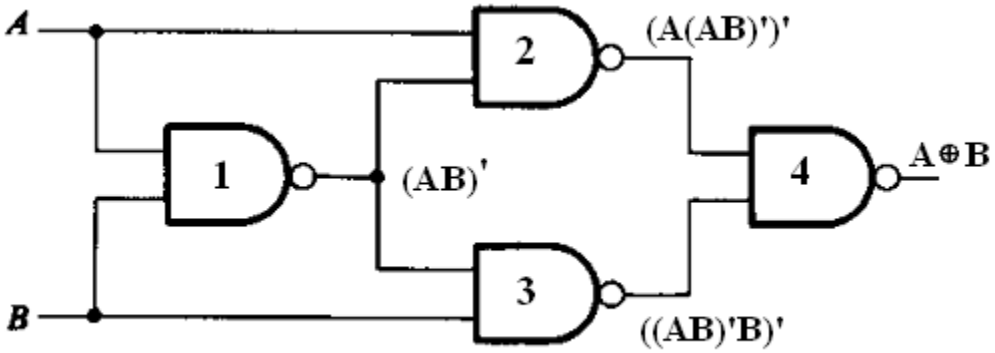


AND

NOT (inverter)



OR



X-OR

Theory:

1. NAND gate is usually a combination of two logic gates. AND gate followed by NOT gate.

2. It's output is complement of the output of an AND gate.

3. can construct any gates using NAND and NOR gates.

4. so these gates are called as universal gates.

5. Demorgan's Theorem: (AB)'=A'+B'

(A+B)'=A'.B'

Procedure:

1. Switch ON the Computer, which is installed with ORCAD Pspice 9.2
2. After logging into the computer, go to the Start Menu and go to: Start Menu->All Programs->ORCAD_Pspice9.2->Capture
3. Once Capture is up, start a new project going to File->New->Project...

The project dialogue box should appears. From the dialog box

-Select "Analog or Mixed A/D" for your project type.

-Give Name to the Project: AND gate

-Change the LOCATION of the saved project to required folder.

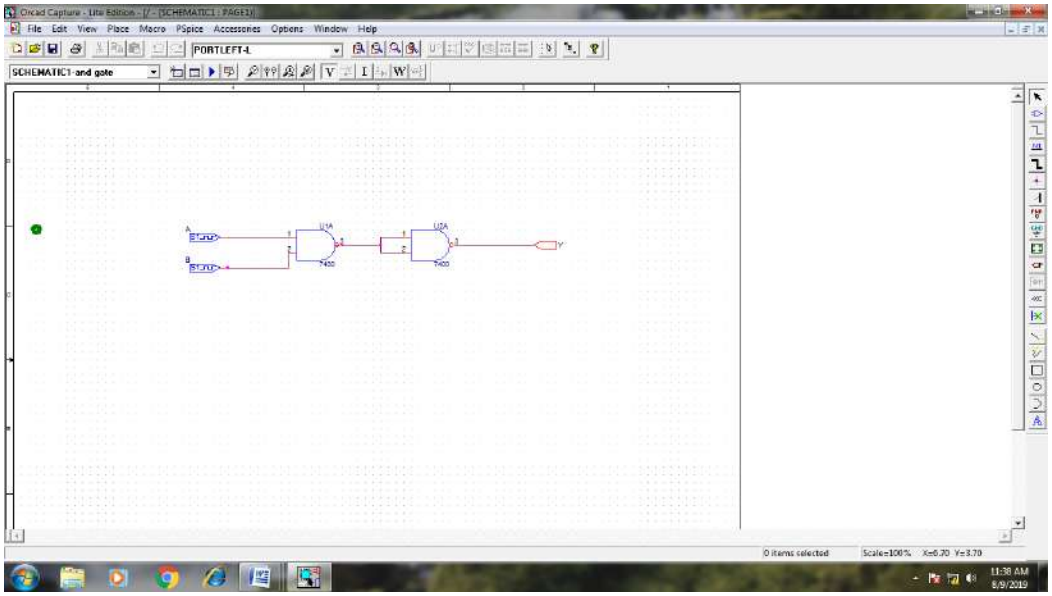
4. After selecting "OK" to the above dialog box the box below comes up. Make sure you select "Create a blank project" before clicking OK.
5. You should be seeing a blank grid. On the right hand side of the grid, there are a lot of buttons. To place a certain part, select the button shaped like this: 
6. After selecting the "Add Library…" button, Add the following libraries:

   sourcstm.olb

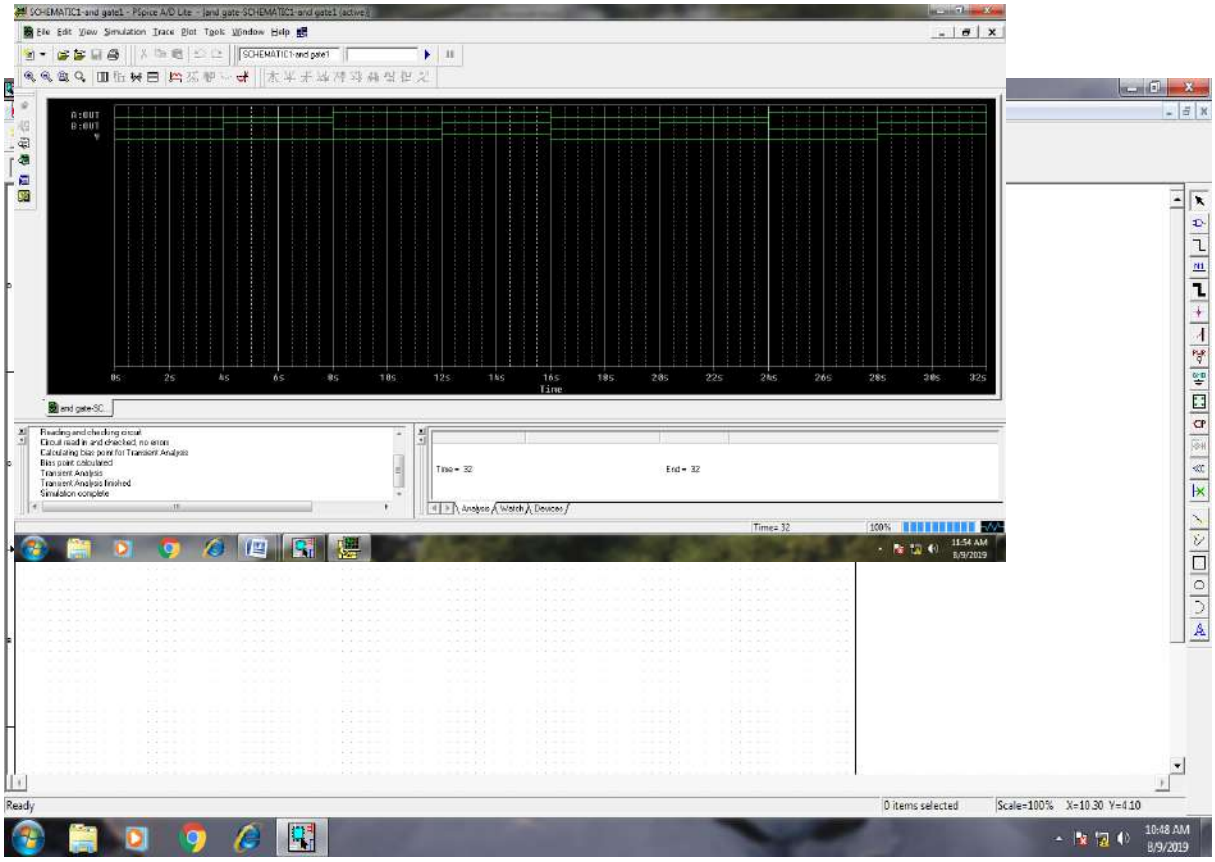
   eval.olb

7. Select the Eval library. This will have all of the logic gates you need. Select the "7400" part
8. After selecting "OK" in the above dialog box, you return to the schematic grid. When you left click your mouse, you now place the NAND part twice. To return to a normal cursor right-click the mouse and select "End mode".
9. Just as you added the 7400 (NAND) part as shown in the circuit diagram for AND gate.
10. Now we must select and label one port for the output of NAND gate, Name it as Y. To add a port select the button on the right that looks like this  .
11. Select the port called "PORTLEFT-L" and place it and name them as Y.
12. To rename the port, double-click the name "PORTLEFT-L" to get a dialog box as shown below. Change the name to "Y".
13. To add inputs, select the "place part" button on the right hand side as you did when you added the NAND part. When you get the place part dialog box, make sure the SOURCESTM library is selected. Select the "DigStim1" part.
14. This part will serve as your input. Therefore, place two of them as shown below:
15. Rename the inputs to be A, B.
16. Now we want to make sure that our sources will cover all possible input values. Since there are two inputs, that means we have 2^2 = 4 input combinations. We can ensure that we cover all combinations of inputs. First select the part A go to Edit->PSpice Stimulus and apply time period as 4s and ON time as 2s.

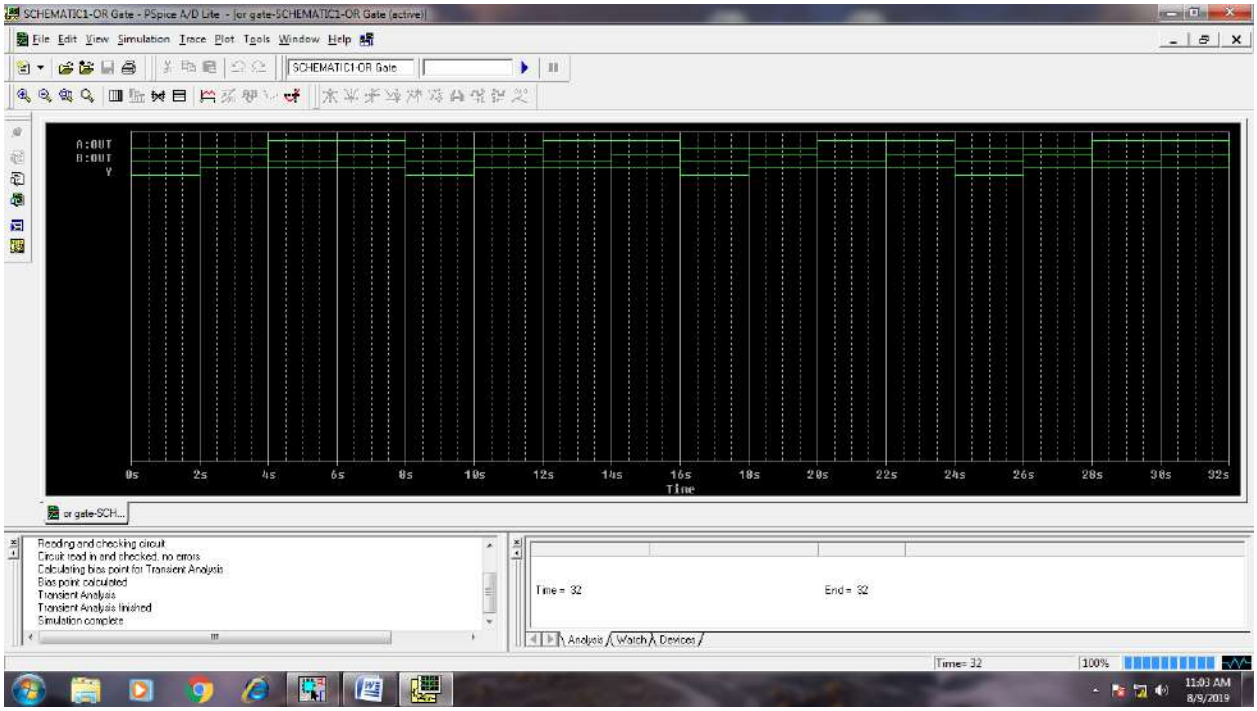
17. Repeat the above step for Part B, apply time period as 8s and ON time as 4s, apply time period as 16s and ON time as 8s.
18. Now wire the circuit as per the circuit diagram shown in the description



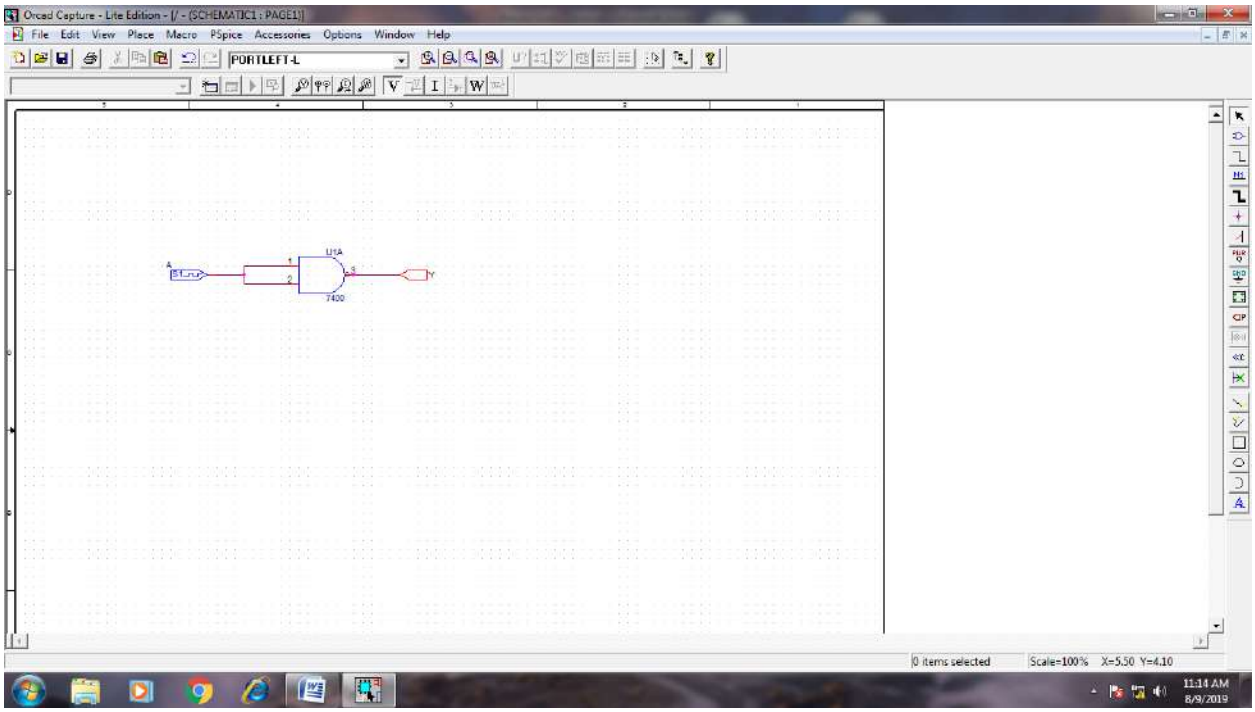
19. You are now ready to simulate the circuit. To do this select PSpice -> New Simulation Profile
20. Apply simulation run time as 16s and ADD traces of A, B, Y then the following output is obtained

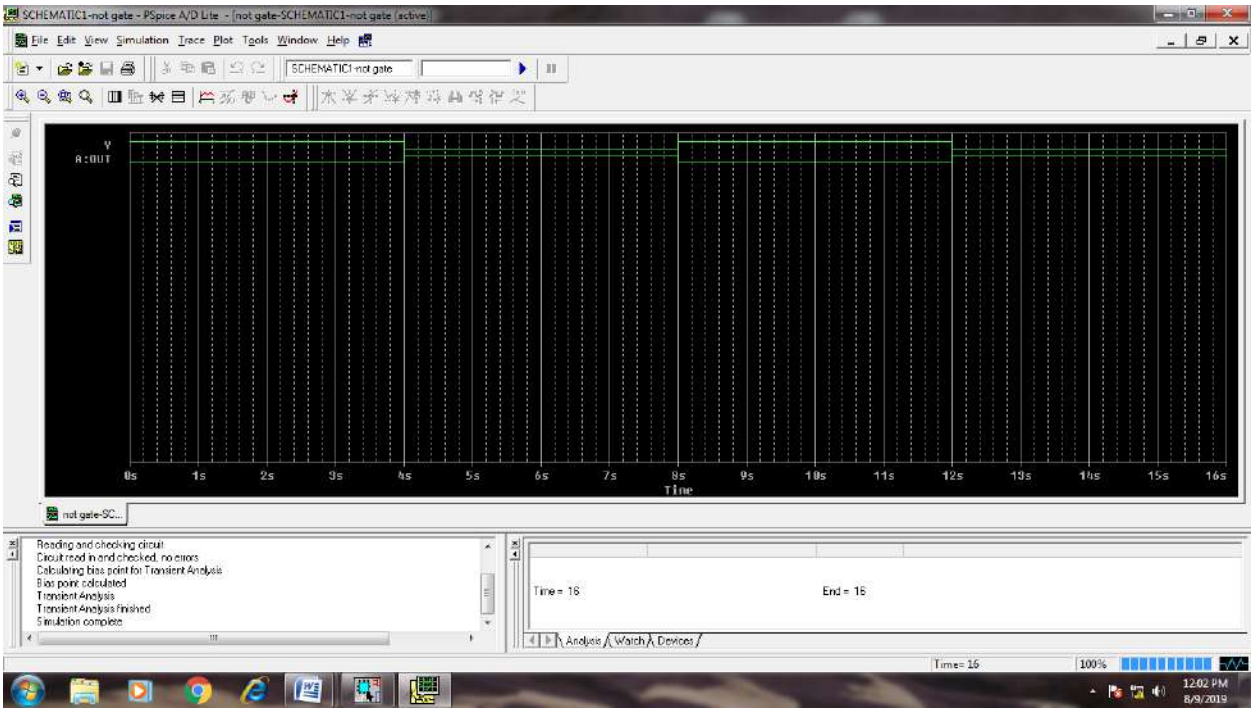


OR realization using NAND circuit

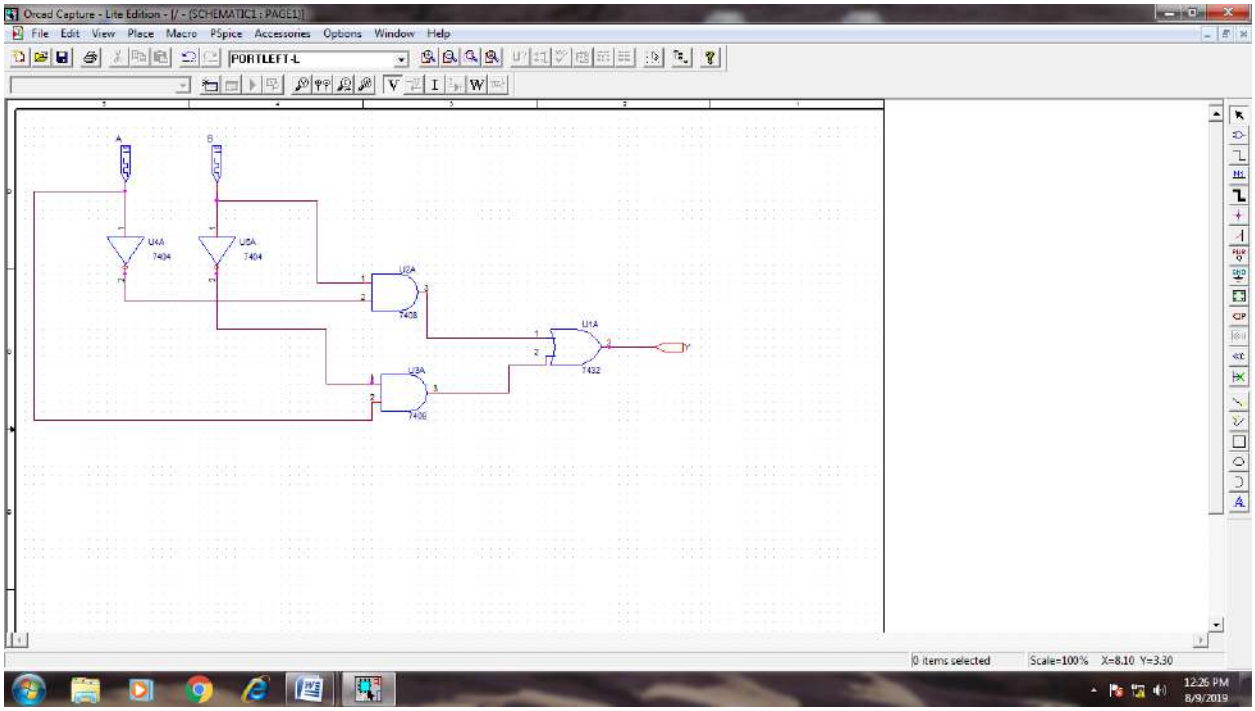


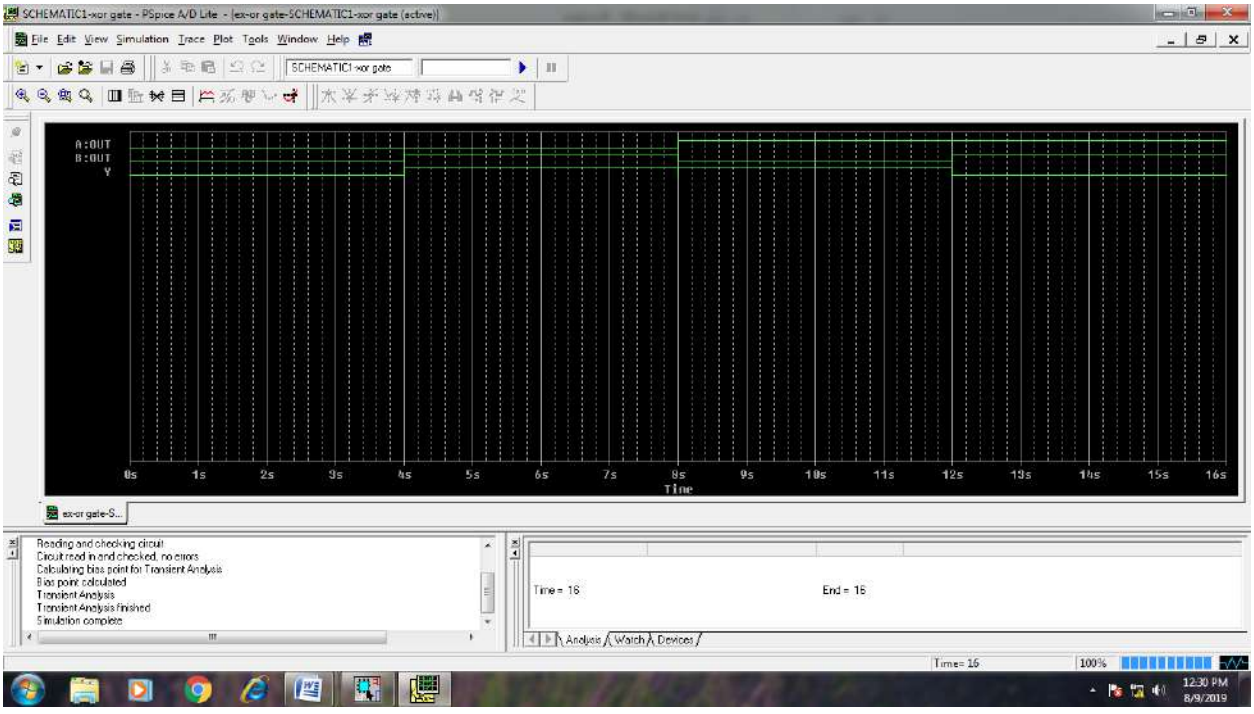
Realization of NOT gate using NAND circuit





Realization of EXOR using NAND gates





Result:

The output waveforms obtained in the Pspice simulation is exactly following the truth table of basic gates and EX-OR gate. Hence the logic gates and EX-OR circuit is simulated in Pspice and observed the circuit behavior.

SIMULATION OF AND, OR, NOT and EXOR USING NOR GATE

1. Description

The setup for this experiment requires the following Equipment

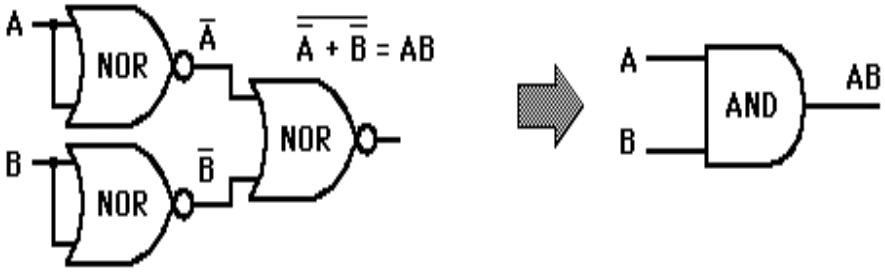
Name	Specifications	No	Purpose
PC with Windows OS		1	To insert IC
ORCAD Pspice 9.2 software package	DIP 14 PIN Quad 2-input IC	1	To realize basic gates

2. Circuit Diagram

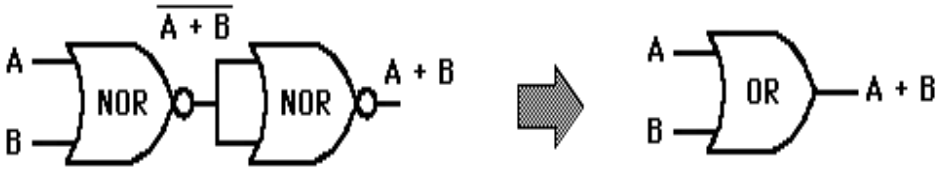
Realization of NOT, AND, OR using NOR Gates

NOT Gate

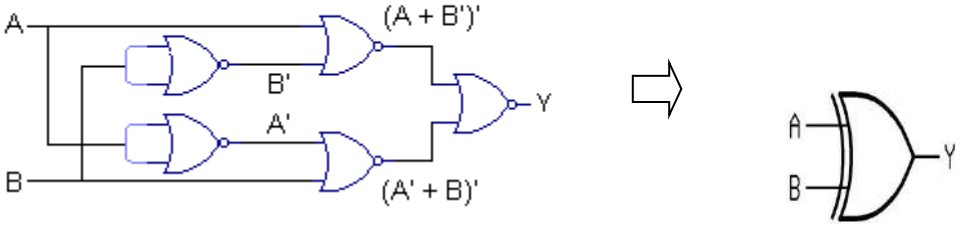
AND Gate



OR Gate



TWO INPUT XNOR GATE USING NOR GATE



3. Theory

NOR Gate is called Universal Gate because we can realize any basic gates using NOR Gate.

To realize NOT Gate using NOR Gate both the inputs has been shorted since NOT Gate has only one input. When binary high signal i.e.1 is given at the input, binary low i.e.0 is the output and vice-versa.

To realize OR Gate using NOR Gate, NOR Gate is connected to NOT Gate.

To realize AND Gate using NOR Gate, the inputs are complemented using 2 NOR gates and their outputs are given as inputs to the other NOR gate.

4. Procedure

1. Switch ON the Computer, which is installed with ORCAD Pspice 9.2
2. After logging into the computer, go to the Start Menu and go to: Start Menu->All Programs->ORCAD_Pspice9.2->Capture
3. Once Capture is up, starts a new project going to File->New->Project...

The project dialogue box should appears from the dialog box

-Select "Analog or Mixed A/D" for your project type.

-Give Name to the Project: Basic gates using NOR

-Change the LOCATION of the saved project to required folder.

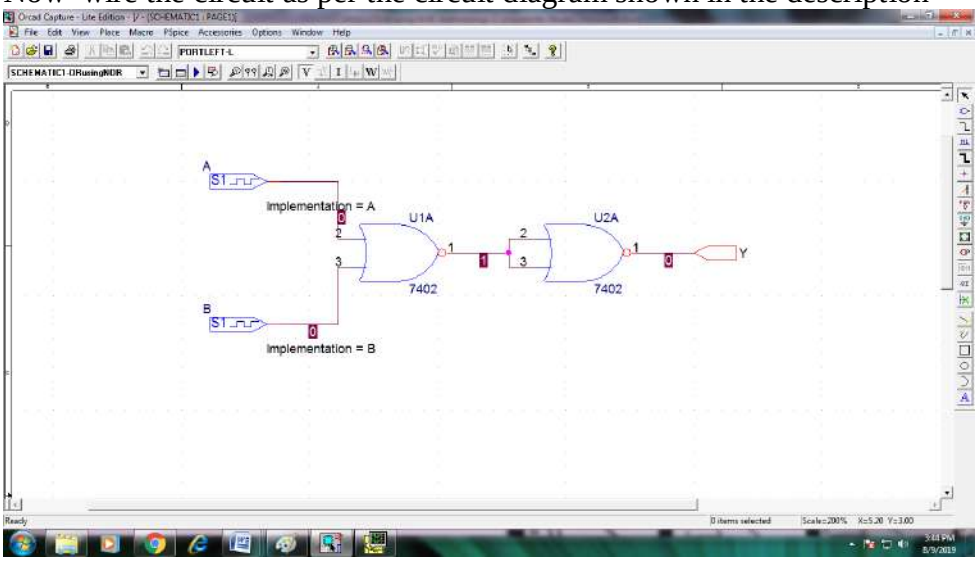
4. After selecting "OK" to the above dialog box make sure you select "Create a blank project" before clicking OK.
5. You should be seeing a blank grid. On the right hand side of the grid, there are a lot of buttons. To place a certain part, select the button shaped like this: 
6. After selecting the "Add Library…" button, Add the following libraries:

   sourcstm.olb

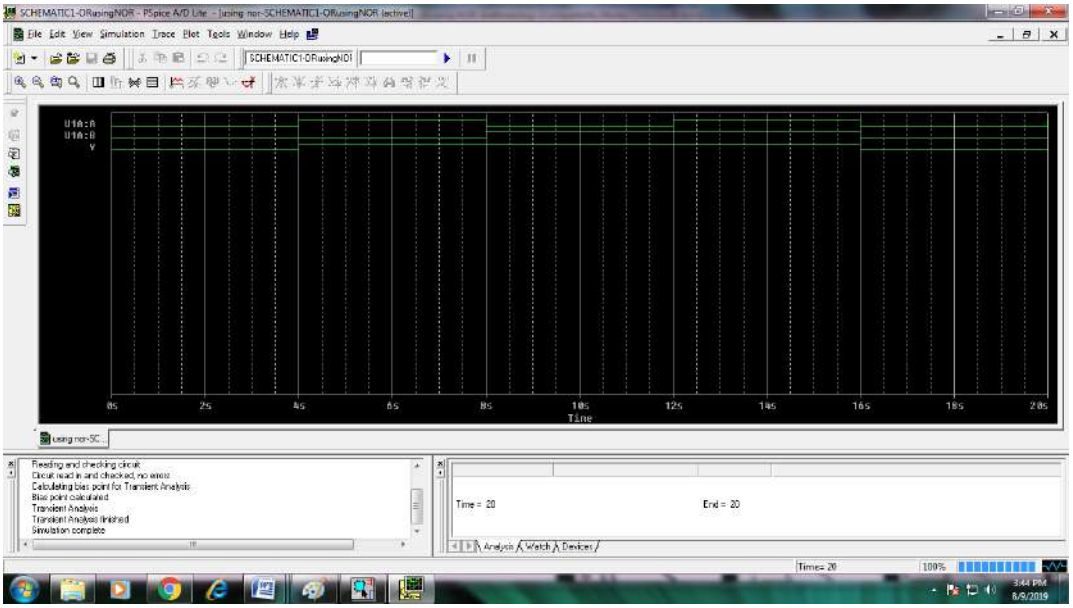
   eval.olb

7. Select the EVAL library. This will have all of the logic gates you need. Select the "7402" part for NOR gate
8. After selecting "OK" in the above dialog box, you return to the schematic grid. When you left click your mouse, you now place the NOR part for required number of times. For example to realize OR gate using NOR, place NOR gate twice. To return to a normal cursor right-click the mouse and select "End mode".
9. Now we must select and label output port for the output of OR gate Y. To add a port select the button on the right that looks like this  .
10. Select the port called "PORTLEFT-L" and place it and name as Y.
11. To rename the port, double-click the name "PORTLEFT-L" to get a dialog box as shown below. Change the name to "Y".

12. To add inputs, select the “place part” button on the right hand side as you did when you added the NOR part. When you get the place part dialog box, make sure the SOURCESTM library is selected. Select the “DigStim1” part.
13. This part will serve as your input. Therefore, place two of them
14. Rename the inputs to be A, B
15. Now we want to make sure that our sources will cover all possible input values. Since there are two inputs, that means we have 2^2= 4 input combinations. We can ensure that we cover all combinations of inputs. First select the part A go to Edit->PSpice Stimulus and apply time period as 4s and ON time as 2
16. Repeat the above step for Part B, apply time period as 8s and ON time as 4s, then finally select part C, apply time period as 16s and ON time as 8s.
17. Now wire the circuit as per the circuit diagram shown in the description



18. You are now ready to simulate the circuit. To do this select PSpice -> New Simulation Profile
19. Apply simulation run time as 16s and ADD traces of A,B,Y then the following output is obtained



20. Repeat the same steps to realize NOT, AND and EXOR gates as per the corresponding circuit diagrams

5. Truth Tables

OR GATE

INPUTS		OUTPUT
A	**B**	**Y**
0	0	0
0	1	1
1	0	1
1	1	1

AND GATE

INPUTS		OUTPUT
A	**B**	**Y**
0	0	0
0	1	0
1	0	1
1	1	1

NOT GATE

INPUT	OUTPUT
A	**Y=A**
0	1
1	0

6. Result:

The output waveforms obtained in the Pspice simulation is exactly following the truth tables of NOT, AND, OR and EXOR gates using NOR gate. Hence the gates are simulated in Pspice and observed the circuit behavior.

SIMULATION OF HALF ADDER	Experimental methodology

SIMULATION OF HALF ADDER USING PSPICE

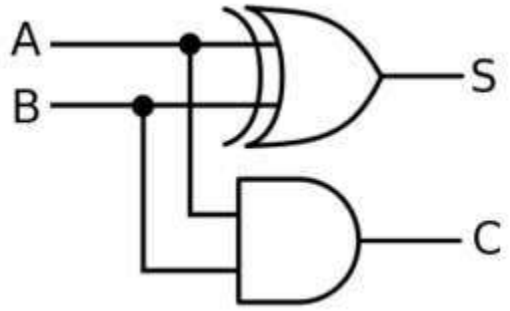
Description:

1. This experiment requires personal computer with Windows OS and ORCAD Pspice 9.2 software package.
2. ORCAD Pspice is Analog and Digital circuit simulation software.
3. Pspice contains both analog and digital circuit component library.
4. The required components for an analog/digital circuit can be picked from the library.
5. The circuit can be built by wiring the selected components, analog or digital sources .
6. Circuit simulation can be done by applying required inputs. Then, the resulting outputs can be observed.
7. Half adder is a combinational circuit with two binary inputs (A & B) and two

binary outputs .

Circuit diagram:

Half adder :



Theory:

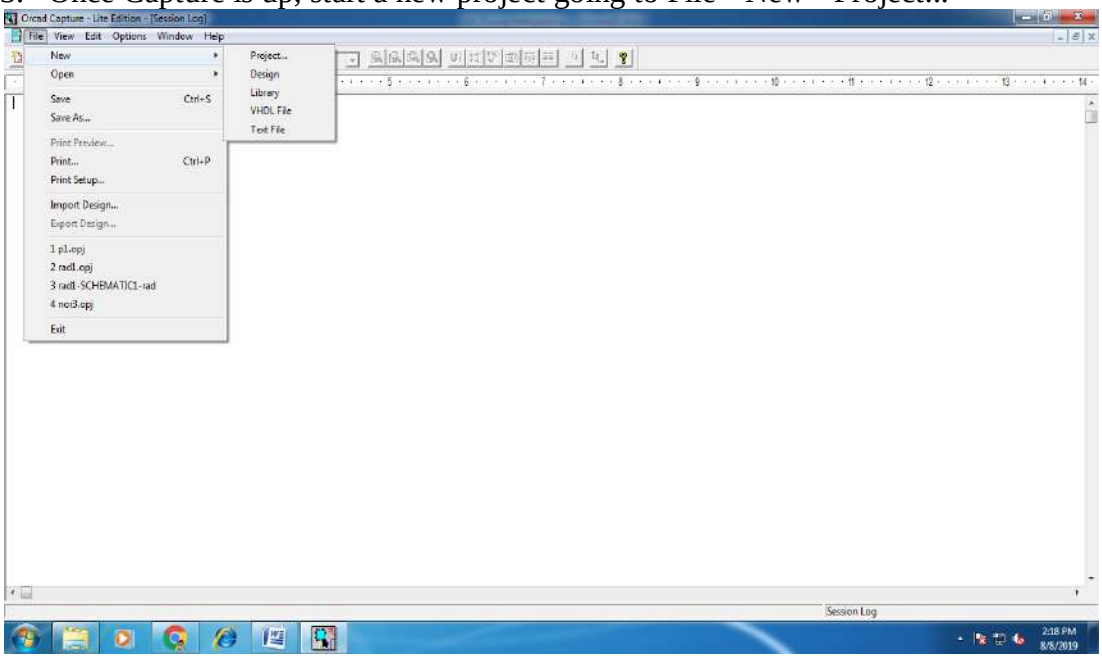
1. A half adder can add two bits at a time.
2. It's outputs are SUM and CARRY.
3. For two bit addition- SUM will be 1, if only one input is 1(EX-OR operation).
4. CARRY will be one, when both inputs are 1 (AND operation).
5. So, by using one AND gate and one X-OR gate, a half adder circuit can be constructed.

SUM = AB' + A'B

CARRY = AB

Procedure:

1. Switch ON the Computer, which is installed with ORCAD Pspice 9.2
2. After logging into the computer, go to the Start Menu and go to: Start Menu->All Programs->ORCAD_Pspice9.2->Capture
3. Once Capture is up, start a new project going to File->New->Project...

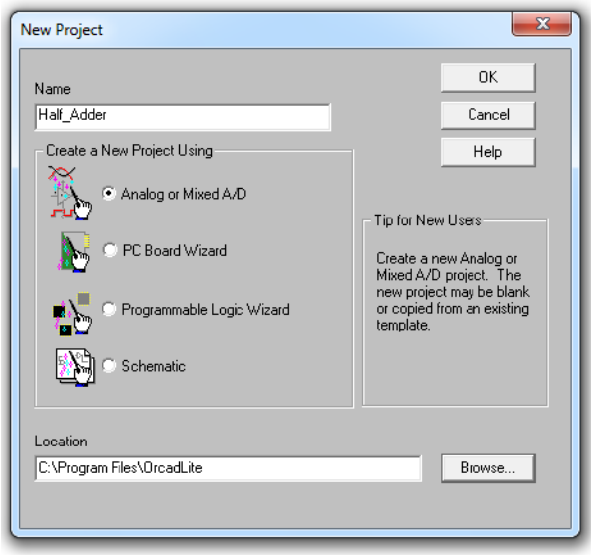


The project dialogue box should appear as below.

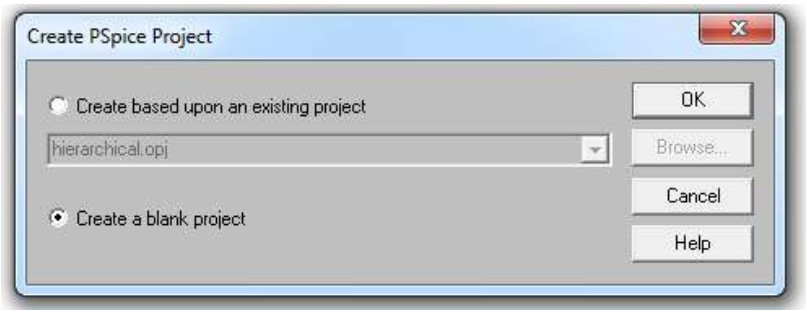
-Select “Analog or Mixed A/D” for your project type.

-Give Name to the Project: Half_Adder

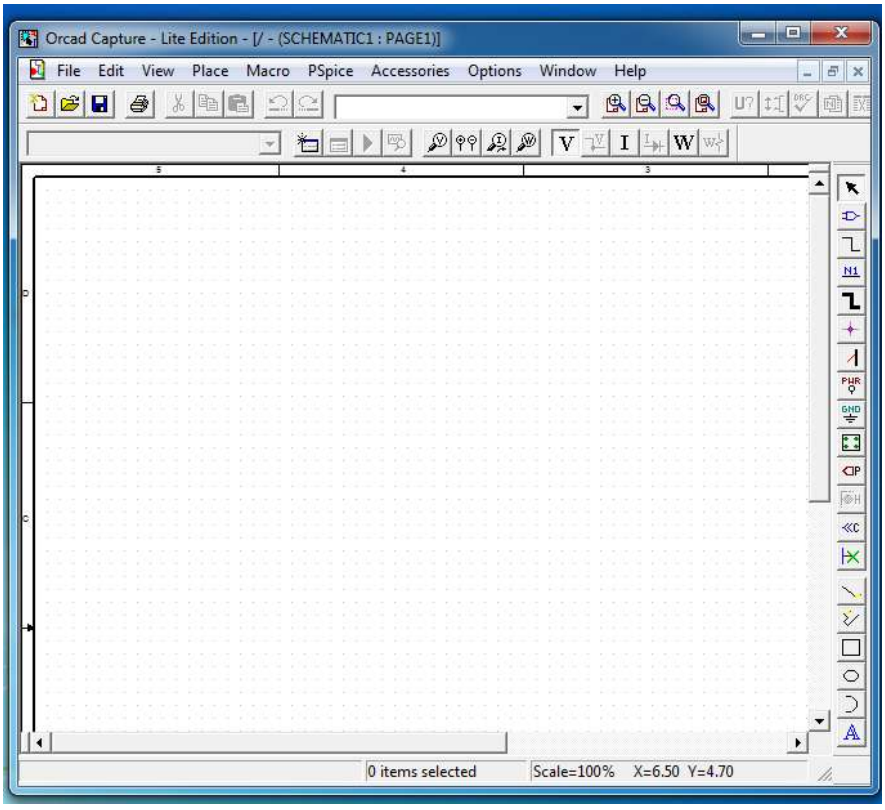
-Change the LOCATION of the saved project to required folder.



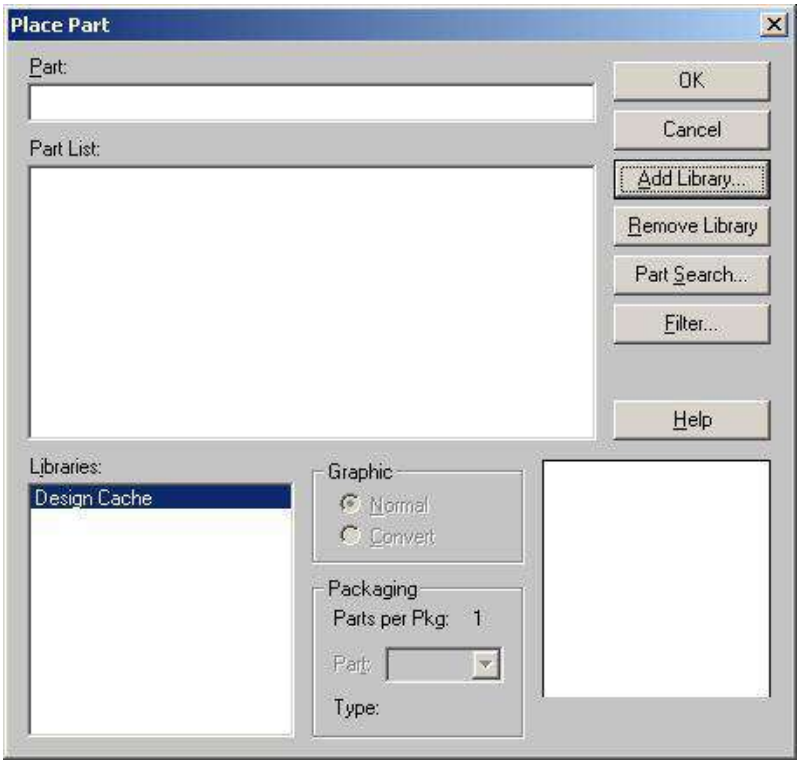
4. After selecting “OK” to the above dialog box the box below comes up. Make sure you select “Create a blank project” before clicking OK.



5. You should be seeing a blank grid. On the right hand side of the grid, there are a lot of buttons. To place a certain part, select the button shaped like this: 



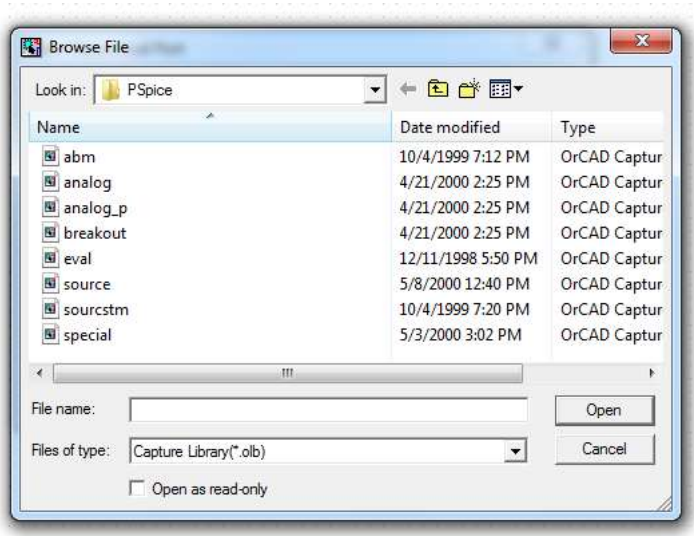
6. When you select the “place tool” button as above, you should get the following dialogue box as shown below. Select the “Add Library…” button.



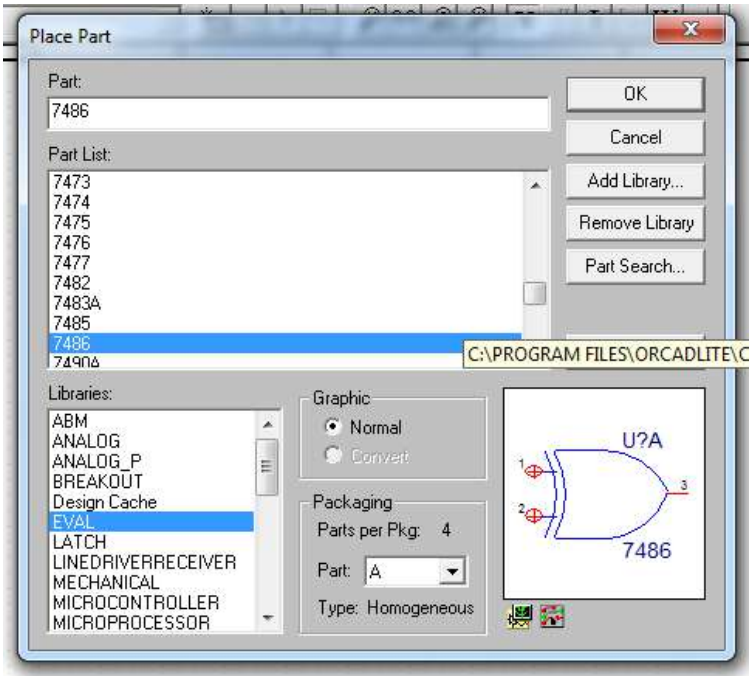
7. After selecting the "Add Library…" button, you should get a selection list that looks like the one below. Add the following libraries:

   sourcstm.olb

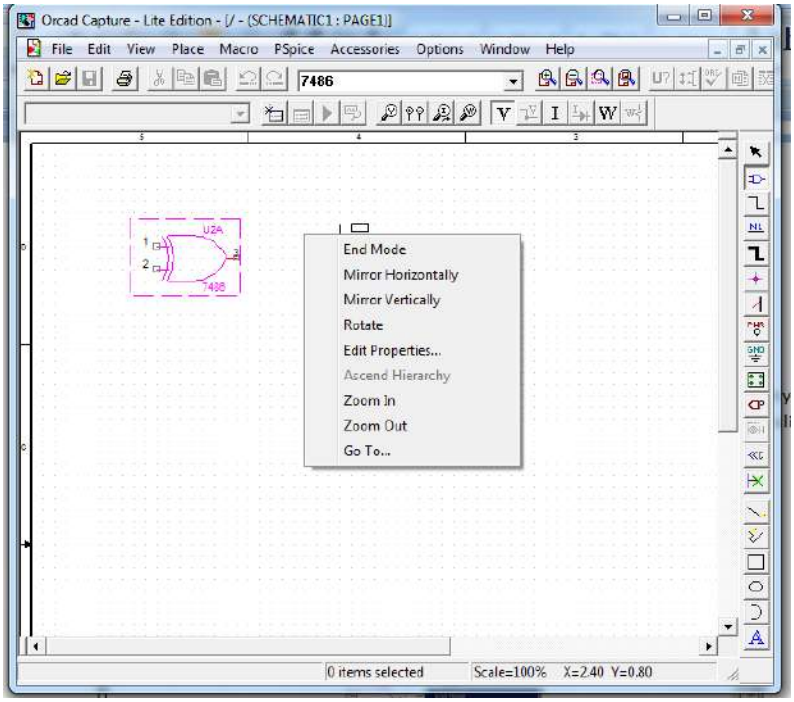
   eval.olb



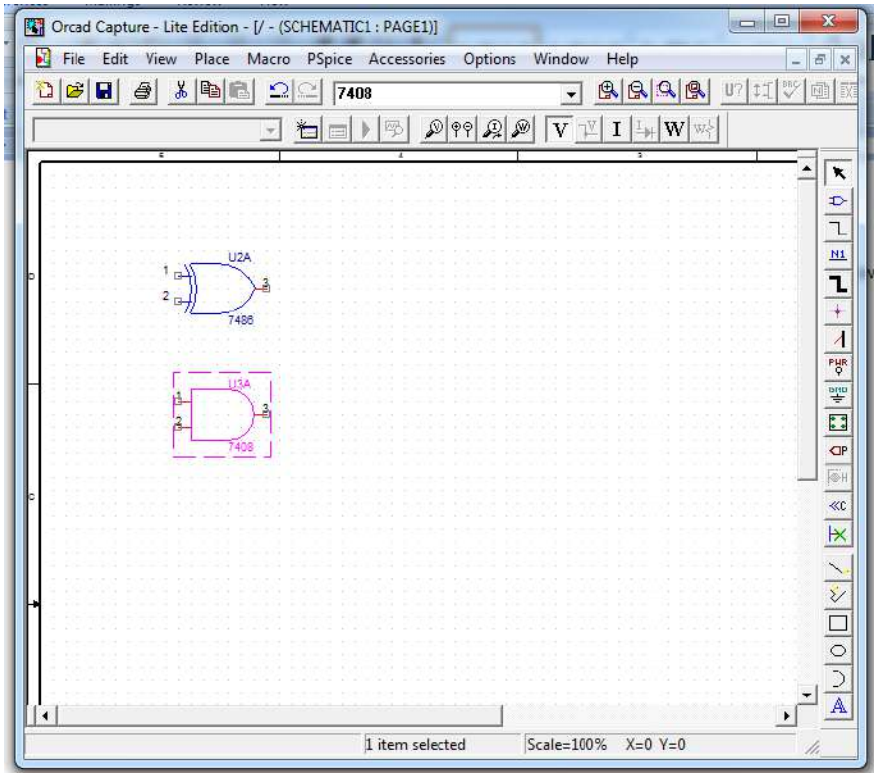
8. Select the Eval library. This will have all of the logic gates you need. Select the "7486" part as shown below



9. After selecting "OK" in the above dialog box, you return to the schematic grid. When you left click your mouse, you now place the XOR part. To return to a normal cursor right-click the mouse and select "End mode".

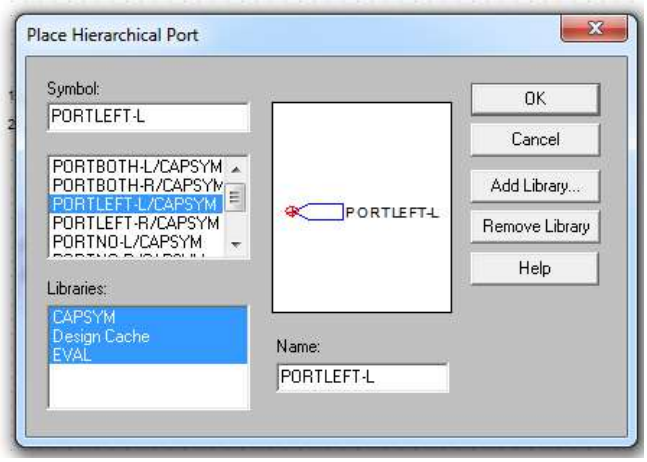


10. Just as you added the 7486 (XOR) part, add an 7408 (AND) part and place as shown below.

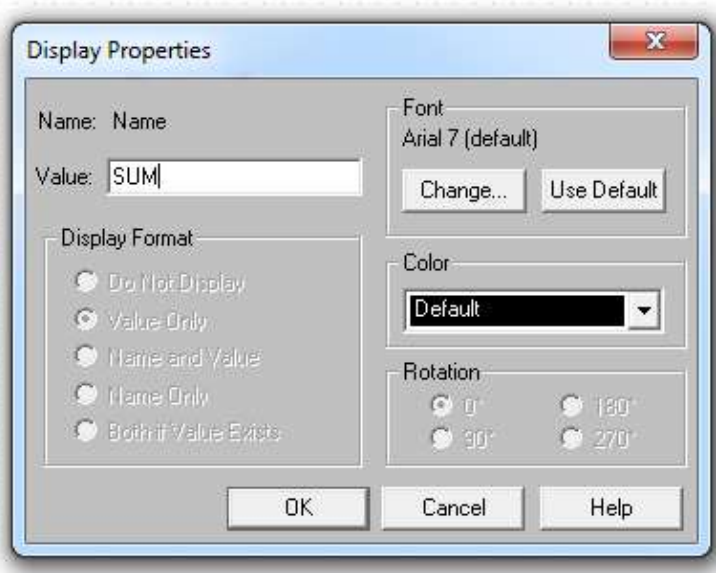


11. Now we must select and label two ports for the outputs of half adder, SUM and CARRY. To add a port select the button on the right that looks like this  .

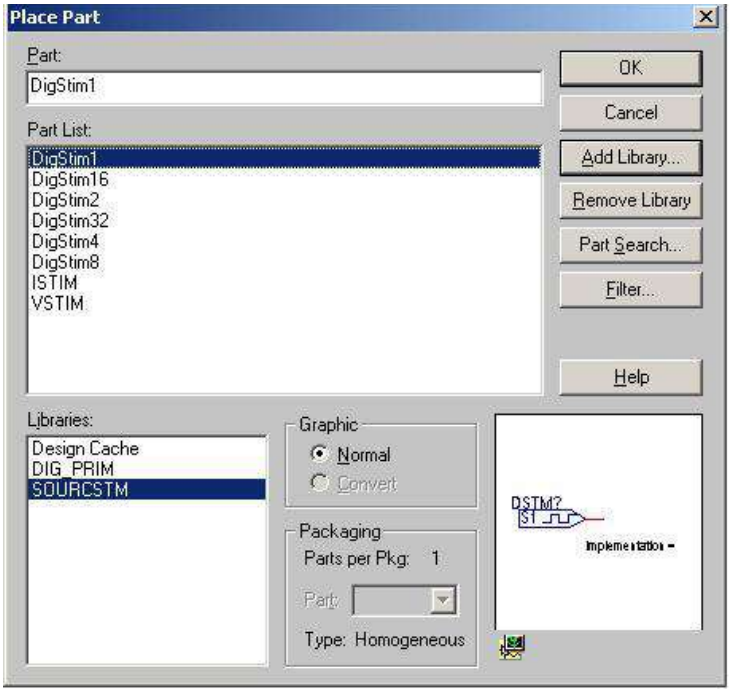
12. Select the port called “PORTLEFT-L” and place as shown below:



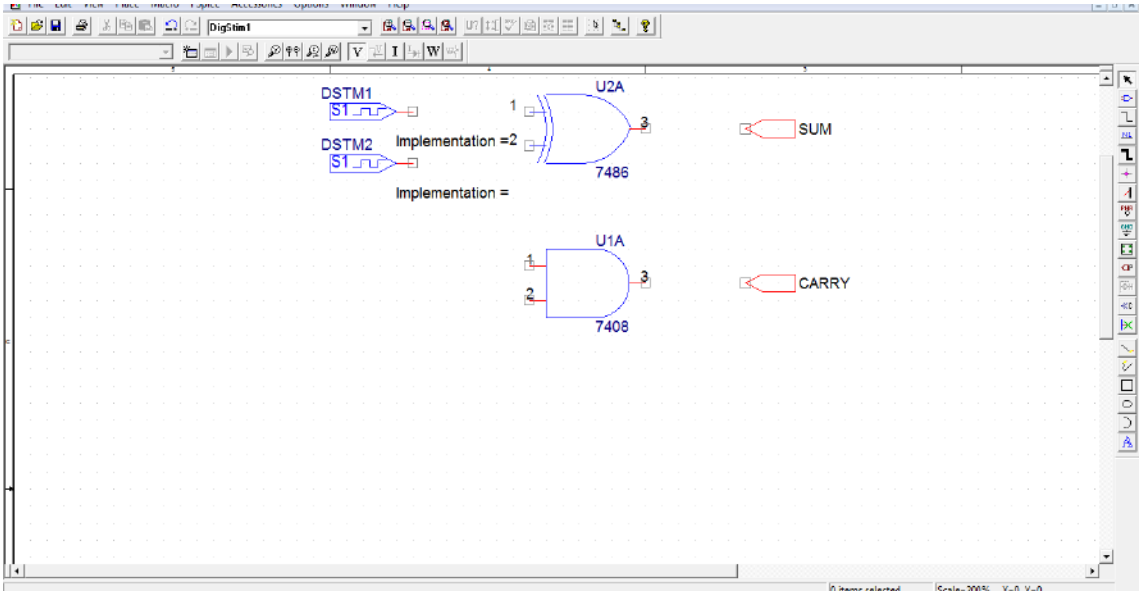
13. To rename the port, double-click the name “PORTLEFT-L” to get a dialog box as shown below. Change the name to “SUM”.



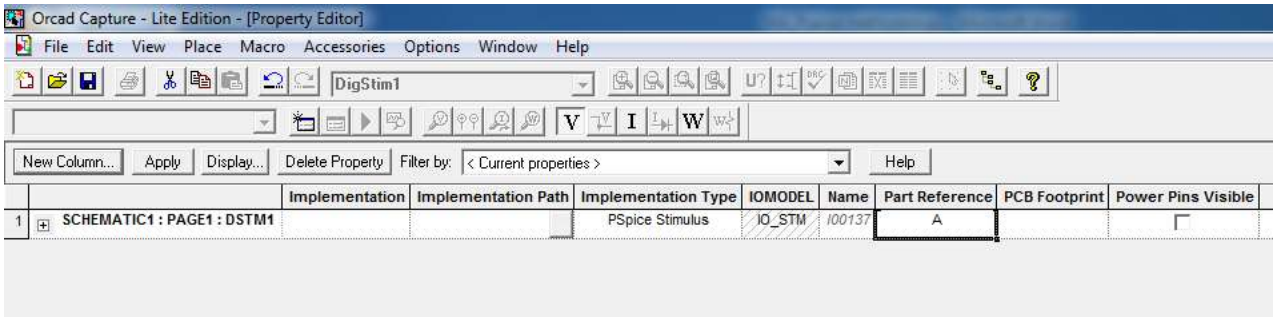
14. To rename the port, double-click the name “PORTLEFT-L” to get a dialog box as shown below. Change the name to “SUM”.
15. Repeat steps 10 to 13 to add a port for CARRY
16. To add inputs, select the “place part” button on the right hand side as you did when you added the XOR and AND part. When you get the place part dialog box, make sure the SOURCESTM library is selected. Select the “DigStim1” part.



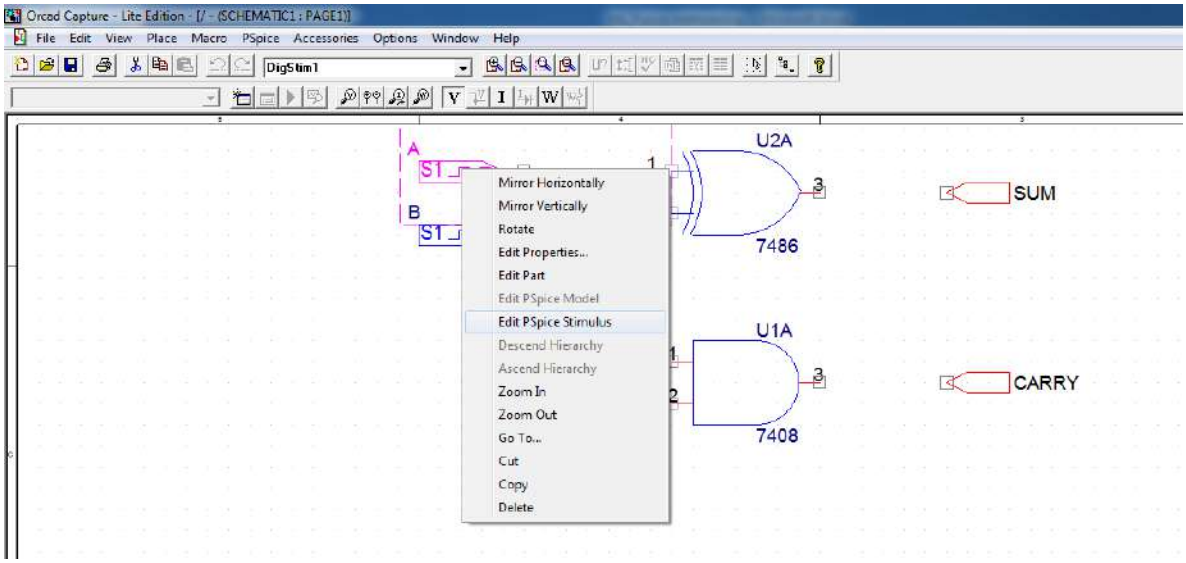
17. This part will serve as your input. Therefore, place four of them as shown below:



18. Rename the inputs to be A, B as you did in step 14

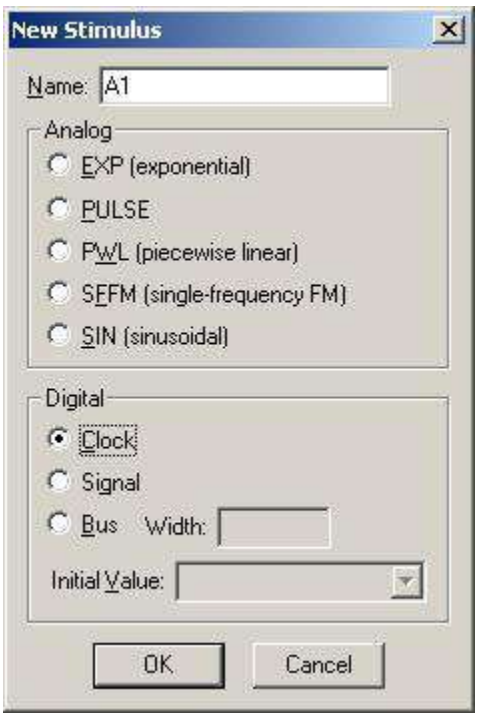


19. Now we want to make sure that our sources will cover all possible input values. Since there are two inputs, that means we have 2^2 = 4 input combinations. We can ensure that we cover all combinations of inputs as follows. First select the part A as shown below



20. While the part is still selected go to Edit->PSpice Stimulus

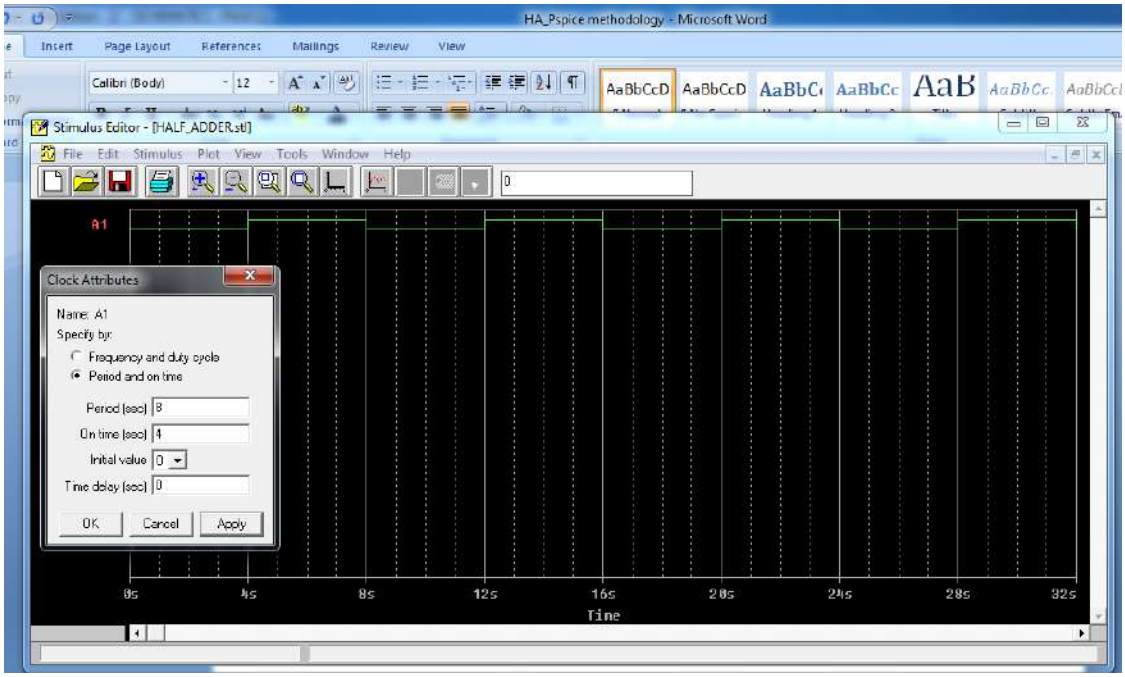
You should get a box as seen below. Make sure you name the stimulus whatever the part is named (in this case A). Make the input a “Clock” and click “OK”.



21. Upon clicking OK, you get a dialog box as shown below. Select “Specify by Period and on time”. For this input, you should make the period 2^4 = 16 s and the on time half of the period (8 s) as shown below. Click “OK”.

Close out of the “Stimulus Editor”.

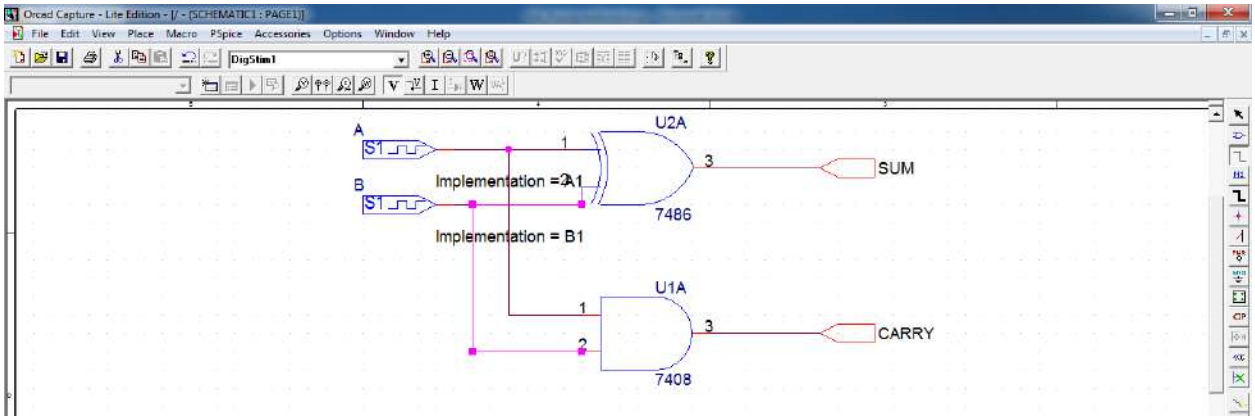
Save the changes and click “Yes” when asked if you want to update the schematic



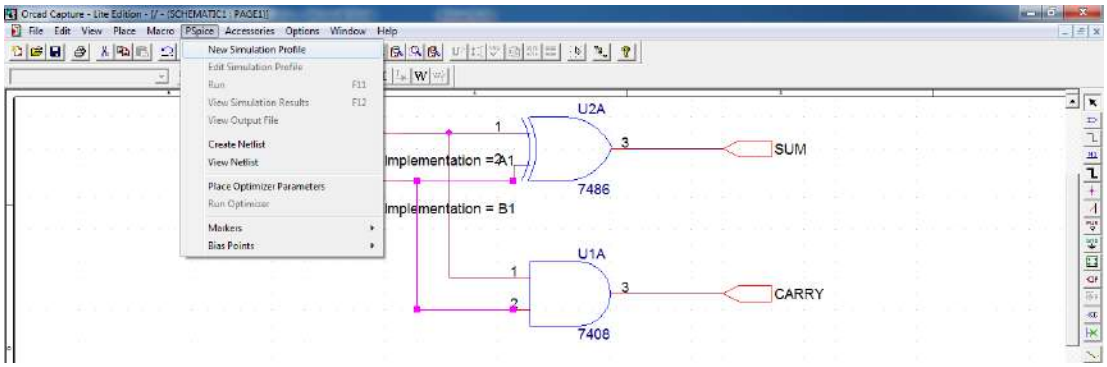
22. Similarly Configure the input B with period :16 and ON time: 8

23. Now we need to wire the circuit together. To do this select the “wire” button on the right hand side that looks like this: 

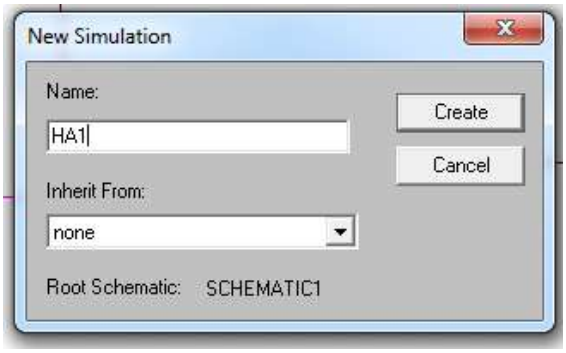
24. When you left click, your mouse lays down wire. Notice that when you connect two parts, both ends of the wire are a bright red dot. Wire the circuit as shown below. Right Click and select “End Wire” to return your mouse to a normal cursor.



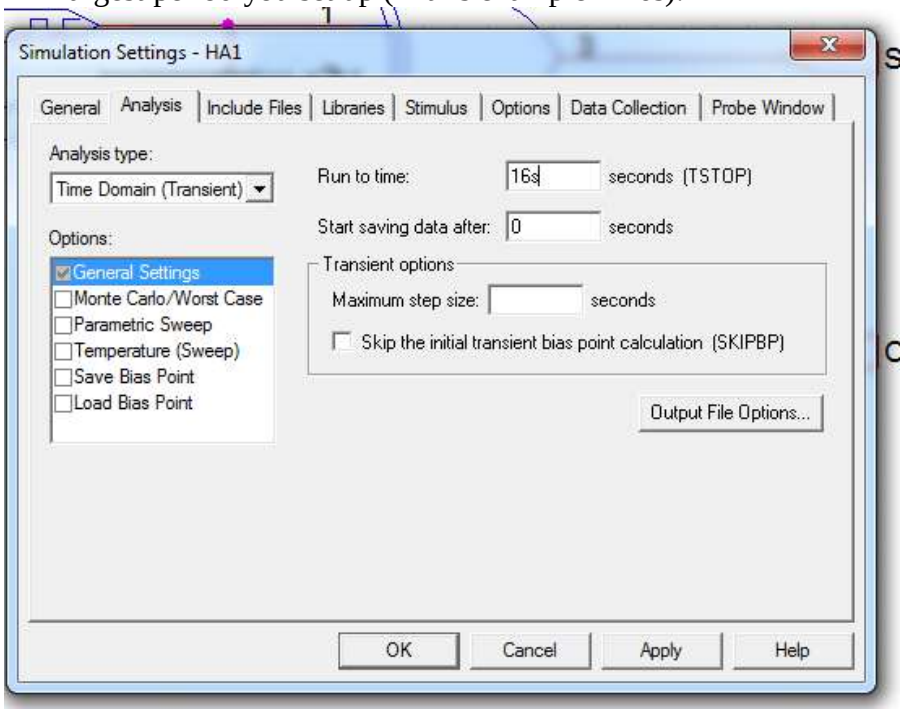
25. You are now ready to simulate the circuit. To do this select PSpice -> New Simulation Profile



26. You will get a dialog box as seen below. Give your simulation profile a name, inherit from "None" and click "Create"

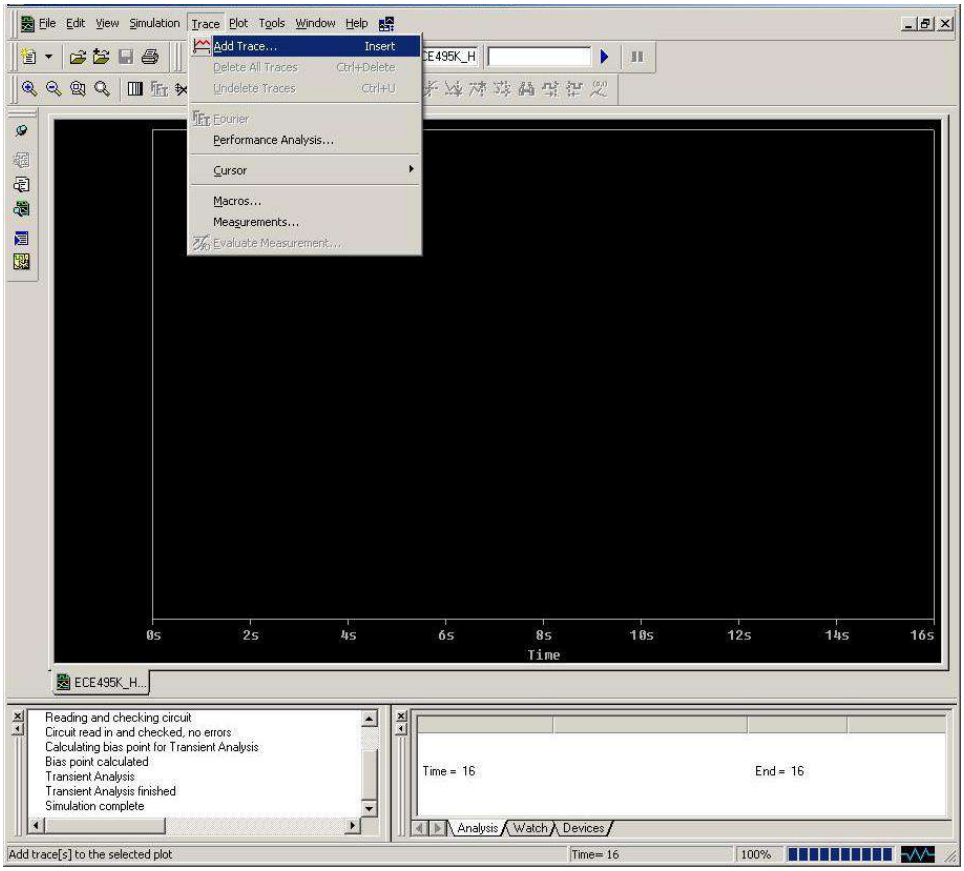


27. You should then get a dialog box as seen below. If you have set up your inputs correctly above, the only thing you need to do is change the "Run to time:" of the simulation to the largest period you set up (in this example – 16s).

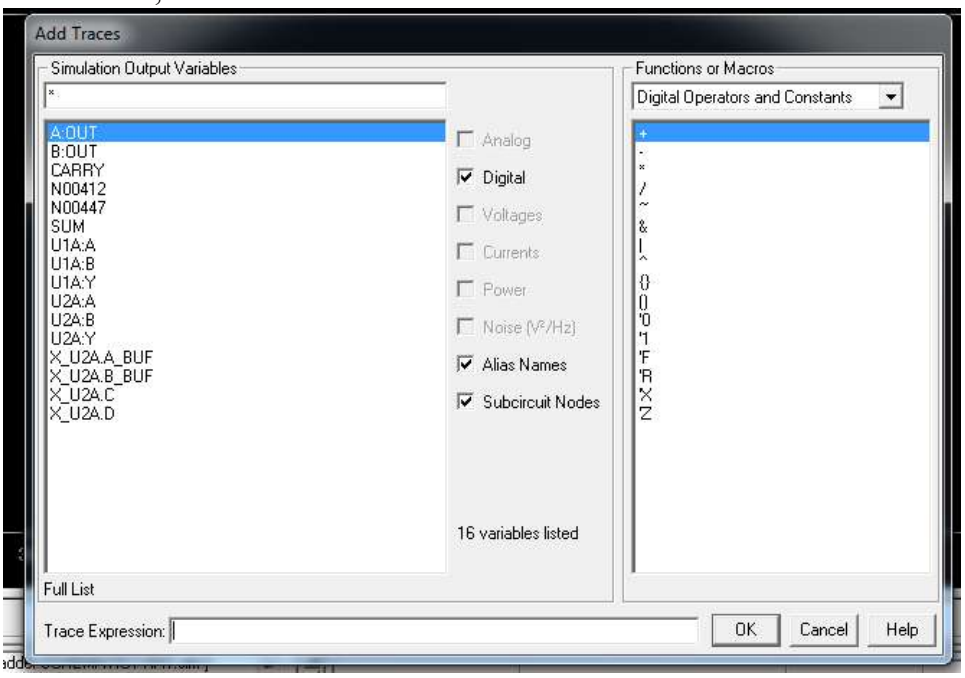


28. Click OK on the above dialog box. You should now be ready to run your simulation. Do so by clicking the  button.

29. After the simulation has completed you should get an empty black box as shown below. We want to look at our inputs compared to our output. To do so, we select "Trace->Add Trace…"

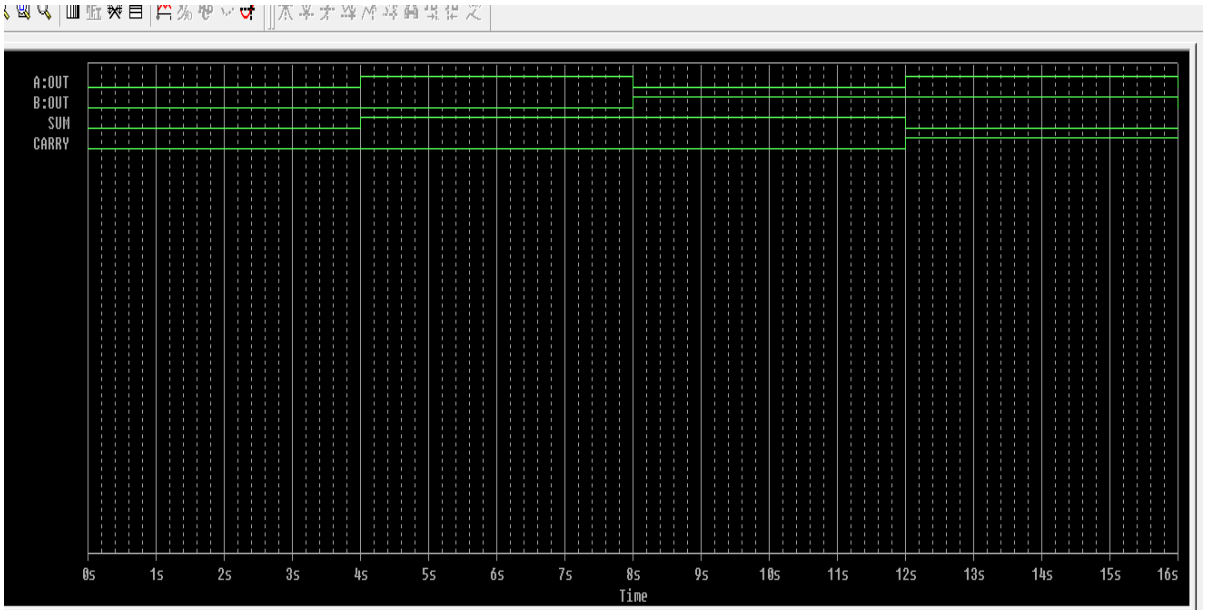


30. The "Add Trace…" dialog box is seen below. We can only add one trace at a time. For now, select "A:OUT" and click "OK".



31. Repeat steps 28 and 29 in the following order: B:OUT SUM ,CARRY

After doing so, your graph should look like below. If it does, you have completed the Half adder exercise successfully. Now observe the results and tally with the truth table



Truth tables:

Half adder:

Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Result:

The waveforms obtained in the Pspice simulation is exactly following the truth table of Half adder. Hence the half adder circuit is simulated in Pspice and observed the circuit behavior.

SIMULATION OF FULL ADDER	Experimental methodology

SIMULATION OF FULL ADDER USING PSPICE

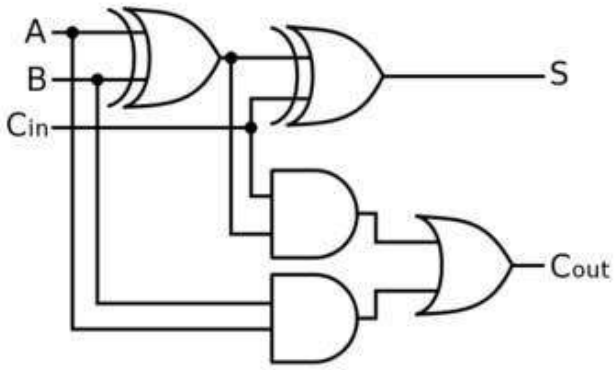
Description:

1. This experiment requires personal computer with Windows OS and ORCAD Pspice 9.2 software package.
2. ORCAD Pspice is an Analog/Digital circuit simulation software
3. Pspice contains both analog and digital circuit component library
4. The required components for an analog/digital circuit can be picked from the library
5. The circuit can be built by wiring the selected components, analog or digital sources
6. Circuit simulation can be done by applying required inputs. Then, the resulting outputs can be observed
7. Full adder is a combinational circuit with three binary inputs (A, B &C) and two

binary outputs .

Circuit diagram:

Full adder :



Truth table of Full adder :

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Theory:

1. A full adder can add three bits at a time.
2. A full adder is a combinational circuit that forms the arithmetic sum of input; it consists of three inputs and two outputs.
3. A full adder is useful to add three bits at a time but a half adder cannot do so.
4. In full adder sum output will be taken from X-OR Gate, carry output will be taken from OR Gate.

Procedure:

1. Switch ON the Computer, which is installed with ORCAD Pspice 9.2
2. After logging into the computer, go to the Start Menu and go to: Start Menu->All Programs->ORCAD_Pspice9.2->Capture
3. Once Capture is up, start a new project going to File->New->Project...

The project dialogue box should appears. From the dialog box

-Select "Analog or Mixed A/D" for your project type.

-Give Name to the Project: Full_Adder

-Change the LOCATION of the saved project to required folder.

4. After selecting "OK" to the above dialog box the box below comes up. Make sure you select "Create a blank project" before clicking OK.
5. You should be seeing a blank grid. On the right hand side of the grid, there are a lot of buttons. To place a certain part, select the button shaped like this: 
6. After selecting the "Add Library…" button, Add the following libraries:

   sourcstm.olb

   eval.olb

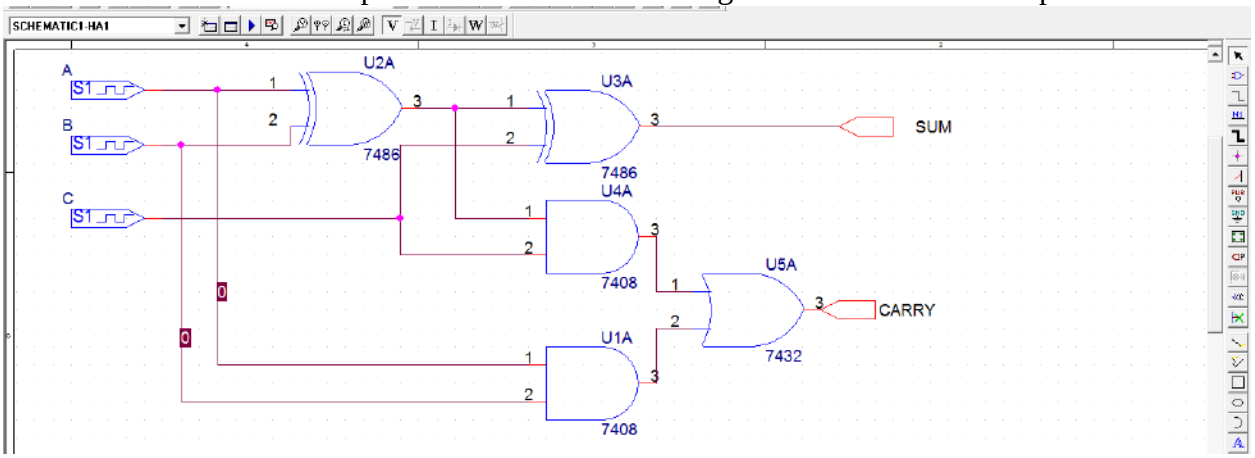
7. Select the Eval library. This will have all of the logic gates you need. Select the "7486" part
8. After selecting "OK" in the above dialog box, you return to the schematic grid. When you left click your mouse, you now place the XOR part twice. To return to a normal cursor right-click the mouse and select "End mode".
9. Just as you added the 7486 (XOR) part, add two 7408 (AND) parts and one OR gate part.
10. Now we must select and label two ports for the outputs of half adder, SUM and CARRY. To add a port select the button on the right that looks like this  .

11. Select the port called “PORTLEFT-L” and place twice and name them as SUM and CARRY repectively.
12. To rename the port, double-click the name “PORTLEFT-L” to get a dialog box as shown below. Change the name to “SUM”.
13. To add inputs, select the “place part” button on the right hand side as you did when you added the XOR and AND part. When you get the place part dialog box, make sure the SOURCESTM library is selected. Select the “DigStim1” part.
14. This part will serve as your input. Therefore, place three of them as shown below:

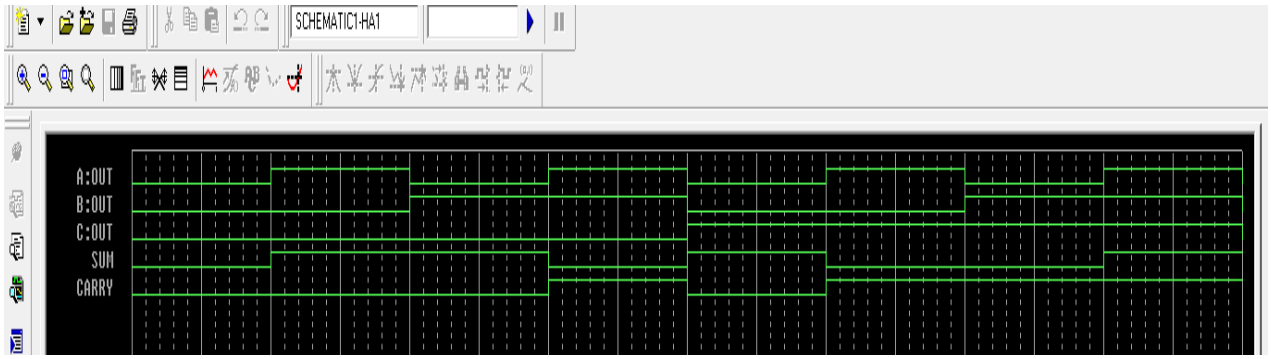
15. Rename the inputs to be A, B and C

16. Now we want to make sure that our sources will cover all possible input values. Since there are two inputs, that means we have 2^3 = 8 input combinations. We can ensure that we cover all combinations of inputs as follows. First select the part A go to Edit->PSpice Stimulus and apply time period as 4s and ON time as 2,

17. Repeat the above step for Part B, apply time period as 8s and ON time as 4s, then finally select part C, apply time period as 16s and ON time as 8s.
18. Now wire the circuit as per the full adder circuit diagram shown in the description



19. You are now ready to simulate the circuit. To do this select PSpice -> New Simulation Profile
20. Apply simulation run time as 16s and ADD traces of A.B,C,SUM,CARRY, then the following output is obtained



Result:

The output waveforms obtained in the Pspice simulation is exactly following the truth table of Full adder. Hence the Full adder circuit is simulated in Pspice and observed the circuit behavior.

SIMULATION OF MULTIPLEXER USING PSPICE

Description:

1. This experiment requires personal computer with Windows OS and ORCAD Pspice 9.2 software package.

2. ORCAD Pspice is Analod and Digital circuit simulation software

3. Pspice contains both analog and digital circuit component library

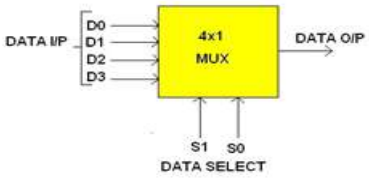
4. The required components for an analog/digital circuit can be picked from the library

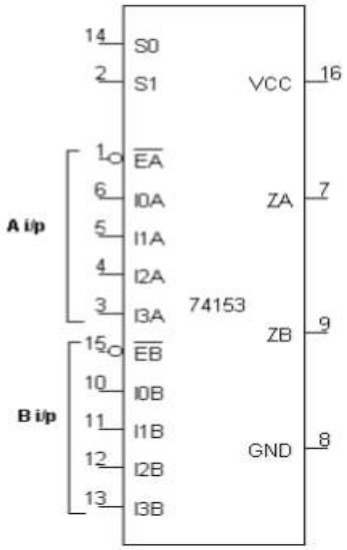
5. The circuit can be built by wiring the selected components, analog or digital sources

6. Circuit simulation can be done by applying required inputs. Then, the resulting outputs can be observed

7. Digital Multiplexer is a combinational circuit with 2^n inputs (data lines), n Selection lines and one output.

Circuit diagram:



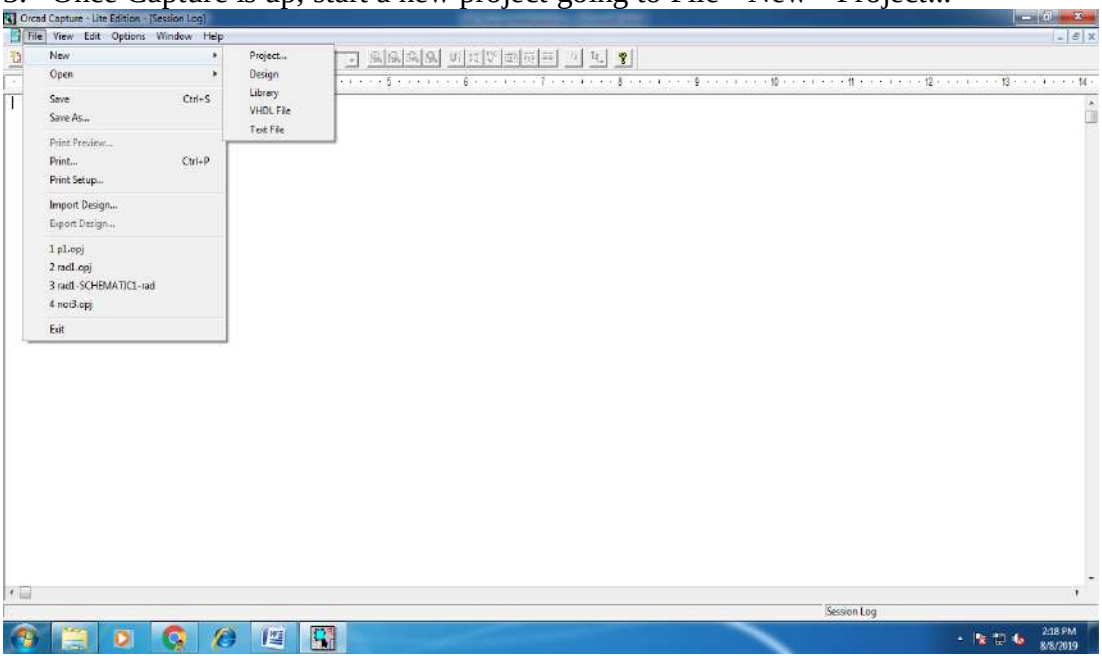


Theory:

1. The multiplexer, shortened to "**MUX**" or "MPX", is a combinational logic circuit designed to switch one of several input lines through to a single common output line by the application of a control signal.
2. Multiplexers are also known as data selectors because they can "select" each input data line.
3. The selection of each input line in a multiplexer is controlled by an additional set of inputs called **Select line**s.
4. A multiplexer has an even number of 2^n **data input** lines where n is number of "select" inputs

Procedure:

1. Switch ON the Computer, which is installed with ORCAD Pspice 9.2
2. After logging into the computer, go to the Start Menu and go to: Start Menu->All Programs->ORCAD_Pspice9.2->Capture
3. Once Capture is up, start a new project going to File->New->Project...

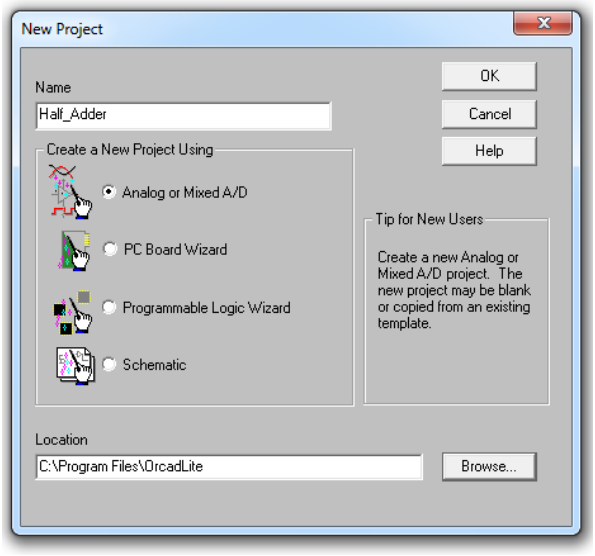


The project dialogue box should appear as below.

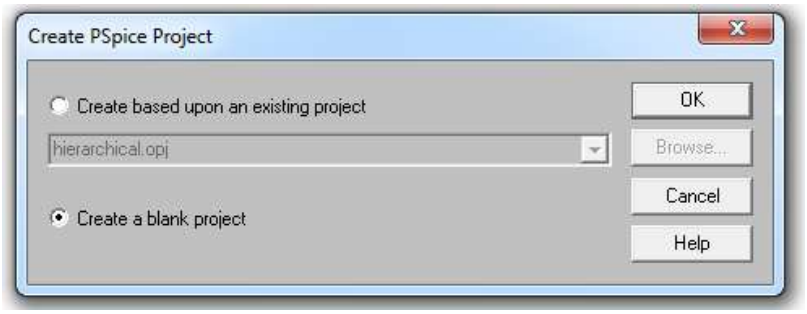
-Select "Analog or Mixed A/D" for your project type.

-Give Name to the Project: Multiplexer

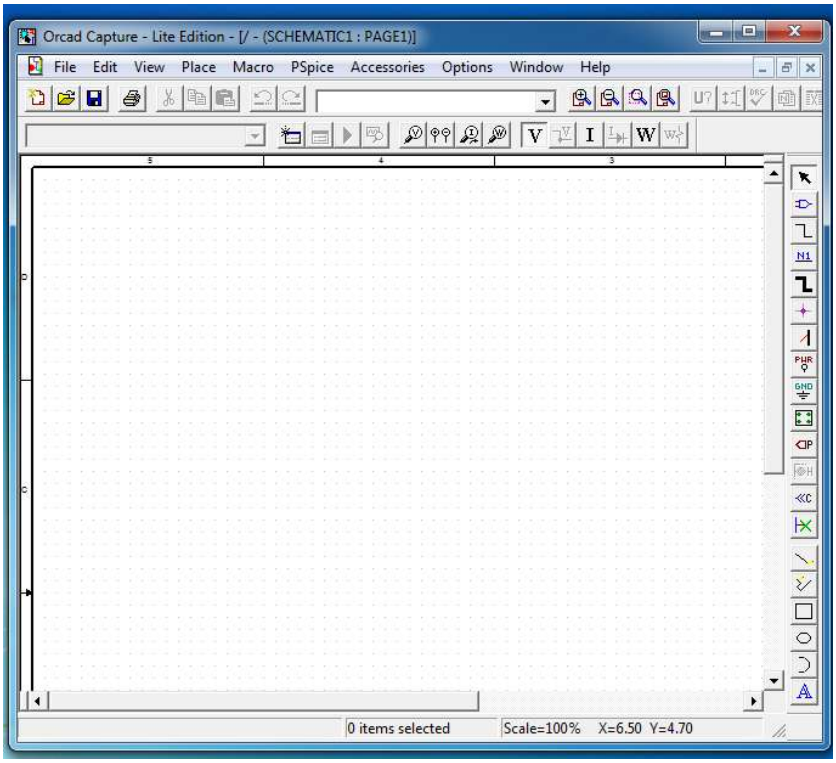
-Change the LOCATION of the saved project to required folder.



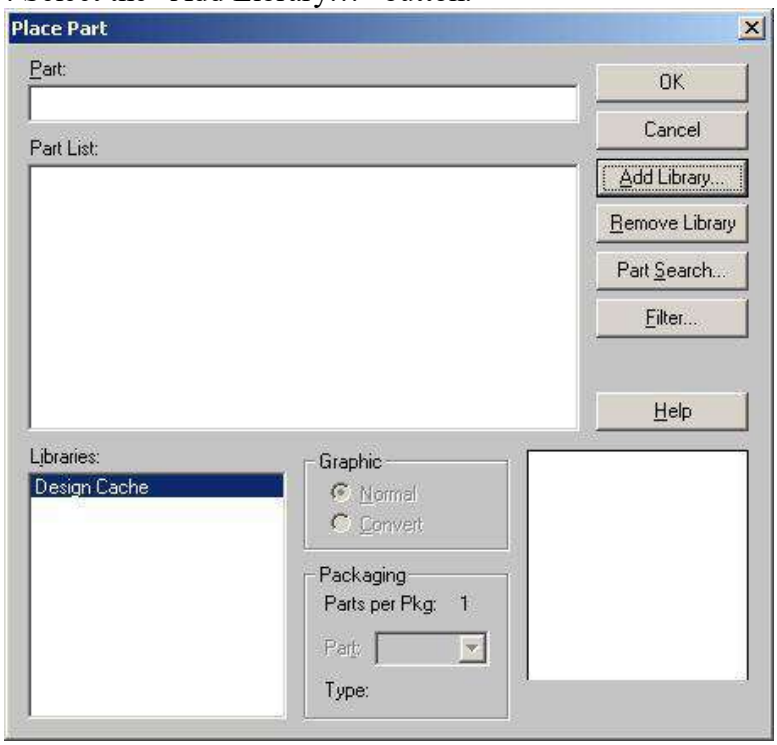
4. After selecting “OK” to the above dialog box the box below comes up. Make sure you select “Create a blank project” before clicking OK.



5. You should be seeing a blank grid. On the right hand side of the grid, there are a lot of buttons. To place a certain part, select the button shaped like this: 



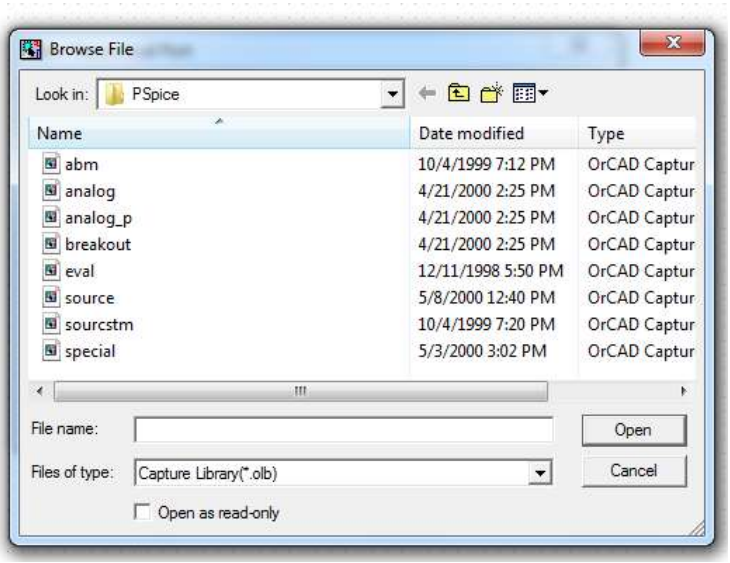
6. When you select the “place tool” button as above, you should get the following dialogue box as shown below. Select the “Add Library…” button.



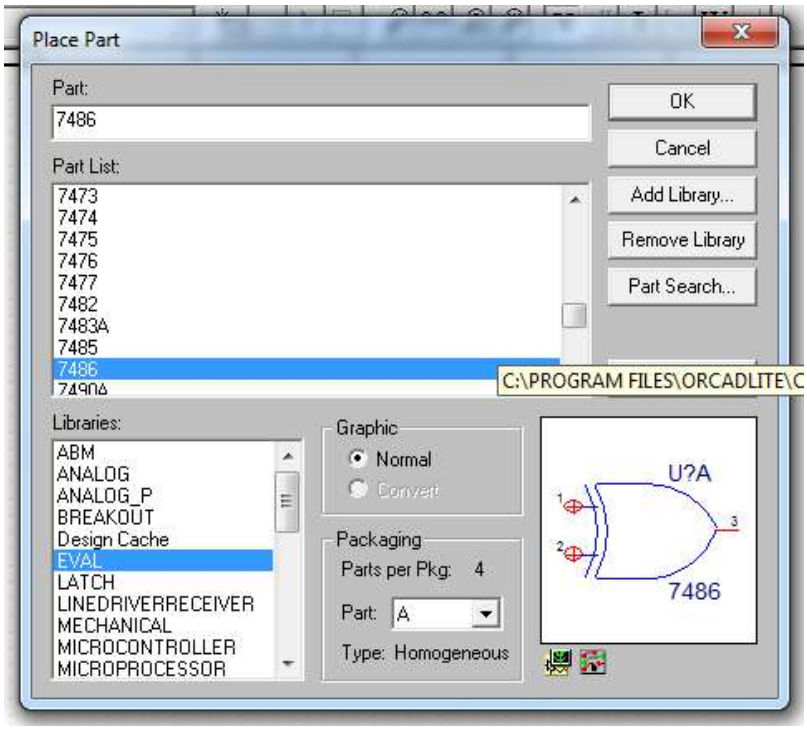
7. After selecting the “Add Library…” button, you should get a selection list that looks like the one below. Add the following libraries:

sourcstm.olb

eval.olb



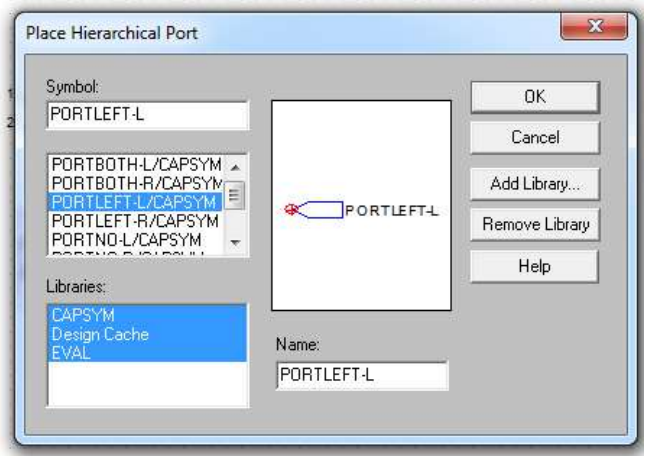
8. Select the Eval library. This will have all of the logic gates you need. Select the “74153” part



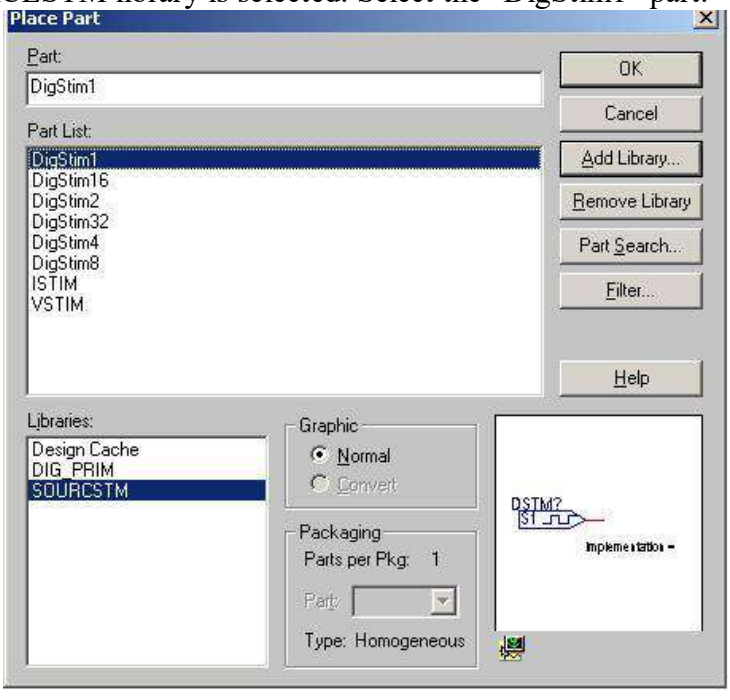
9. After selecting “OK” in the above dialog box, you return to the schematic grid. When you left click your mouse, you now place the IC74153 part. To return to a normal cursor right-click the mouse and select “End mode”.

10. Now we must select and label two ports for the outputs of Multiplexer, Z_A and Z_B. To add a port select the button on the right that looks like this  .

11. Select the port called “PORTLEFT-L” and place as shown below:

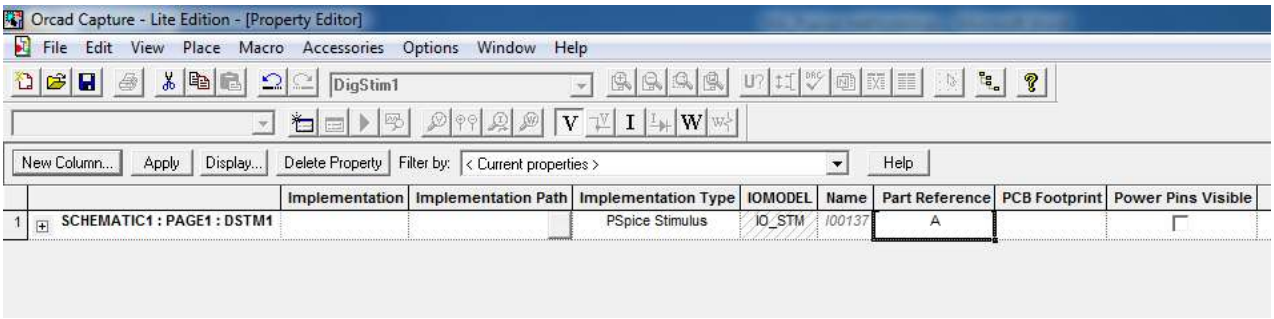


12. To rename the port, double-click the name “PORTLEFT-L” to get a dialog box as shown below. Change the name to “Z_A”.
13. Repeat steps 11 to 13 to add a port for Z_B
14. To add inputs, select the “place part” button on the right hand side as you did when you added the IC 74153 part. When you get the place part dialog box, make sure the SOURCESTM library is selected. Select the “DigStim1” part.



15. This part will serve as your input. Therefore, place 12 of them(Four A channel inputs , Four B Channel inputs, Enable input for A channel, enable input for B channel and Selection lines S_1 and S_0).

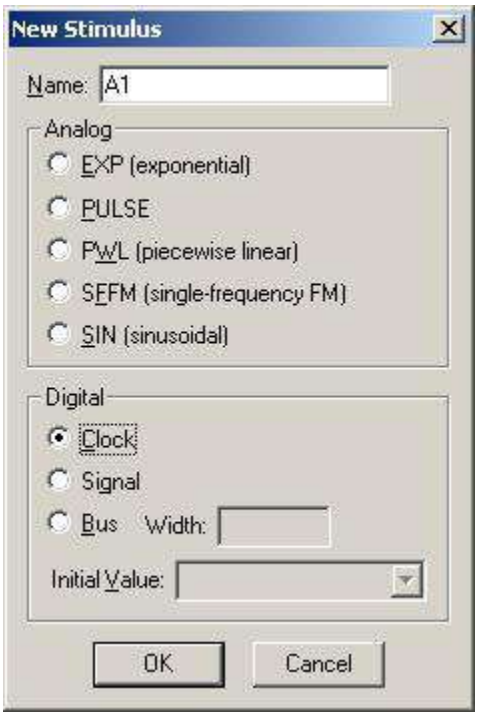
16. Rename the data lines to be I3A, I2A, I1A, I0A, And I3B, I2B, I1B, I0B and selection inputs as S1,S0 and enable inputs as EA and EB.



17. Now we want to make sure that our sources will cover all possible input values. Since there are two inputs(Selection lines), that means we have 2^2 = 4 combinations. We can ensure that we cover all combinations of inputs as follows. First select the part IA3

18. While the part is still selected go to Edit->PSpice Stimulus

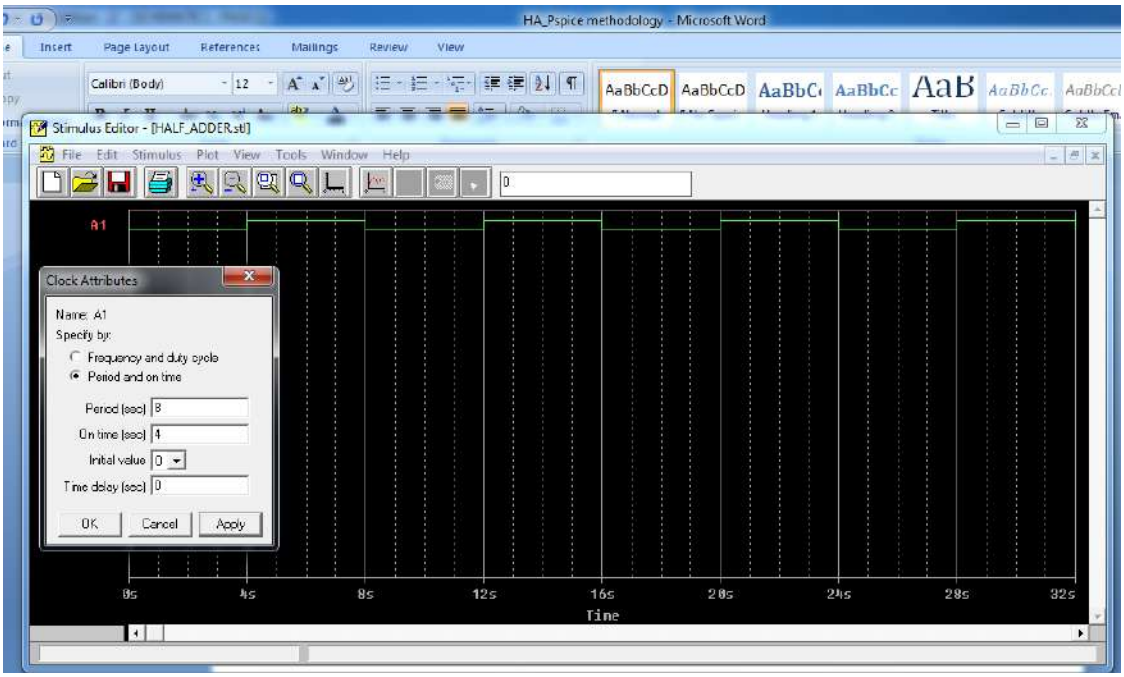
You should get a box. Make sure you name the stimulus whatever the part is named (in this case IA3). Make the input a "Clock" and click "OK".



19. Upon clicking OK, you get a dialog box as shown below. Select “Specify by Period and on time”. For this input, you should make the period 2^4 = 16 s and the on time half of the period (8 s) as shown below. Click “OK”.

Close out of the “Stimulus Editor”.

Save the changes and click “Yes” when asked if you want to update the schematic



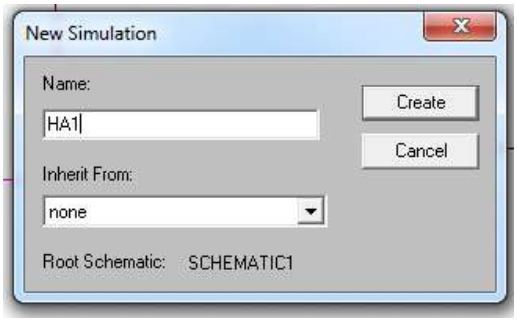
20. Similarly Configure the IA2,IA1,IA0 with period :16 and ON time: 8

21. Configure S_1 with period :4 and ON time: 2

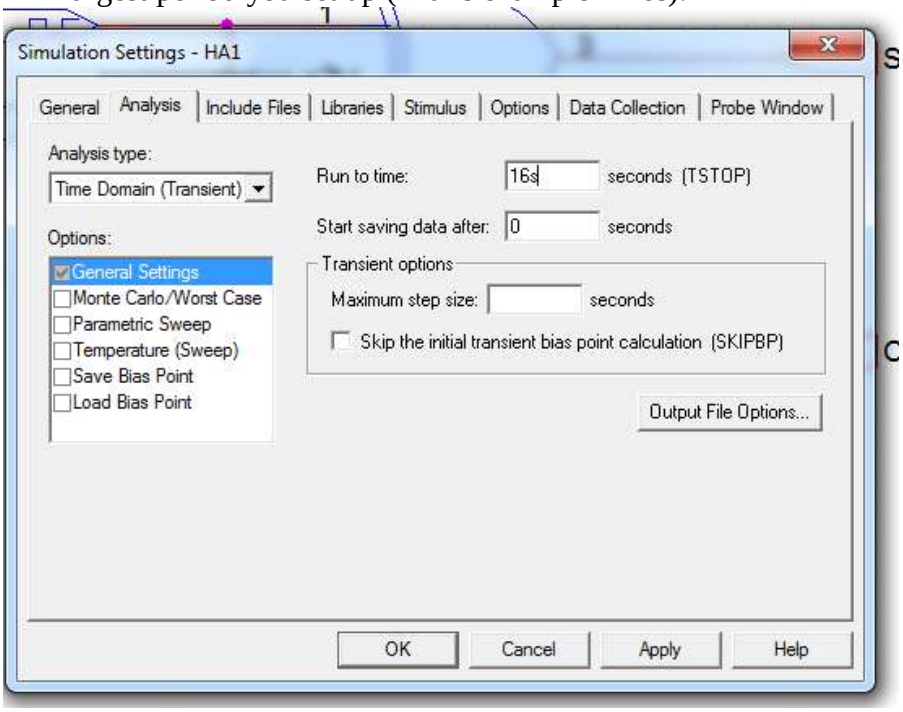
22. Configure S_0 with period :2 and ON time: 1

23. You are now ready to simulate the circuit. To do this select PSpice -> New Simulation Profile

24. You will get a dialog box as seen below. Give your simulation profile a name Multiplexer, inherit from “None” and click “Create”

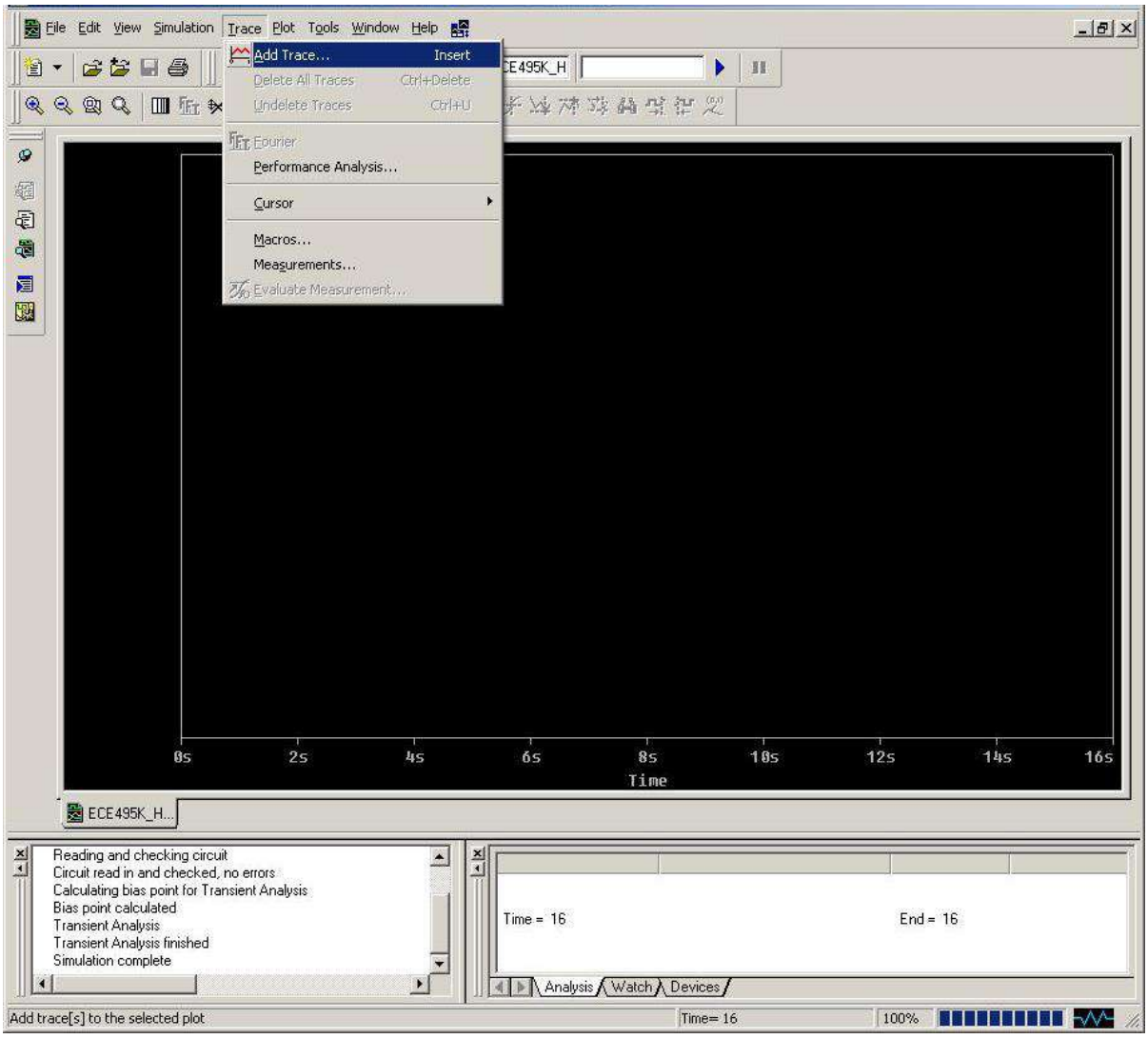


25. You should then get a dialog box as seen below. If you have set up your inputs correctly above, the only thing you need to do is change the "Run to time:" of the simulation to the largest period you set up (in this example – 16s).

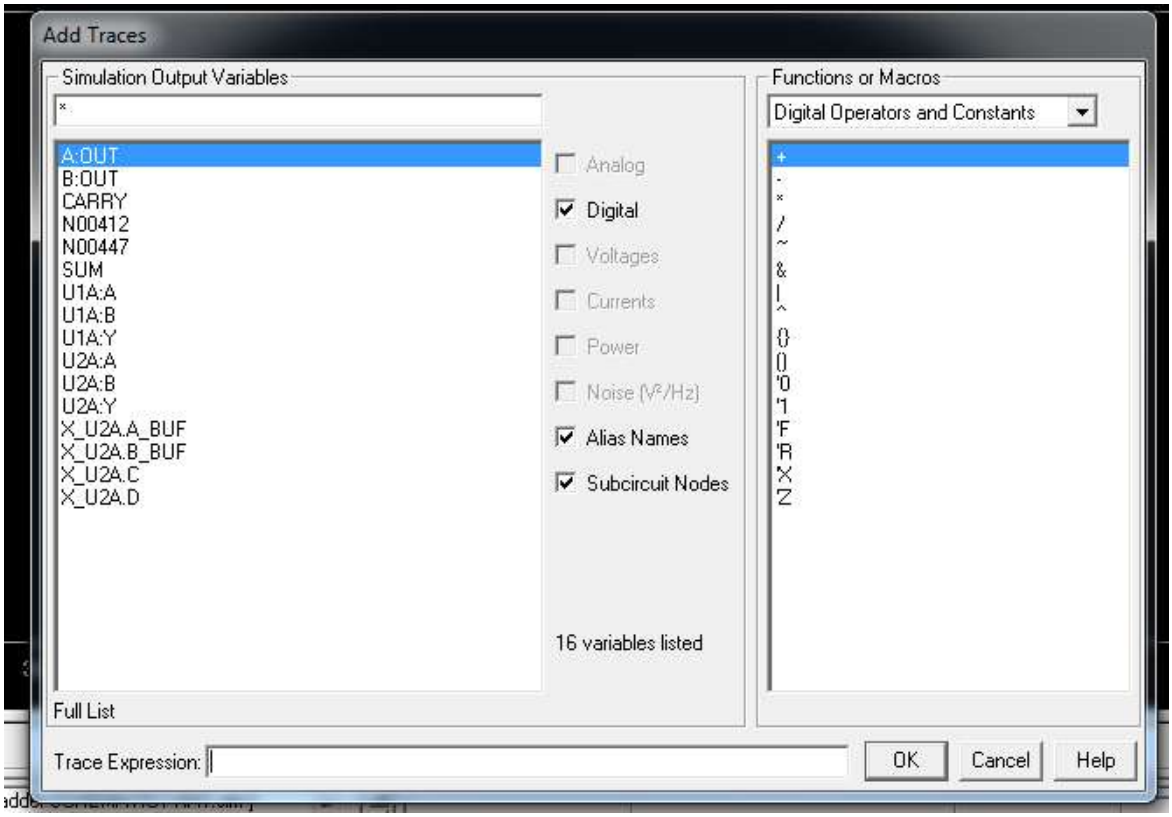


26. Click OK on the above dialog box. You should now be ready to run your simulation. Do so by clicking the  button.

27. After the simulation has completed you should get an empty black box as shown below. We want to look at our inputs compared to our output. To do so, we select "Trace->Add Trace…"

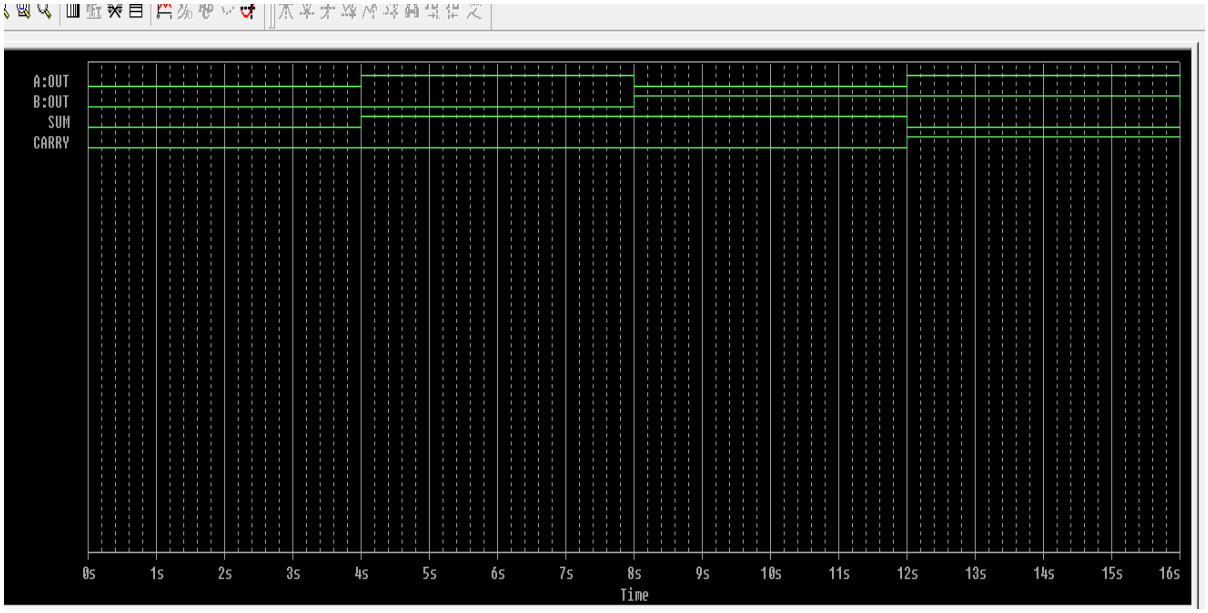

File Edit View Simulation Trace Plot Tools Window Help
Add Trace... Insert
Delete All Traces Ctrl+Delete
Undelete Traces Ctrl+U
Fourier
Performance Analysis...
Cursor
Macros...
Measurements...
Evaluate Measurement...
0s 2s 4s 6s 8s 10s 12s 14s 16s
Time
ECE495K_H...
Reading and checking circuit
Circuit read in and checked, no errors
Calculating bias point for Transient Analysis
Bias point calculated
Transient Analysis
Transient Analysis finished
Simulation complete
Time = 16
End = 16
Analysis Watch Devices
Add trace[s] to the selected plot
Time= 16
100%

28. The “Add Trace…” dialog box is seen below. We can only add one trace at a time. For now, select “S_1:OUT” and click “OK”.



29. Repeat steps 26 and 27 in the following order: S_0:OUT, Z_A

After doing so, your graph should look like below. If it does, you have completed the Multiplexer exercise successfully. Now observe the results and tally with the truth table



Truth tables:

4:1 Multiplexer :

Enable	Data Input Lines				Selection Lines		Output
$\overline{EA}$	I_{0A}	I_{1A}	I_{2A}	I_{3A}	S_1	S_0	Z_A
1	X	X	X	X	X	X	0
0	0	X	X	X	0	0	0
0	1	X	X	X	0	0	1
0	X	0	X	X	0	1	0
0	X	1	X	X	0	1	1
0	X	X	0	X	1	0	0
0	X	X	1	X	1	0	1
0	X	X	X	0	1	1	0
0	X	X	X	1	1	1	1

Result:

The waveforms obtained in the Pspice simulation is exactly following the truth table of Multiplexer. Hence the Multiplexer circuit is simulated in Pspice and observed the circuit behavior.

UNIT TEST –I

Model Question Paper (C-20)

EC-308, Digital Electronics Lab

TIME: 3 hours **Total Marks: 60M**

Instructions: (1) any one **full** question of the following shall be allotted to the students on lottery basis.

(2) All the questions are competency based and are for assessing the candidate's psychomotor skills

(3) Underpinning Knowledge shall be assessed through **Viva-Voice** for 6 Marks.

1 (a)

I. Identify the IC numbers of all Logic gates, logic input section, Logic output section, clock section, power supply section and breadboard sections of universal digital trainer kit
II. Identify the equivalent gate for AND-invert Gate and OR-invert Gate.
III. In a given IC how many NOT gates present.
IV. When one input of AND gate is connected to 1 and another input is connected to the clock, state the output?

(9M) (CO1)

(b)

I. Make the circuit connection to realize the function of AND gate and OR gate in logic trainer kit.
II. Make circuit connection to realize the function of NAND gate and NOR gate in logic trainer kit.

(15M) (CO1)

(c)

I. Make the circuit connection for NAND, NOR and EX-OR gates using basic gates on logic trainer kit and verify their truth tables.

(30M) (CO1)

2 (a)

I. Identify the IC numbers of all Logic gates, logic input section, Logic output section, clock section, power supply section and breadboard sections of universal digital trainer kit.
II. Show the output of NAND gate, when only one input is given to the both the inputs of NAND gate.
III. Make the circuit connection for NOT gate using NOR Gate.

(9M) (CO1)

(b)

II. Making connections for universal gates on logic trainer kits.

(15M) (CO1)

(c)

I. Make the circuit connection for EX-OR Gate using NOR & NAND on logic trainer kits and verify its truth tables

II. Make the circuit connection for NOR & NAND on logic trainer kits and verify its truth tables

(30M) (CO1)

3 (a)

I. Identify the IC numbers of Logic gates required to design HA and FA on logic trainer kit.

II. Identify the logic input section, Logic output section, clock section, power supply section and breadboard sections on logic trainer kit.

(9M) (CO2)

(b)

I. Make circuit connection for half adder using NAND gates.

II. Make circuit connection for half adder using NOR gates.

(15M) (CO2)

(c)

I. Make the connection of full adder circuit with two half adder and one OR gate on logic trainer kit and verify its truth table.

II. Is it possible to design Full adder circuit with alternative ICs? Justify?

(30M) (CO2)

4 (a)

I. Identify the major sections in trainer board and record the IC Nos

II. Mention number of outputs in 4 bit magnitude comparator.

(9M) (CO2)

(b)

I. Make connections of 4-bit magnitude comparator using IC 7485

II. Give the truth table of 4-bit magnitude comparator

(15M) (CO2)

(c)

I. Make the connection of 4-bit magnitude comparator using logic gates on logic trainer kits and verify its truth table.

(30M) (CO2)

5 (a)

I. Identify multiplexer section in the trainer board.

II. Mention the IC numbers of 4x1 and 8x1 multiplexers.

(9M) (CO2)

(b)

I. Make the connections of 4x1 multiplexer using IC 74153.

II. if selection line pins (S_1 and S_0) are connected in opposite direction, what happens justify?

(15M) (CO2)

(c)

I. Make the connection of 4x1 multiplexer circuit and Verify the truth table.

II. What happens at the output (Z_B) if we give data lines to A channel and enable pin low in IC74153.

(30M) (CO2)

6 (a)

I. Identify BCD to Seven segment decoder sections in the trainer board

II. Mention the ic number of BCD to Seven segment decoder.

(9M) (CO2)

(b)

I. Make connection of BCD to seven segment decoder using IC 7448.

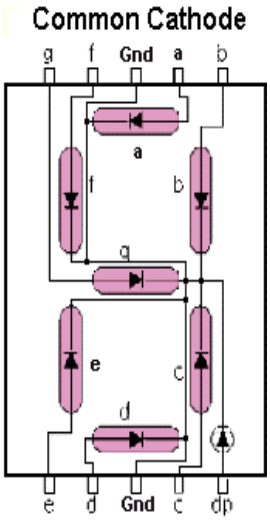
II. Write the truth table of BCD to seven segment decoder,

(15M) (CO2)

(c)

I. Verify the output by replacing 7448 with another IC.

II. Conduct the necessary exercise and state which diodes in seven segment display are **ON,** when display 7 is shown as output?



(30M) (CO2)

7(a)

I. Identify the major sections in a digital trainer kit

II. Identify the pin no. of enable inputs in the IC 74148

III. Identify various pins in IC 74138

(9M) (CO2)

(b)

I. Make the connections of encoder using IC 74148
II. Make the connections of decoder using IC 74138
III. Verify the truth tables of encoder
IV. Verify the truth tables of decoder

(15M) (CO2)

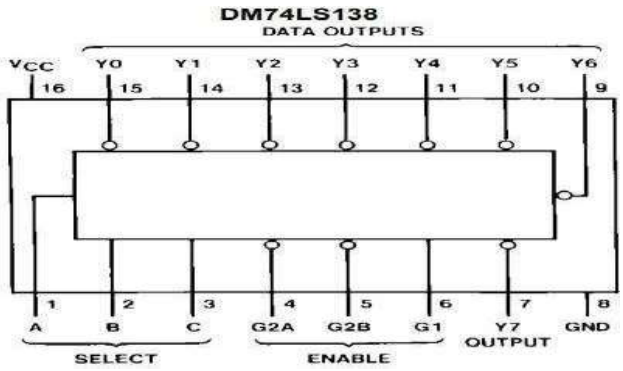
(c)

I. Given a readily made circuit to verify truth table of IC 74138 Decoder.

G_1	G_{2A}	G_{2B}	A	B	C	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7

II. Design a 3 to 8 Decoder, by change IC 74138 to IC 74156?

(30M) (CO2)



UNIT TEST –II

Model Question Paper (C-20)

EC-308, Digital Electronics Lab

TIME: 3 hours Total Marks: 60M

Instructions: (1) any one **full** question of the following shall be allotted to the students on lottery basis.

(2) All the questions are competency based and are for assessing the candidate's psychomotor skills

(3) Underpinning Knowledge shall be assessed through **Viva-Voice** for 6 Marks.

1 (a)

I. Identify SR, JK, T and D flip flop sections on the Digital trainer Kit
II. Identify clear, preset and clock sections on the Digital trainer Kit

(9M) (CO3)

(b)

I. Draw the pin configuration of IC 7400.
II. Make connections of SR flip-flop as per the circuit diagram
III. Make connections of JK flip-flop as per the circuit diagram
IV. What is the purpose of dual JK flip flop IC 7476

(15M) (CO3)

(c)

I. Perform an exercise to find out the output for SR clocked flip flop when the values S=0 and R=1, are given.
II. Perform an exercise to find out the output for SR clocked flip flop with negative edgetriggered clock of 1 H_z is given to the circuit.
III. Make the connection for JK flip-flop using SR Flip flop and verify its truth table
IV. Make the connection for T flip-flop using JK Flip flop and verify its truth table

(30M) (CO3)

2 (a)

I. Identifying decade, up/down and ripple counters sections in the trainer kit.
II. Identify the IC number used for ripple counter?

(9M) (CO3)

(b)

I. Make the circuit connection of 4-bit ripple counter with negative edge clock pulse.
II. Why do we use reset or clear signal when you get output state 1010 in designing BCD ripple counter?

(15M) (CO3)

(c)

I. Connect the logic circuit for 4-bit ripple counter and get the output 1110 by applying pulse input.

II. Connect the logic circuit for decade counter by using 7476 IC and AND GATE.

(30M) (CO3)

3 (a)

I. Identifying different counter sections in the trainer kit.

II. Identify the IC number used for decade counter.

III. Identify the pin numbers for clock, Vcc, reset of IC 7490.

(9M) (CO3)

(b)

I. Make the circuit connection for decade counter using IC 7490.

(15M) (CO3)

(c)

I. Construct mod-5 counter using IC 7490 and verify the number of output stage.

II. Construct mod-9 counter using IC 7490 and verify the number of output stage.

III. Verify the functioning of IC 7490 as decade counter.

(30M) (CO3)

4 (a)

I. Identify different counter sections in the trainer board.

II. Mention the IC number used for UP/DOWN counter.

(9M) (CO3)

(b)

I. Identify the pin numbers of UP/DOWN, ripple and enable signals of IC 7419.

II. Make the connections of UP/DOWN counter as per the circuit diagram.

(15M) (CO3)

(c)

I. Verify the counting process in 4-bit UP/DOWN counter for UP & DOWN counting.

II. Make the circuit connection of modulus-13 down counter and obtain the output waveforms.

(30M) (CO3)

5(a)

I. Identify the pin numbers for mode control inputs, serial data input and parallel data input in IC 7495.

(9M) (CO3)

(b)

I. Make the circuit connection for shift left operation using 7495 IC.

(15M) (CO3)

(c)

I. Make the circuit connection to operate in Parallel in Parallel out (PIPO) mode using IC 7495 and verify the process.
II. Make the circuit connection to operate in Serial in Serial out (PIPO) mode using IC 7495 and verify the process.

(30M) (CO3)

6(a)

I. Identify Menu Bar and various tabs under it when software is opened.
II. How do you create a project and save it in appropriate location in PC?
III. Identify the various symbols which are used to design circuit in PSpice software.

(9M) (CO4)

(b)

I. How can you apply clock signals set Time period & on time for a signal in PSpice.
II. How can you perform simulation of the designed circuits using ORCAD Pspice.
III. How can you customise label names for all the inputs/outputs of logic gates?
IV. How can you edit the logic diagram when it is required in Pspice?

(15M) (CO4)

(c)

I. Simulate AND,OR and NOT Gate using universal gates in Pspice software.
II. Simulate EX-OR gate using universal gates in Pspice software.

(30M) (CO4)

7 (a)

I. Identify Menu Bar and various tabs under it when software is opened.
II. How to give ground and Vcc connection for circuit in Pspice.
III. Identify different files created and saved when we use pspice software for an application.

(9M) (CO4)

(b)

I. Generate logic diagram for half adder using NAND gates on blank grid in Pspice.
II. Generate logic diagram for half adder using NOR gates on blank grid in Pspice.

(15M) (CO4)

(c)

I. Simulate half adder circuit using Pspice and show the input/output timing diagram.
II. Simulate Full adder circuit using Pspice and show the input/output timing diagram.

(30M) (CO4)

8 (a)

I. Show how to create an input files in Pspice.
II. Identify different tool bars in Pspice.
III. When should we use PSpice professional Version?

(9M) (CO4)

(b)

I. Generate logic diagram for 8x1 multiplexer using 4x1 multiplexer in Pspice.
II. Generate logic diagram for 8x1 multiplexer using 2x 1 multiplexer in Pspice.

(15M) (CO4)

(c)

I. Simulate 8x1 Multiplexter circuit using Pspice and show the input/output timing diagram.

(30M) (CO4)

Model Question Paper (C-20)

End Exam

EC-308, Digital Electronics Lab

TIME: 3 hours Total Marks: 60M

Instructions: (1) any one **full** question of the following shall be allotted to the students on lottery basis.

(2) All the questions are competency based and are for assessing the candidate's psychomotor skills

(3) Underpinning Knowledge shall be assessed through **Viva-Voice** for 6 Marks.

1. A) Identify logic input section, Logic output section, clock section, power supply section and breadboard sections of universal digital trainer (9M) (CO1)
   B) Using the Universal trainer, make circuit connections to realize the function of AND gate using NOR gates (15M) (CO1)
   C) Simulate Half Adder circuit using Pspice and show the input/output timing diagrams (30M) (CO4)
2. A) Draw the symbols of two input AND, OR, NOT, NAND, NOR gates and Identify the corresponding TTL digital ICs used in the lab (9M) (CO1)
   B) Connect four bit magnitude comparator and verify its functionality (15M) (CO2)
   C) Given the full adder circuit connected on the Universal trainer, apply various input combinations and note down the outputs. Then verify the truth table of full adder (30M) (CO2)
3. A) Draw the Circuit diagram of RS Flip flop using NAND gates. How can you convert it into JK flip flop (9M) (CO3)
   B) Connect the circuit of Decade counter using IC 7490 and verify its working on logic outputs (15M) (CO3)
   C) Given the mod-16 counter (ripple) connected on the universal trainer, demonstrate the conversion of the counter into mod-10 counter (30M) (CO3)
4. A) Verify the truth tables of two input AND, OR, NOT gates (9M) (CO1)
   B) Realize the functionality of EX-OR gate using only NAND gates (15M) (CO1)
   C) With the given JK flip flop circuit, construct D-Flip flop and T-Flip flop and verify their truth tables (30M) (CO3)
5. A) Draw the circuit symbols of level triggered JK Flip flop, Positive edge triggered JK flip flop and negative edge triggered JK flip flop (9M) (CO3)
   B) Realize the functionality of EX-OR gate using basic gates (15M) (CO1)
   C) Simulate full adder circuit using Pspice (30M) (CO4)

6. A) Demonstrate the steps to place NAND gate onto work space in PSpice (9M) (CO4)
   B) Construct BCD to seven segment decoder circuits using 7448 IC (15M) (CO2)
   C) From the given 4-bit magnitude comparator circuit readily connected, verify its function (30M) (CO2)

7. A) Troubleshoot the half adder circuit if the following truth table is observed (9M) (CO2)

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	1	1

   B) Demonstrate the steps to apply Pspice stimulus to the NOT gate in PSpice (15M) (CO4)
   C) Construct shift register using IC 7495 and demonstrate the shifting of data when clock input is applied (30M) (CO3)

8. A) Troubleshoot the JK flipflop circuit if it is working like T-flipflop (9M) (CO3)
   B) Construct up/down counter using IC 74190 (15M) (CO3)
   C) Simulate 4-bit magnitude comparator using IC7485 in Pspice and demonstrate its functionality (30M) (CO4)