Code No: **R163202C** **R16** SET - 1

III B. Tech II Semester Regular/Supplementary Examinations, August-2021

VLSI DESIGN

(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

~~~~~~

PART –A **(14 Marks)**

1. a) Define Figure of Merit. [2M]
   b) What are the uses of Stick diagrams? [2M]
   c) Define Fan-in and Fan-out. [2M]
   d) Mention the limitations of scaling of MOS circuits. [3M]
   e) What are feed-through cells? State their uses. [3M]
   f) Give an overview of power consumption. [2M]

PART –B **(56 Marks)**

2. a) Explain the latch-up phenomenon in CMOS circuits and the methods by which that can be eliminated. [7M]
   b) Why NMOS technology is preferred more than PMOS technology? Explain. [7M]

3. Draw the static CMOS logic circuit for the following expressions: [14M]
   i) Y= (ABCD)′ ; ii) Y= [D(A+BC)]′.

4. a) Explain different capacitances present in CMOS design. [7M]
   b) Write notes on sheet resistance concept and its applications. [7M]

5. a) Explain in detail about BIST. [7M]
   b) Explain how an improved layout can reduce faults in CMOS circuits? [7M]

6. a) Write a note on Ad Hoc testable design techniques. [7M]
   b) Explain the operation of a basic 4 bit adder. [7M]

7. a) Discuss about Power Grid and Clock Design in low power VLSI design. [7M]
   b) Explain the any one method of reduction of switching capacitance. [7M]

*****

|''|''|||''|'''|||'|
~~~~~~