Code No: **R1632044** **R16** SET - 1

**III B. Tech II Semester Regular/Supplementary Examinations, August-2021**

**DIGITAL SIGNAL PROCESSING**

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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**PART –A** **(14 Marks)**

1. a) Define the energy and power signal. [2M]
   b) What are the applications of FFT algorithm? [2M]
   c) What are the advantages and disadvantages of bilinear transformation? [2M]
   d) What is Gibb's phenomenon? [3M]
   e) What are the applications of Interpolation? [3M]
   f) Describe the significance of program controller. [2M]

**PART –B** **(56 Marks)**

2. a) Determine the response of the causal system: [7M]
   y(n)-y(n-1)=x(n)+x(n-1) for the inputs x(n)=u(n) and x(n)=2–n u(n).
   b) Find the inverse z-transform of x(z) = $(z^2+z)/(z-1)(z-3)$, ROC: z > 3; using Partial fraction method. [7M]

3. a) State and prove the circular convolution property of DFT. [7M]
   b) Given x(n)={0,1,2,3,4,5,6,7}. Find X(k) using DIT FFT algorithm. [7M]

4. a) Use impulse invariance to obtain H(z) if T= 1 sec and H(s) is: [7M]
   (i) $\frac{1}{(S^3+3S^2+4S+1)}$ (ii) $\frac{1}{(S^2+\sqrt{2}\,S+1)}$
   b) Design a Butterworth low pass filter satisfying the specifications: [7M]
   $F_p$=0.10 Hz; $\alpha_p$=0.5 dB; $f_s$=0.15 Hz; $\alpha_s$=15 dB; F=1 Hz.

5. a) Using a rectangular window technique, design a low pass filter with pass band gain of unity, cut off frequency of 1 kHz and working at a sampling frequency of 5 kHz. The length of the impulse response should be 7. [7M]
   b) Prove that an FIR filter has linear phase if the unit sample response satisfies the condition: h(n)= ±h(M-1-n), n=0,1,….M-1. Also discuss symmetric and antisymmetric cases of FIR filter. [7M]

6. a) Explain the time and frequency domain description of a decimator. [7M]
   b) Explain the concept of multirate signal processing with spectral interpretation of decimation of a signal from 8 kHz to 2 kHz and spectral interpretation of a signal from 2 kHz to 8 kHz. [7M]

7. a) Discuss about the Central Arithmetic Logic Unit and Auxiliary Registrar of TMS 320C5X DSP processor. [7M]
   b) What are the various memory access schemes in DSP processors? Explain. [7M]

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