Code No: **R1632043** **R16** SET - 1

**III B. Tech II Semester Regular/Supplementary Examinations, August-2021**

**VLSI DESIGN**

(Common to Electronics and Communication Engineering, Electronics and Instrumentation Engineering, Electronics and Computer Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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**PART –A** **(14 Marks)**

1. a) Explain the role of pass transistors. [2M]
   b) What is the fundamental goal in device modelling? [2M]
   c) Write a short note on Propagation Delays. [2M]
   d) Define ESD protection. [3M]
   e) Write the principle of any one fast multiplier. [3M]
   f) What is the interconnect design. [2M]

**PART –B** **(56 Marks)**

2. a) With neat diagrams, explain the different steps in p-well fabrication of CMOS transistors. [7M]
   b) Explain with neat diagrams the various NMOS fabrication technologies. [7M]

3. a) Using flow diagram explain the VLSI design process. [7M]
   b) Draw the stick diagram layout of 8:1 inverter using nMOS and CMOS technologies. [7M]

4. a) Derive the expression for the CMOS inverter delay. [7M]
   b) Explain about the scaling models and the scaling factors of MOS circuits. [7M]

5. a) Write short note on chip input circuits and output circuits. [7M]
   b) Explain fault models of VLSI Design. [7M]

6. a) Explain the configuration and logic block architecture of a FPGA. [7M]
   b) Draw the structure of a 4×4 static RAM and explain its operation. [7M]

7. a) Explain the various types of IC packages. [7M]
   b) Explain the need for low power design circuits in VLSI chip fabrication. [7M]

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