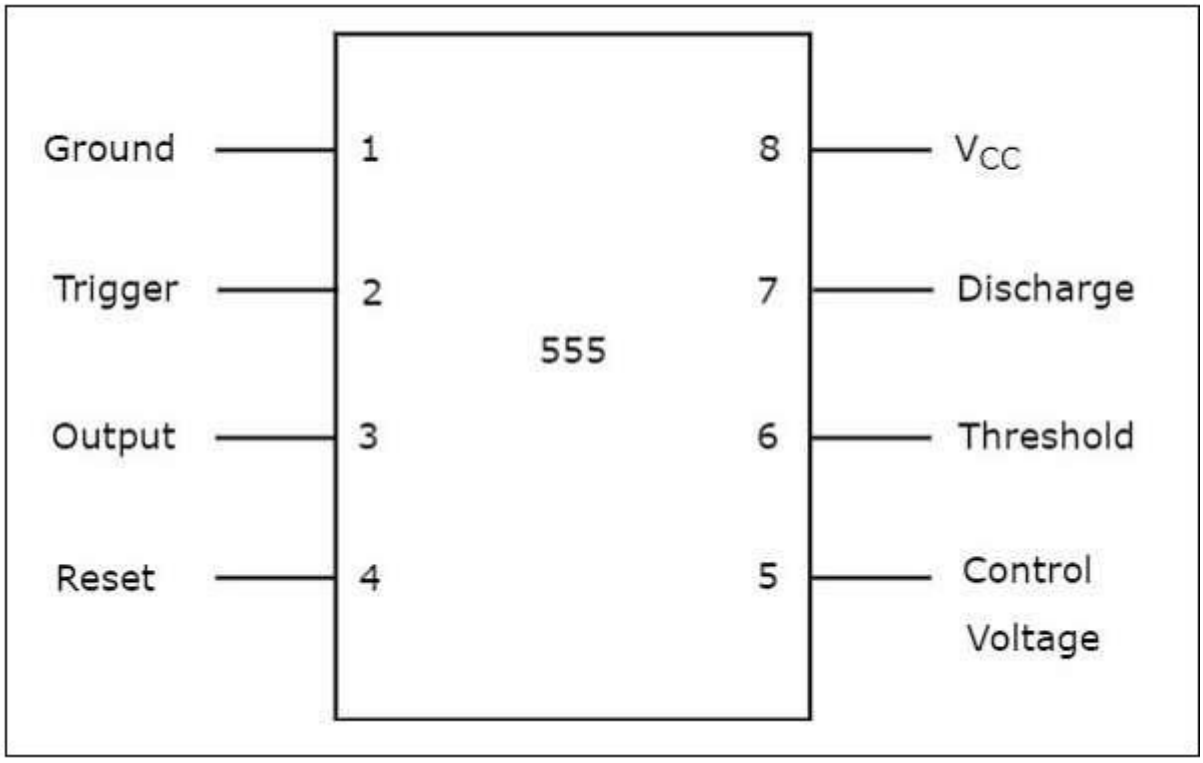
MODULE-III - 555 Timers

The **555 Timer** IC got its name from the three 5KΩ resistors that are used in its voltage divider network. This IC is useful for generating accurate time delays and oscillations.

Pin Diagram and Functional Diagram:

Pin Diagram:

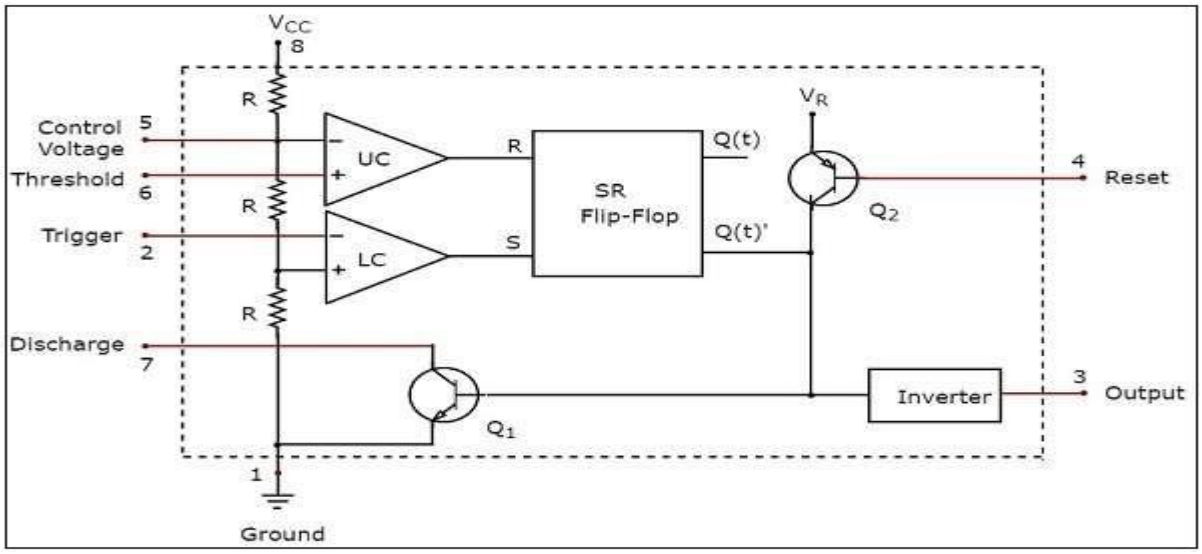
The 555 Timer IC is an 8 pin mini Dual-Inline Package (DIP). The **pin diagram** of a 555 Timer:



The significance of each pin is self-explanatory from the above diagram. This 555 Timer IC can be operated with a DC supply of +5V to +18V. It is mainly useful for generating **non-sinusoidal** wave forms like square, ramp, pulse & etc

Functional Diagram:

The pictorial representation showing the internal details of a 555 Timer is known as functional diagram. The **functional diagram** of 555 Timer IC is shown below:



Observe that the functional diagram of 555 Timer contains a voltage divider network, two comparators, one SR flip-flop, two transistors and an inverter. This section discusses about the purpose of each block or component in detail −

Voltage Divider Network

- The voltage divider network consists of a three 5KΩ5KΩ resistors that are connected in series between the supply voltage VccVcc and ground.
- This network provides a voltage of Vcc3Vcc3 between a point and ground, if there exists only one 5KΩ5KΩ resistor. Similarly, it provides a voltage of 2Vcc32Vcc3 between a point and ground, if there exists only two 5KΩ5KΩ resistors.

Comparator

- The functional diagram of a 555 Timer IC consists of two comparators: an Upper Comparator (UC) and a Lower Comparator (LC).
- Recall that a **comparator** compares the two inputs that are applied to it and produces an output.
- If the voltage present at the non-inverting terminal of an op-amp is greater than the voltage present at its inverting terminal, then the output of comparator will be +Vsat+Vsat. This can be considered as **Logic High** ('1') in digital representation.
- If the voltage present at the non-inverting terminal of op-amp is less than or equal to the voltage at its inverting terminal, then the output of comparator will be −Vsat−Vsat. This can be considered as **Logic Low** ('0') in digital representation.

SR Flip-Flop

- Recall that a **SR flip-flop** operates with either positive clock transitions or negative clock transitions. It has two inputs: S and R, and two outputs: Q(t) and Q(t)'. The outputs, Q(t) & Q(t)' are complement to each other.
- The following table shows the **state table** of a SR flip-flop:

S	R	Q(t+1)

0	0	Q(t)
0	1	0
1	0	1
1	1	-

- Here, Q(t) & Q(t+1) are present state & next state respectively. So, SR flip-flop can be used for one of these three functions such as Hold, Reset & Set based on the input conditions, when positive (negative) transition of clock signal is applied.
- The outputs of Lower Comparator (LC) and Upper Comparator (UC) are applied as **inputs of SR flip-flop** as shown in the functional diagram of 555 Timer IC.

Transistors and Inverter

- The functional diagram of a 555 Timer IC consists of one npn transistor Q1Q1 and one pnp transistor Q2Q2. The npn transistor Q1Q1 will be turned ON if its base to emitter voltage is positive and greater than cut-in voltage. Otherwise, it will be turned-OFF.
- The pnp transistor Q2Q2 is used as **buffer** in order to isolate the reset input from SR flip-flop and npn transistor Q1Q1.
- The **inverter** used in the functional diagram of a 555 Timer IC not only performs the inverting action but also amplifies the power level.

The 555 Timer IC can be used in mono stable operation in order to produce a pulse at the output. Similarly, it can be used in astable operation in order to produce a square wave at the output.

Phase Locked Loops

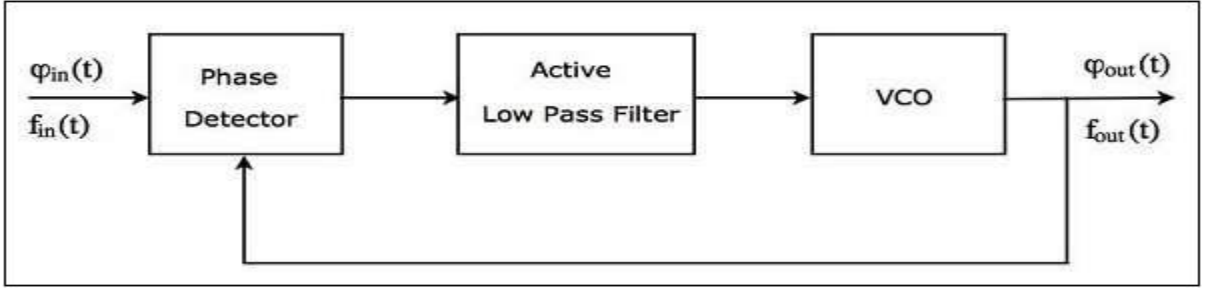
Phase Locked Loop **(PLL)** is one of the vital blocks in linear systems. It is useful in communication systems such as radars, satellites, FMs, etc.

Block Diagram of PLL:

A Phase Locked Loop (PLL) mainly consists of the following **three blocks** −

- Phase Detector
- Active Low Pass Filter
- Voltage Controlled Oscillator (VCO)

The **block diagram** of PLL is shown in the following figure −



The output of a phase detector is applied as an input of active low pass filter. Similarly, the output of active low pass filter is applied as an input of VCO.

The **working** of a PLL is as follows −

- **Phase detector** produces a DC voltage, which is proportional to the phase difference between the input signal having frequency of finfin and feedback (output) signal having frequency of fout.
- A **Phase detector** is a multiplier and it produces two frequency components at its output − sum of the frequencies finfin and foutfout and difference of frequencies finfin & foutfout.
- An **active low pass filter** produces a DC voltage at its output, after eliminating high frequency component present in the output of the phase detector. It also amplifies the signal.
- A **VCO** produces a signal having a certain frequency, when there is no input applied to it. This frequency can be shifted to either side by applying a DC voltage to it. Therefore, the frequency deviation is directly proportional to the DC voltage present at the output of a low pass filter.

The above operations take place until the VCO frequency equals to the input signal frequency. Based on the type of application, we can use either the output of active low pass filter or output of a VCO. PLLs are used in many **applications** such as FM demodulator, clock generator etc.

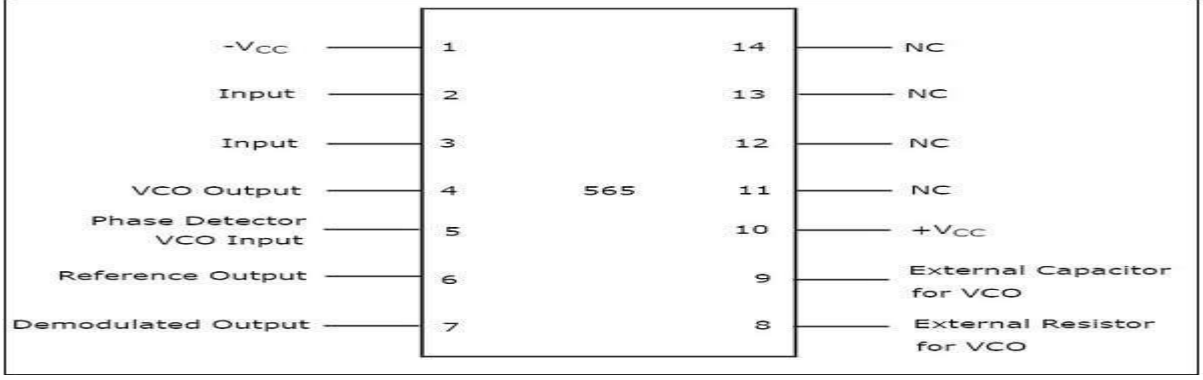
PLL operates in one of the **following three modes** −

- Free running mode
- Capture mode
- Lock mode

Initially, PLL operates in **free running mode** when no input is applied to it. When an input signal having some frequency is applied to PLL, then the output signal frequency of VCO will start change. At this stage, the PLL is said to be operating in the **capture mode**. The output signal frequency of VCO will change continuously until it is equal to the input signal frequency. Now, it is said to be PLL is operating in the **lock mode**.

IC 565:

IC 565 is the most commonly used in phase locked loop IC. It is a 14 pin Dual-Inline Package (DIP). The **pin diagram** of IC 565 is shown in the following figure −



The purpose of each pin is self-explanatory from the above diagram. Out of 14 pins, only 10 pins (pin number 1 to 10) are utilized for the operation of PLL. So, the remaining 4 pins (pin number 11 to 14) are labelled with NC (No Connection).

The **VCO** produces an output at pin number 4 of IC 565, when the pin numbers 2 and 3 are grounded. Mathematically, we can write the output frequency, fout of the VCO:

$$fout=0.25R_VC_V$$

where, R_V is the external resistor that is connected to the pin number 8

C_V is the external capacitor that is connected to the pin number 9

- By choosing proper values of R_V and C_V, we can determine the output frequency, fout of VCO.
- **Pin numbers 4 and 5** are to be shorted with an external wire so that the output of VCO can be applied as one of the inputs of phase detector.
- IC 565 has an internal resistance of 3.6KΩ. A capacitor, C has to be connected between pin numbers 7 and 10 in order to make a **low pass filter** with that internal resistance.

Module-IV:Voltage Regulators

The function of a voltage regulator is to maintain a constant DC voltage at the output irrespective of voltage fluctuations at the input and (or) variations in the load current. In other words, voltage regulator produces a regulated DC output voltage.

Voltage regulators are also available in Integrated Circuits (IC) forms. These are called as voltage regulator ICs.

Types of Voltage Regulators

There are two types of voltage regulators −

- Fixed voltage regulator
- Adjustable voltage regulator

Fixed voltage regulator:

A fixed voltage regulator produces a fixed DC output voltage, which is either positive or negative. In other words, some fixed voltage regulators produce positive fixed DC voltage values, while others produce negative fixed DC voltage values.

78xx voltage regulator ICs produce positive fixed DC voltage values, whereas, 79xx voltage regulator ICs produce negative fixed DC voltage values.