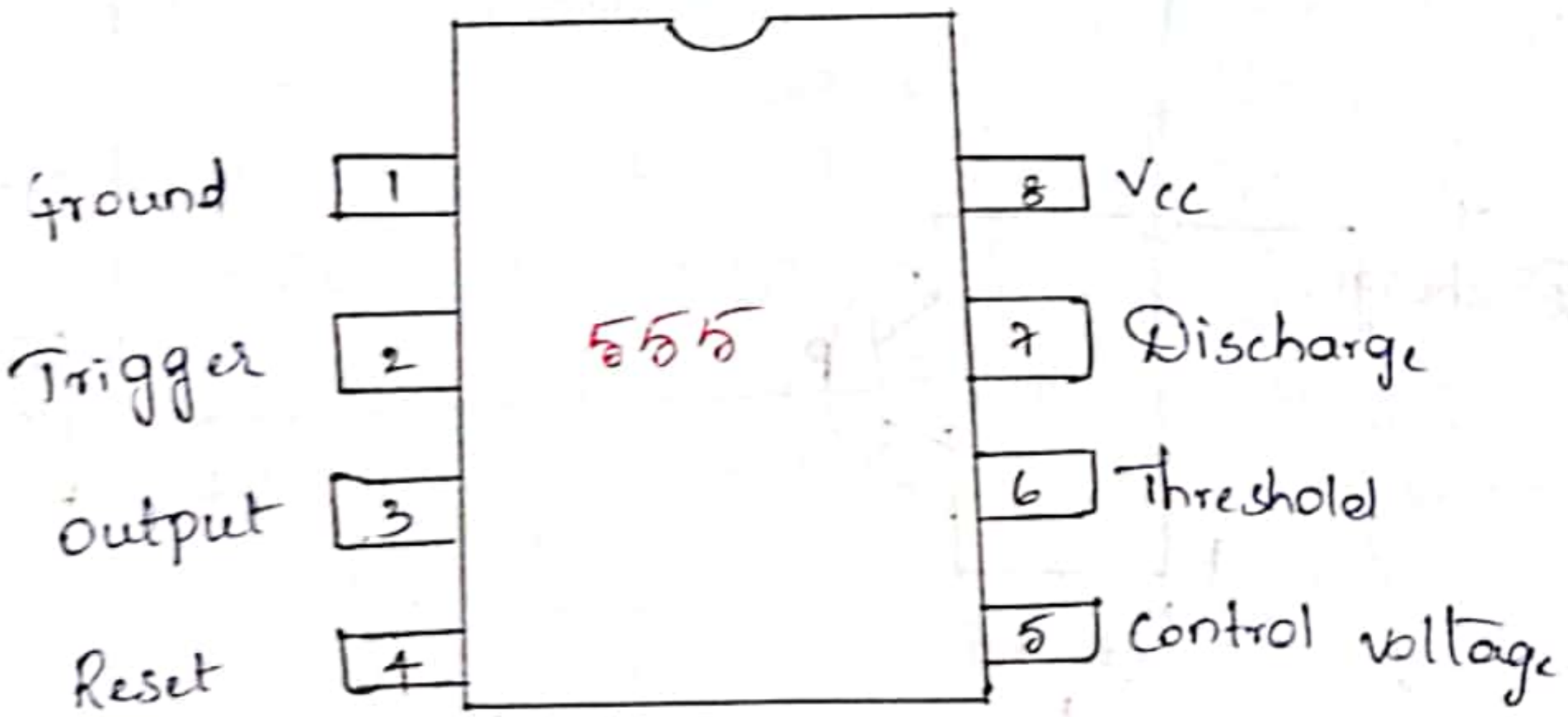
555 TIMER.

* The 555 timer is highly stable device for generating accurate time delay or oscillations.

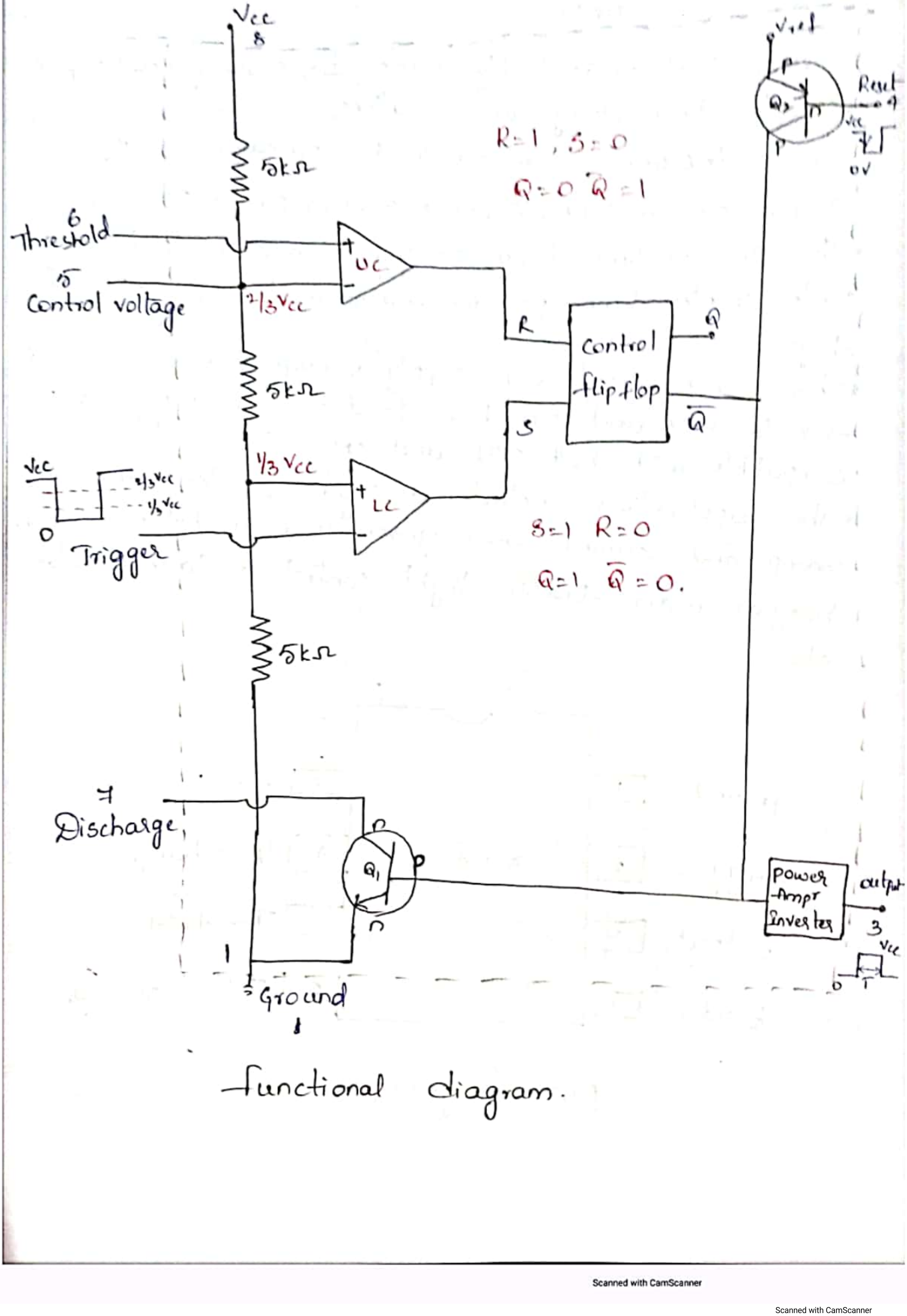
SE 555 / NE 555 - Available in two packages.

8 pin circular style, 8 pin DIP or 14 pin DIP.

* This provides time delay ranging from μsec to hours while counter timer, provides maximum timing range of days.
* This can be used with supply voltage in the range of +5V to +18V, and can drive load upto 200mA. This is compatible with both TTL and CMOS logic ckts.
* The applications include oscillators, pulse generator, ramp and square wave generator, Monoshot multivibrator, burglar alarm, traffic light control, voltage monitor etc.



Pin diagram.



functional diagram.

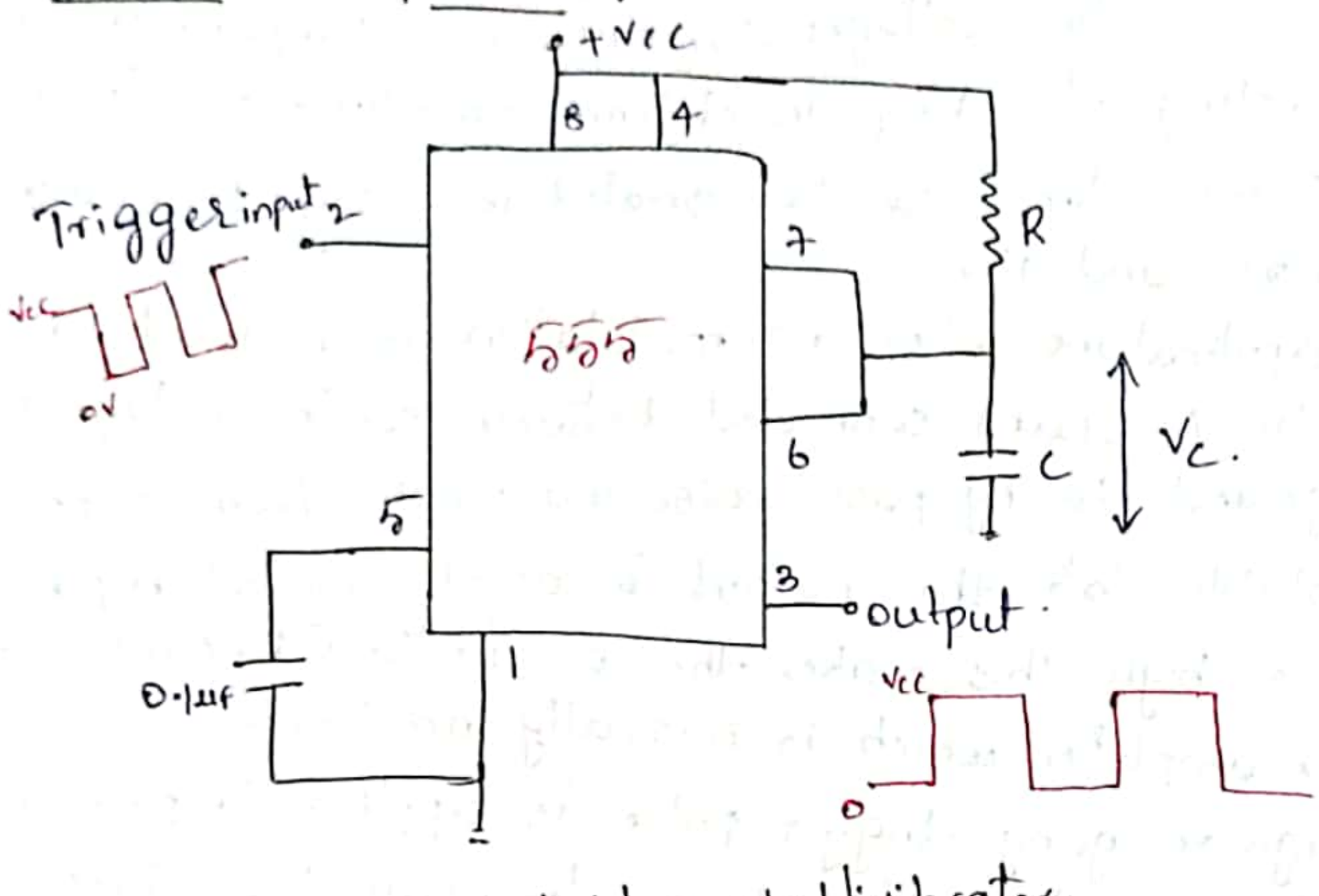
Scanned with CamScanner

Description :-

* Three resistors of 5kΩ of internal resistors acts as a voltage divider, providing bias voltage $(\frac{2}{3})V_{cc}$ to upper comparator (UC) and $(\frac{1}{3})V_{cc}$ to lower comparator [LC] where as V_{cc} is the supply voltage.
* Since these two voltages fix necessary comparator threshold voltage, they also help in determining timing interval.
* The Ic 555 timer can be operated with supply voltage blw 4.5v and 16v.
* In applications where no modulation is required, a capacitor (0.01μf) connected between control voltage (pin 5) and ground to by-pass noise low ripple from supply.
* In stable state, the output $\bar{Q}$ of the control flip-flop (ff) is high. This makes the output 'low' because of power amplifier which is basically an Inverter.
* A negative going trigger pulse is applied to pin 2 and should have its dc level greater than the threshold level of lower comparator ($\frac{1}{3}V_{cc}$).
* At negative going edge of trigger, as trigger passes through $\frac{1}{3}V_{cc}$, the output of lower comparator goes high and sets ff [$\bar{Q}=0$, $Q=1$]
* During the positive excursion when the threshold voltage at pin 6 passes through $\frac{2}{3}V_{cc}$ the output of upper comparator goes High and resets the ff [$Q=0$, $\bar{Q}=1$]
* The reset input (pin 4) resets ff overriding the effect of any instruction coming to ff from lower comparator.

* The transistor Q_2 serves as buffer to isolate the reset input from ff and the transistor Q_1. Also Q_1 is driven by an Internal reference voltage V_{ref} obtained from supply voltage V_{cc}.

* Monostable operation :-

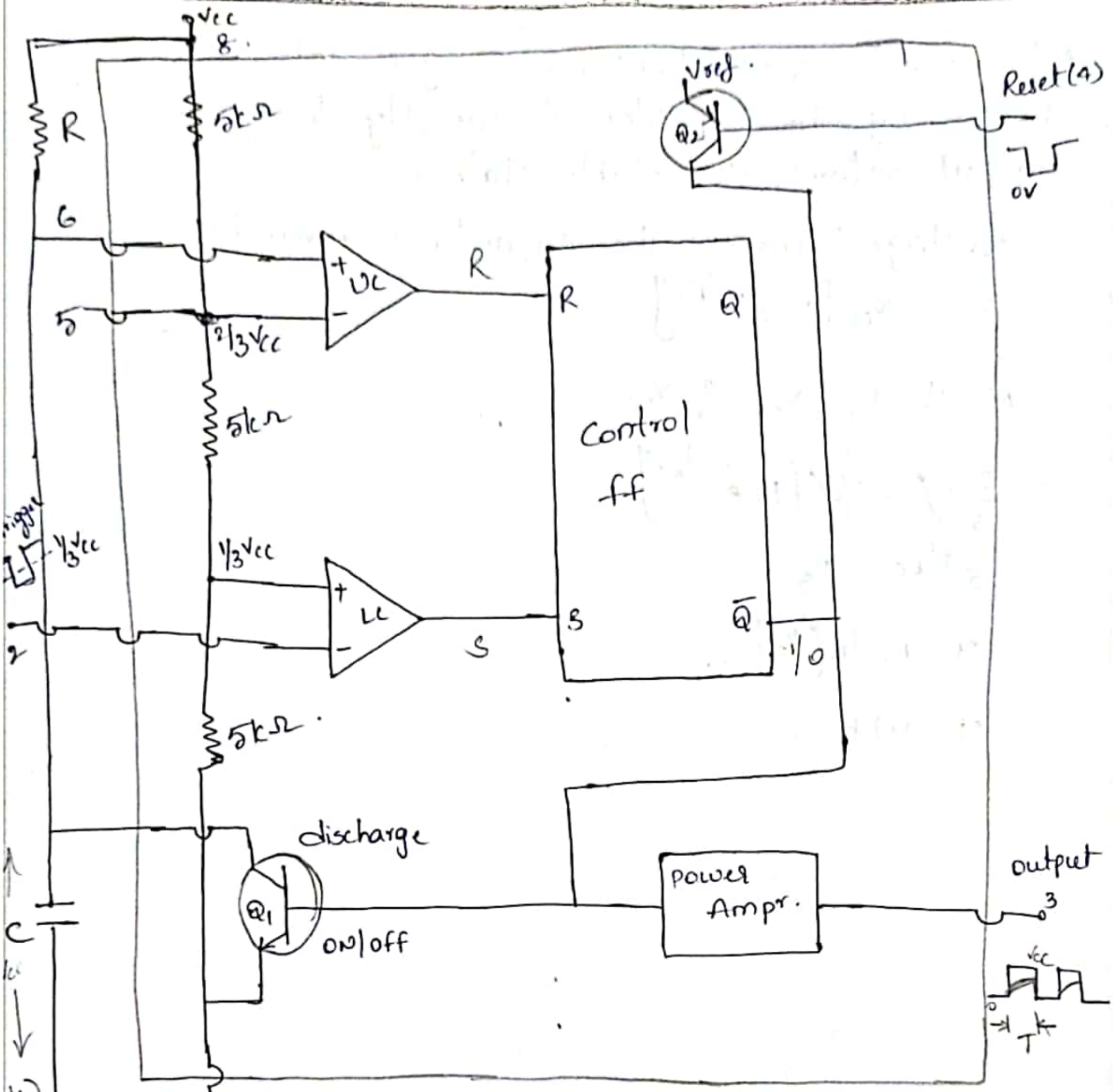


Monostable Multivibrator.

operation :-

. In stable state, ff holds transistors ON (Q_1) thus clamping the external timing capacitor 'c' to ground. The output remains at ground (Low).

* As trigger passes through $\frac{1}{3}V_{cc}$, ff is set i.e $S=1, R=0 \Rightarrow \bar{Q}=0$ [$Q=1$] This makes the transistor Q_1 off ord short circuit across timing capacitor c is released.



functional Diagram.

*As $\bar{Q}$ is low, output goes high (V_{cc}). The timing cycle now begins. Since 'C' is unclamped, voltage across it rises exponentially through R towards V_{cc} with time constant Rc.

*After time period 'T' the capacitor voltage is just greater than $\frac{2}{3}V_{cc}$ and upper comparator resets the ff. R=1, S=0; $\bar{Q}$ = 1 [Q=0]

*This makes $\bar{Q}=1$ transistor Q_1 goes ON thereby discharging the capacitor 'c' rapidly to ground. The output returns to stable state.

Voltage across the capacitor is given by.

$$V_c = V_{cc}\left[1 - e^{-t/Rc}\right]$$

At $t = T$, $V_c = \frac{2}{3} V_{cc}$

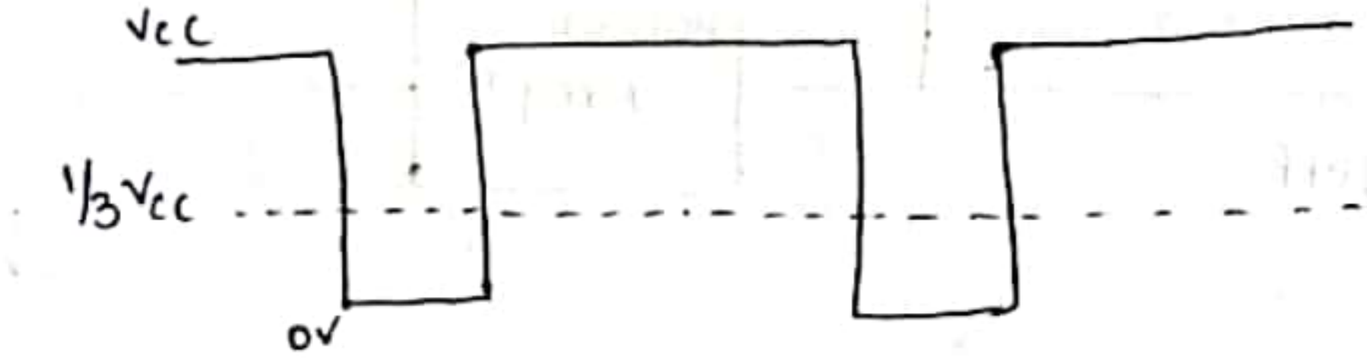
$$\frac{2}{3}V_{cc} = V_{cc}\left[1 - e^{-t/Rc}\right]$$

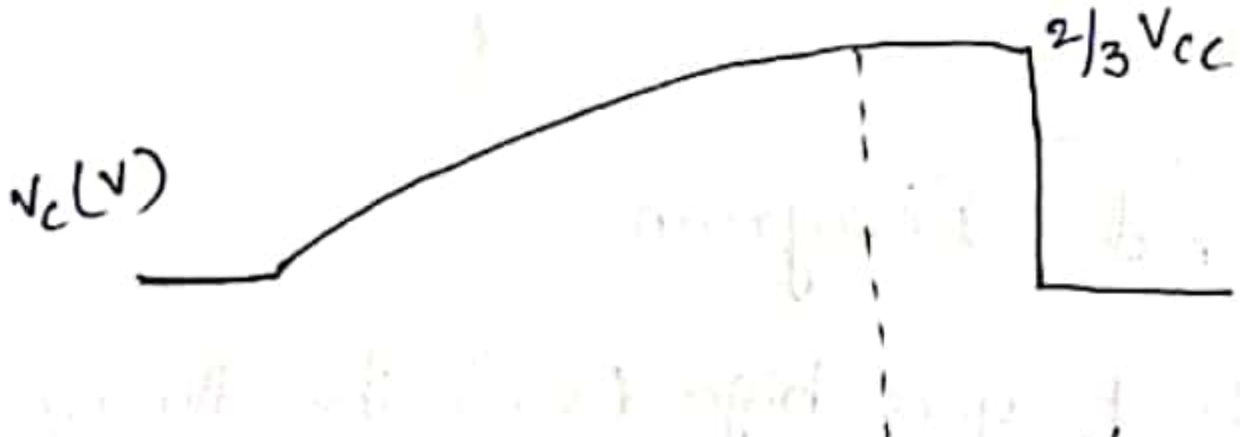
$$e^{-T/Rc} = 1/3$$

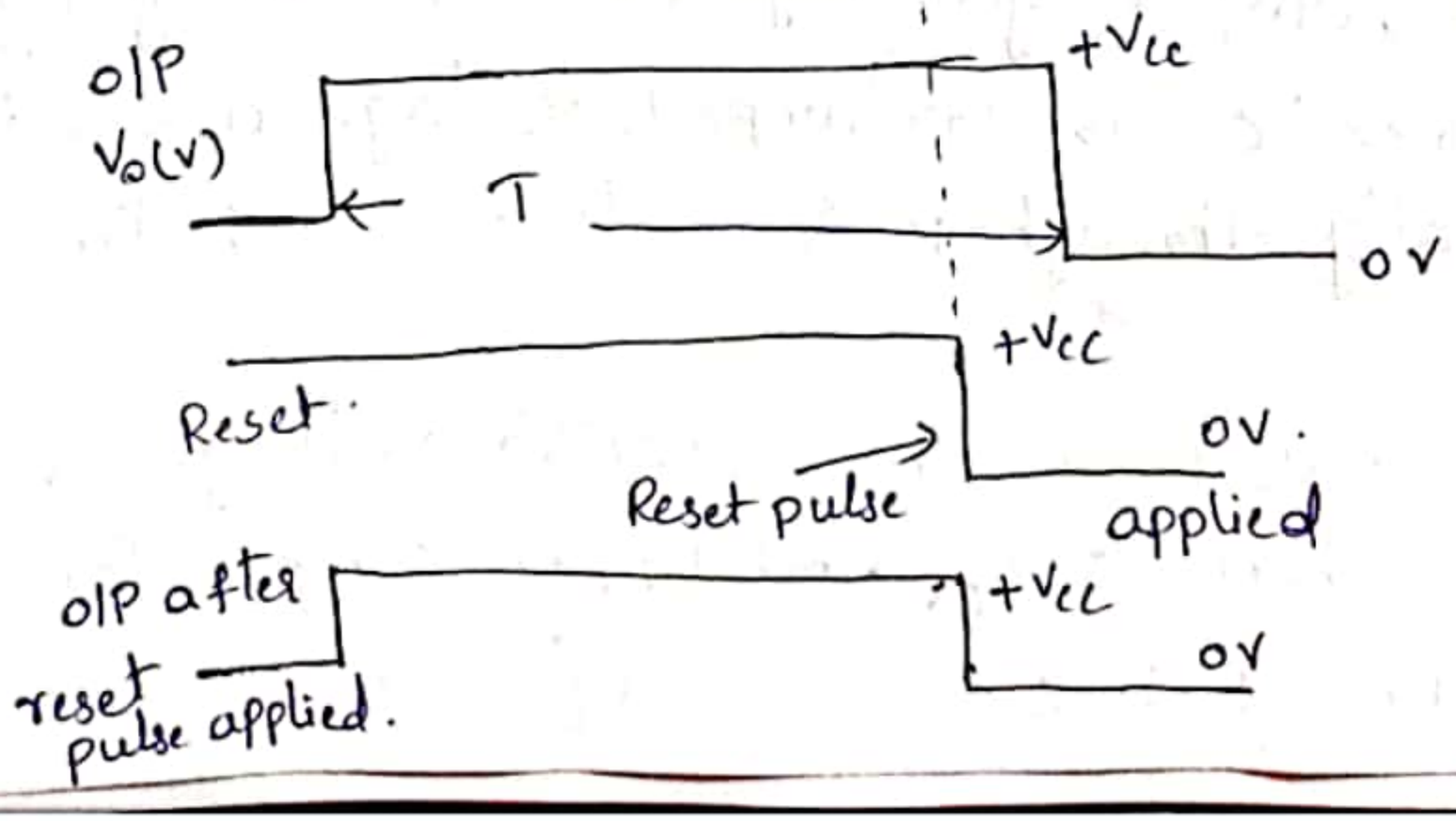
$$T = Rc \ln[1/3]$$

$$T = 1.1\,Rc.$$

Timing pulse :-







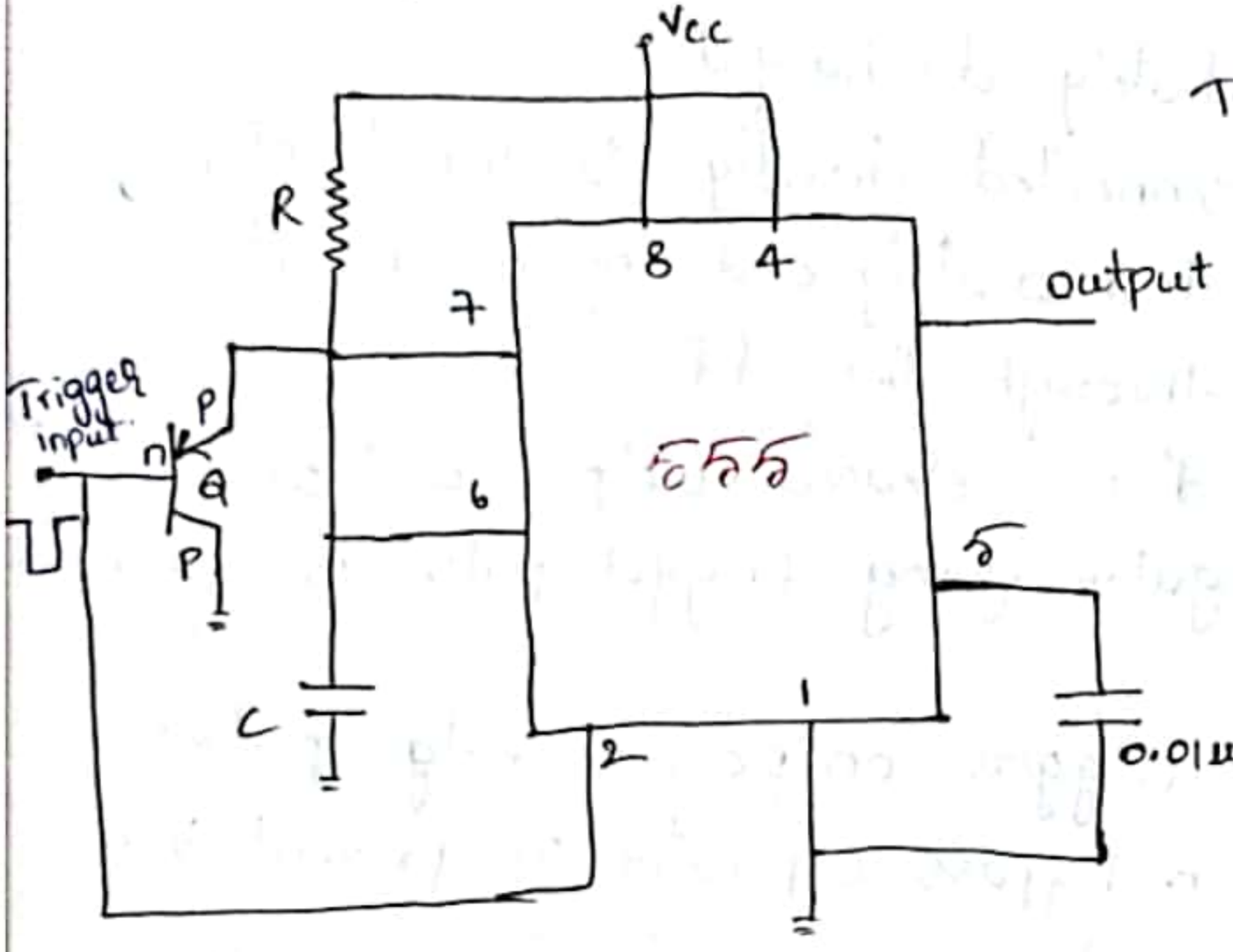
* The timing interval is independent of the supply voltage once triggered the output remains in High state until time T elapses which depends on value of R and C.
* Any additional trigger pulse coming during this time will not change the output state. If a negative going reset pulse is applied to reset terminal [pin 4) during timing cycle transistor Q_2 goes off, Q_1 turns ON and external timing capacitor C is immediately discharged
* The output Q_2 is connected directly to input of Q_1 so as to turn ON Q_1 immediately and thereby avoid propagationed delay through the f-f.
* Even if the reset f is released, output will still remain low until negative going trigger pulse is again applied to pin 2.
* Monostable ckt mis-triggers on positive edge pulses, even with control pin bypass capacitor. To prevent this modified ckt is used.

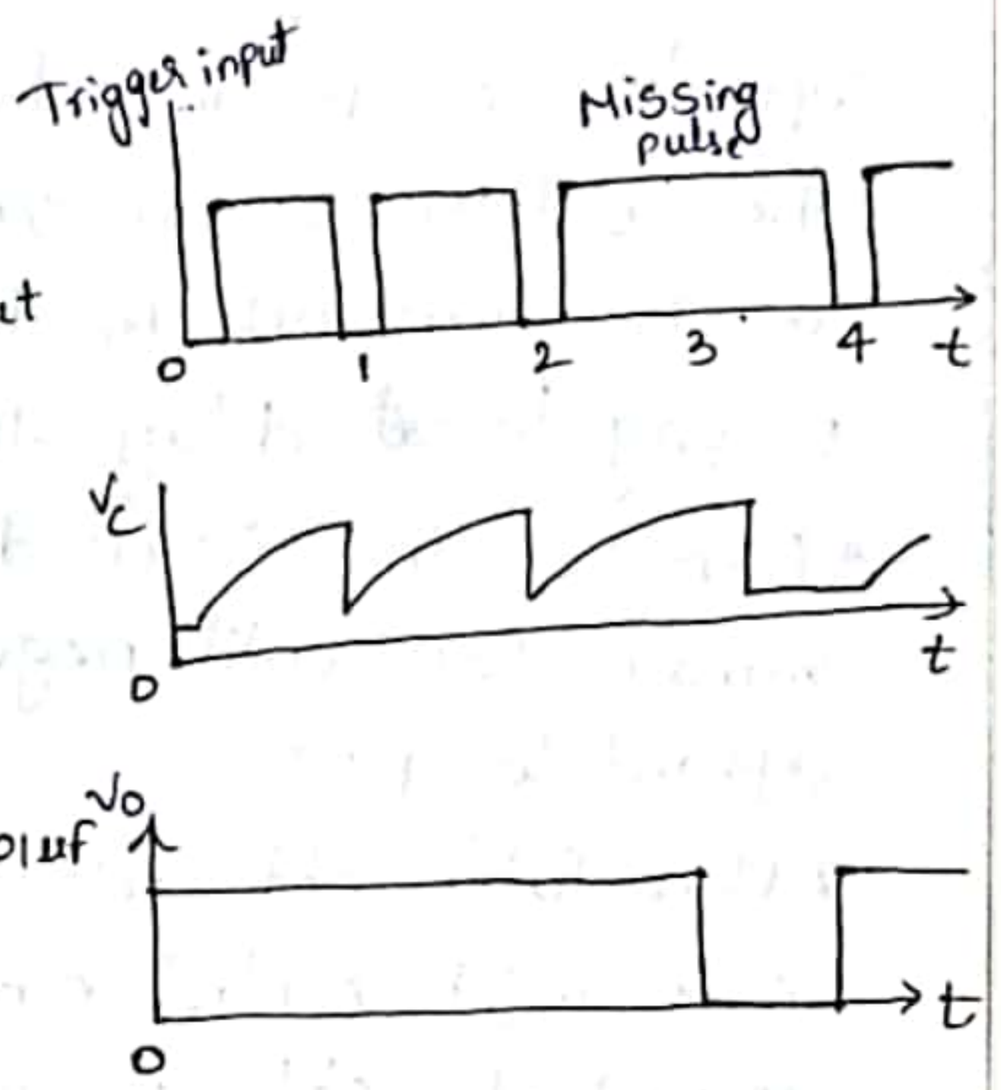
Missing pulse detector.

* The resistor and capacitor combination forms the differentiator ckt. During the positive going edge of trigger, diode D becomes forward biased, thereby limiting amplitude of pulse positive spike to 0.7V.

*Applications in Monostable Mode :-

- Missing pulse Detector :-





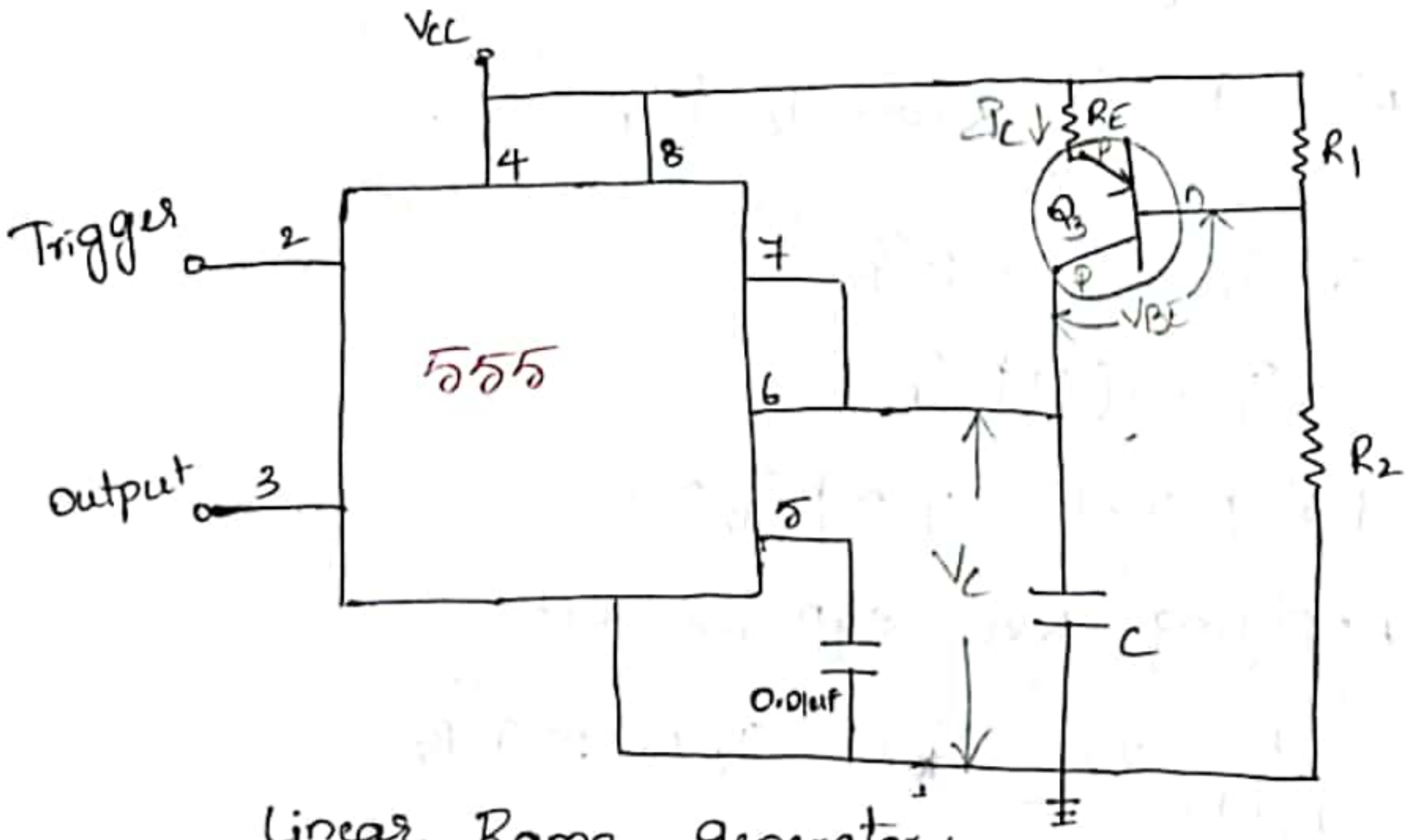
Missing pulse Detector Monostable ckt

output of Missing pulse detector.

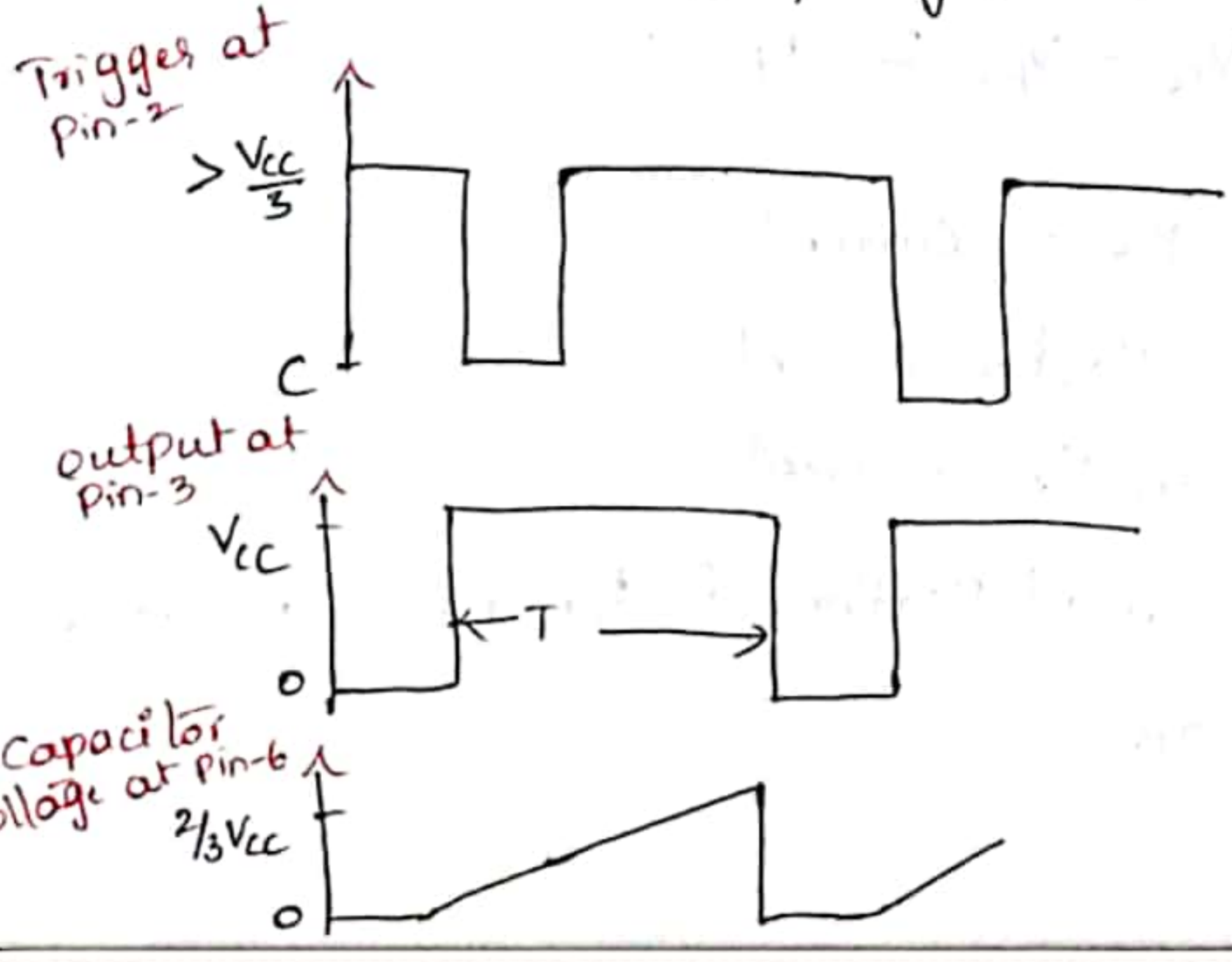
* Whenever, input trigger is low, emitter diode of transistor Q is forward biased. The capacitor C gets clamped to 0.7V. The output of timer goes High.
* The circuit is designed such that the time period of monostable ckt is slightly greater (1/3) than that of triggering pulses.
* As long as trigger pulse train keeps coming at pin 2 the output remains High. If a pulse misses the trigger input is High and transistor Q is cut off [off].

* The 555 timer enters into normal state of Monostable operation. The output goes low after time T of monostable.
* This type of ckt used to detect the missing heartbeat It can also be used for speed control and measurement.
  - PNP → when the base i/p is -ve then Q_1 - ON
  - when trigger i/p high then Q_1 will be in off condition means missing condition
  - whenever trigger i/p goes high the n-type base receives +ve value the Q will be off condition normal operation is resumed back to monostable multivibrator.

* Linear Ramp Generator :-



Linear Ramp generator.



* A linear ramp can be generated using the linear Ramp generator. The Resistor R of the monostable ckt is replaced by constant current source.

* The capacitor voltage v_c is charged linearly by the constant current source formed by transistor Q_3.

→ The capacitor voltage V_c given by

$$V_c = \frac{1}{C}\int_0^t i\,dt \quad \text{— (1)}$$

Where i - current supplied by the constant current source.

$v_c = \alpha t$

$V_c = \frac{1}{C} i \int dt$

$\alpha = \frac{i}{C}$

$V_c = \frac{i}{C} t$

$I_E = I_B + I_C$

Also $\beta = \frac{I_C}{I_B}$ (or) $I_C = \beta I_B$

$\therefore I_E = I_B + \beta I_B$

$I_E = (1+\beta) I_B$.

for $\beta >> 1$, $I_E \simeq \beta I_B \simeq I_C$

Applying KVL Eqn we get

$$\frac{R_1}{R_1+R_2} V_{cc} - V_{BE} = I_E R_E \simeq I_C R_E$$

(or) $$\frac{R_1}{R_1+R_2} V_{cc} - V_{BE} \simeq i R_E$$

where I_B - Base current

I_C - collector current

I_E - Emitter current

β - current amplification factor of CE mode and is very high.

$$i = \frac{R_1 V_{CC} - V_{BE}(R_1+R_2)}{R_E (R_1+R_2)} \quad -(2)$$

Substituting value of current in V_c then

$$V_c = \left[\frac{R_1 V_{CC} - V_{BE}(R_1+R_2)}{C\ R_E (R_1+R_2)} \right] x\ t$$

At time $t=T$ the capacitor voltage V_c becomes $\frac{2}{3}V_{CC}$

then $\frac{2}{3}V_{CC} = \left[\frac{R_1 V_{CC} - V_{BE}(R_1+R_2)}{R_E (R_1+R_2)\ C} \right] x\ T$

Thus the time period of linear ramp generatbr given by

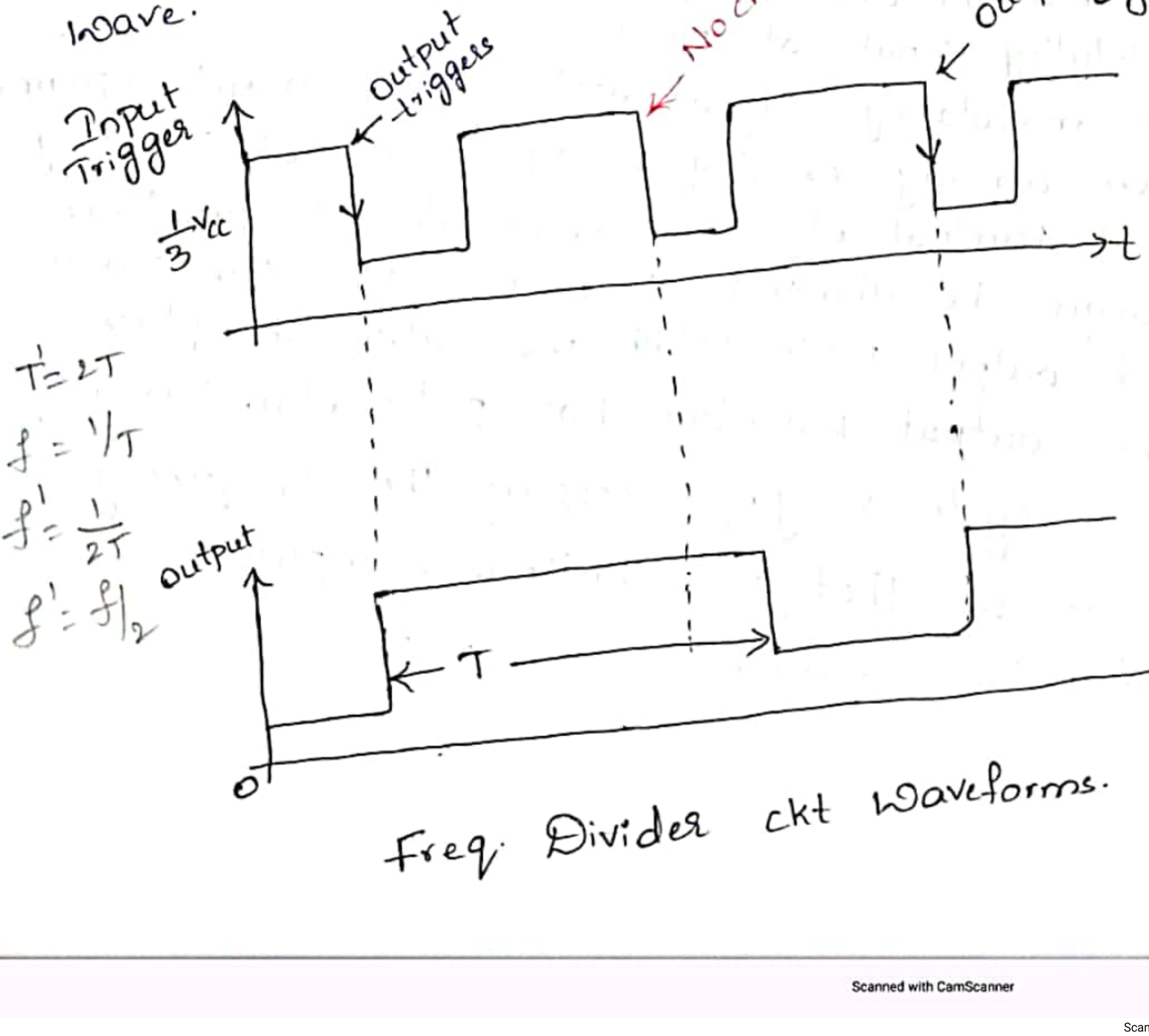
$$T = \left[\frac{\left(\frac{2}{3}V_{CC}\right) R_E (R_1+R_2)\ C}{R_1 V_{CC} - V_{BE}(R_1+R_2)} \right]$$

*The capacitor discharges as soon as its voltage reaches $\frac{2}{3}V_{CC}$ which is threshold of the upper comparator in monostable ckt functional diagrams. The capacitor voltage remains zero until another trigger pulse is applied.

* Frequency Divider :-

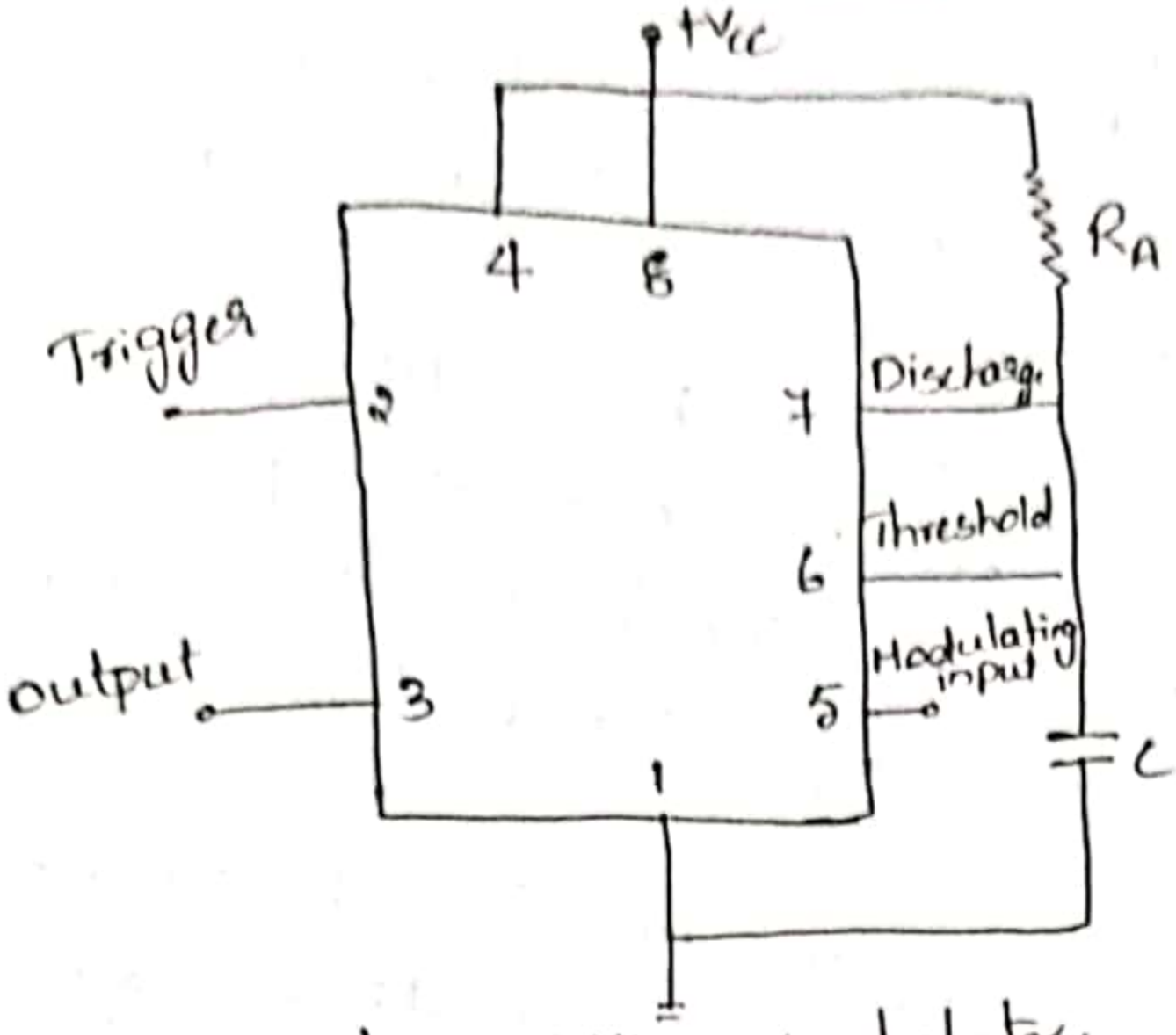
* A continuously triggered monostable ckt when triggered by square wave generator can be used as frequency divider if timing interval is adjusted to be longer than the period of the triggering square-wave input signal.
* The monostable Multivibrator will be triggered by first negative going edge of square wave input but the output will remain high [due to greater timing interval] for next negative going edge of input square-wave.
* The monoshot will be triggered on the third negative going input, depending on the choice of time delay.

Hence in this way, the output can be made integral functions of frequency of the input trigger square-wave.

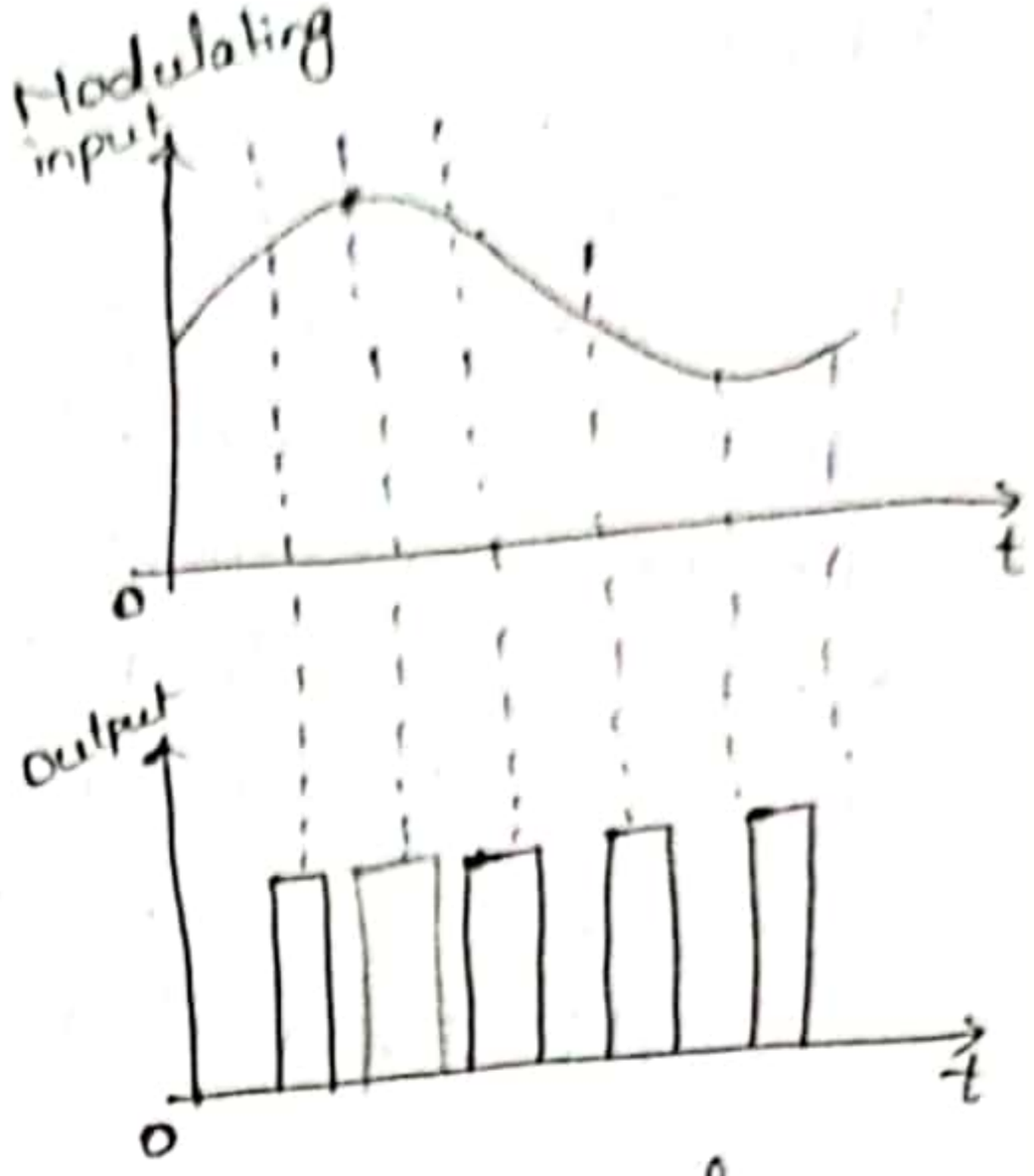


Freq. Divider ckt waveforms.

* Pulse Width Modulation :-



pulse width Modulator.

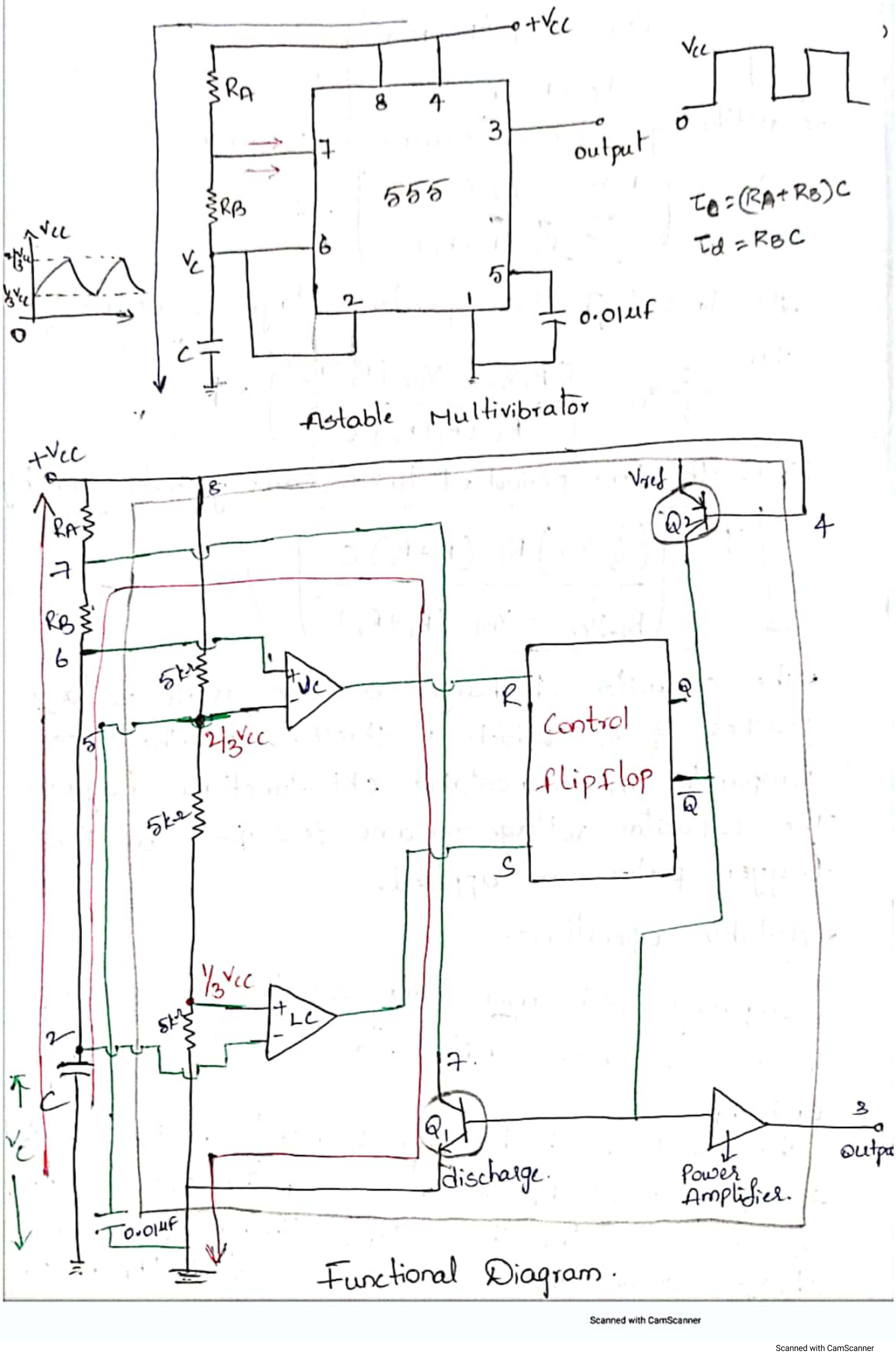


output waveform

*This is basically a monostable multivibrator with modulating input signal applied at pin 5. By application of continuous trigger at pin 2, a series of output pulses are obtained the duration (width) of which depends on modulating input at pin-5.

*The modulating signal applied at pin 5 gets superimposed upon already existing voltage ($\frac{2}{3}V_{cc}$) at inverting input terminal of upper comparator. This in turn changes the threshold level of upper comparator and output pulse width modulation takes place.

*The output waveform has pulse duration as duty cycle varying. keeping the frequency same as that of continuous input pulse-train trigger.



+ The pin-1 of discharging transistor Q_1 is connected to junction of R_A and R_B. When the power supply V_{cc} is connected the external timing capacitor 'C' charges towards V_{cc} with a time constant $(R_A + R_B)C$.

* During this time, output (Pin 3) is high [equal to V_{cc}] as reset $R=0$ and set $S=1$ and this combination makes $\bar{Q}=0$ unclamping the timing capacitor C.

* When capacitor voltage equals [or just greater than] $\frac{2}{3}V_{cc}$ the upper comparator triggers the control flip flop so that $\bar{Q}=1$.

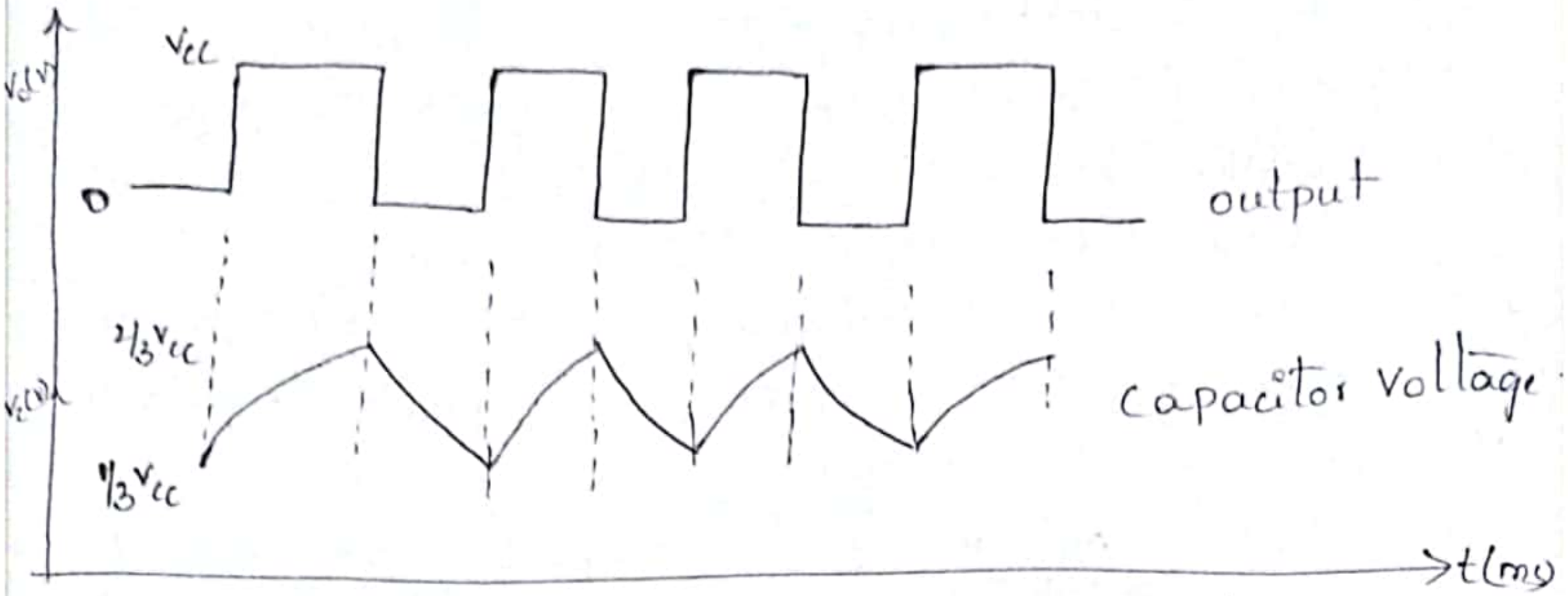
* This in turn makes transistor Q_1 ON and capacitor C starts discharging towards ground through R_B and transistor Q_1 with time constant R_BC. The current also flows into transistor Q_1 through R_A.

* Resistors R_A and R_B must be large enough to limit this current and prevent damage to discharge transistor Q_1.

* During the discharge of timing capacitor C, as it reaches [just less than] $\frac{V_{cc}}{3}$ the lower comparator is triggered and at this stage $S=1$, $R=0$ which turns $\bar{Q}=0$.

* $\bar{Q}=0$ unclamps the external timing capacitor C. The capacitor is periodically charged and discharged between $\frac{2}{3}V_{cc}$ and $\frac{1}{3}V_{cc}$ resp.

* The length of time that output remains High. is the time for capacitor to charge from $1/3\,V_{cc}$ to $2/3\,V_{cc}$.



Timing sequence of Astable Multivibrator.

The capacitor voltage for low pass Rc ckt subjected to step input of V_{cc} is given by

$$V_c = V_{cc}\left[1 - e^{-t/Rc}\right]$$

The time t_1 taken by the ckt to charge from 0 to $\frac{2}{3}V_{cc}$

$$\frac{2}{3}V_{cc} = V_{cc}\left[1 - e^{-t_1/Rc}\right]$$

$$\boxed{t_1 = 1.09RC}$$

The time t_2 taken by the ckt to charge from 0 to $\frac{1}{3}V_{cc}$ is

$$\frac{1}{3}V_{cc} = V_{cc}\left[1 - e^{-t_2/RC}\right]$$

$$\boxed{t_2 = 0.405RC}$$

So time to charge from $\frac{1}{3}V_{cc}$ to $\frac{2}{3}V_{cc}$ is

$$t_{+high} = t_1 - t_2$$

$$= 1.09RC - 0.405RC$$

$$t_{+high} = 0.69RC$$

for given ckt

$$\boxed{t_{+high} = 0.69\left[R_A + R_B\right]C}$$

*The output is low, while the capacitor discharges from $\frac{2}{3}V_{cc}$ to $\frac{1}{3}V_{cc}$ and voltage across the capacitor is given by

$$V_c(t) = V_{cc}\, e^{-t/RC}$$

$$\frac{1}{3}V_{cc} = \frac{2}{3}V_{cc}\, e^{-t/RC}$$

$$t = 0.69RC$$

For given ckt $\boxed{t_{low} = 0.69R_BC}$

Both R_A and R_B are in charge path but only R_B in discharge path.

Total time, $T = t_{High} + t_{low}$

$$T = 0.69(R_A + R_B)C + 0.69R_BC$$

$$T = 0.69(R_A + 2R_B)C.$$

$$\boxed{f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}}$$

The duty cycle is defined as the ratio of ON time to total time period (T). [$T = T_{ON} + T_{off}$]

$$D = \frac{t_{ON}}{t_{ON} + t_{off}}.$$

When transistor Q_1 is ON output goes low.

$$D\% = \frac{t_{low}}{T} \times 100 \quad \Rightarrow D\% = \frac{0.69R_Bf}{0.69(R_A + 2R_B)f} \times 100$$

$$D\% = \frac{R_B}{R_A + 2R_B} \times 100.$$

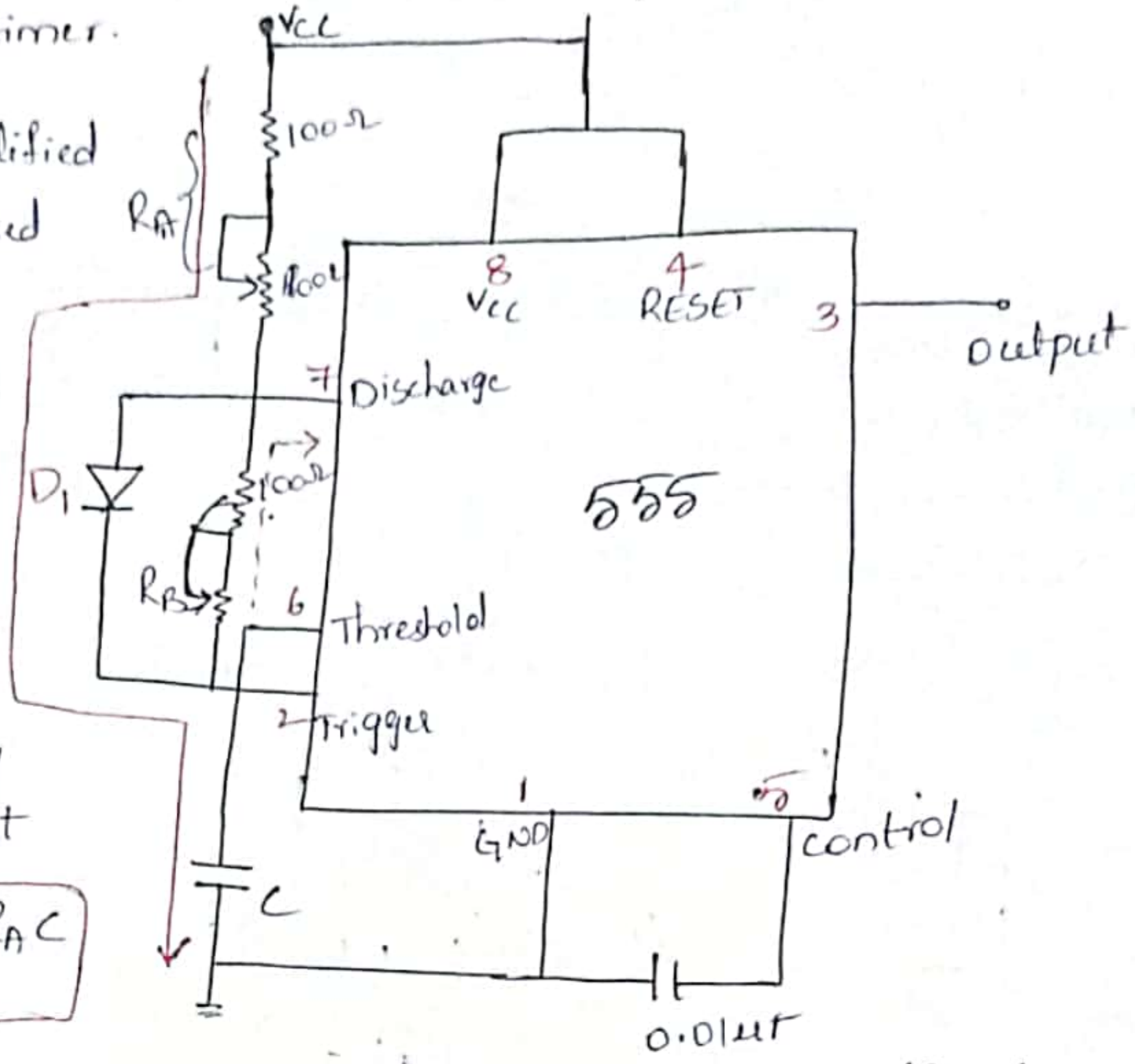
*Hence with existing ckt it is not possible to have duty cycle more than 50% since $t_{High} = 0.69C(R_A + R_B)$ will always be greater than $t_{low} = 0.69R_BC$.

*In order to obtain symmetrical square wave i.e D = 50%. the resistance R_A must be reduced to zero However pin 7 is connected directly to V_{cc} and extra current flows through Q_1 when Q_1 is turned ON. This may damage Q_1 and hence the timer.

*Thus the modified ckt is considered

During the charging portion of cycle, diode D_1 is F.B effectively short circuiting R_B such that

$$t_{High} = 0.69 R_A C$$



Adjustable Duty cycle rectangular wave generator:

*However during the discharging portion of cycle, transistor Q_1 turns ON thereby grounding pin 7 and hence diode D_1 turns RB.

$$t_{low} = 0.69 R_B C$$

$$T = t_{High} + t_{low}$$

$$T = 0.69(R_A + R_B) C$$

$$f = \frac{1}{T} = \frac{1.45}{0.69(R_A + R_B) C}$$

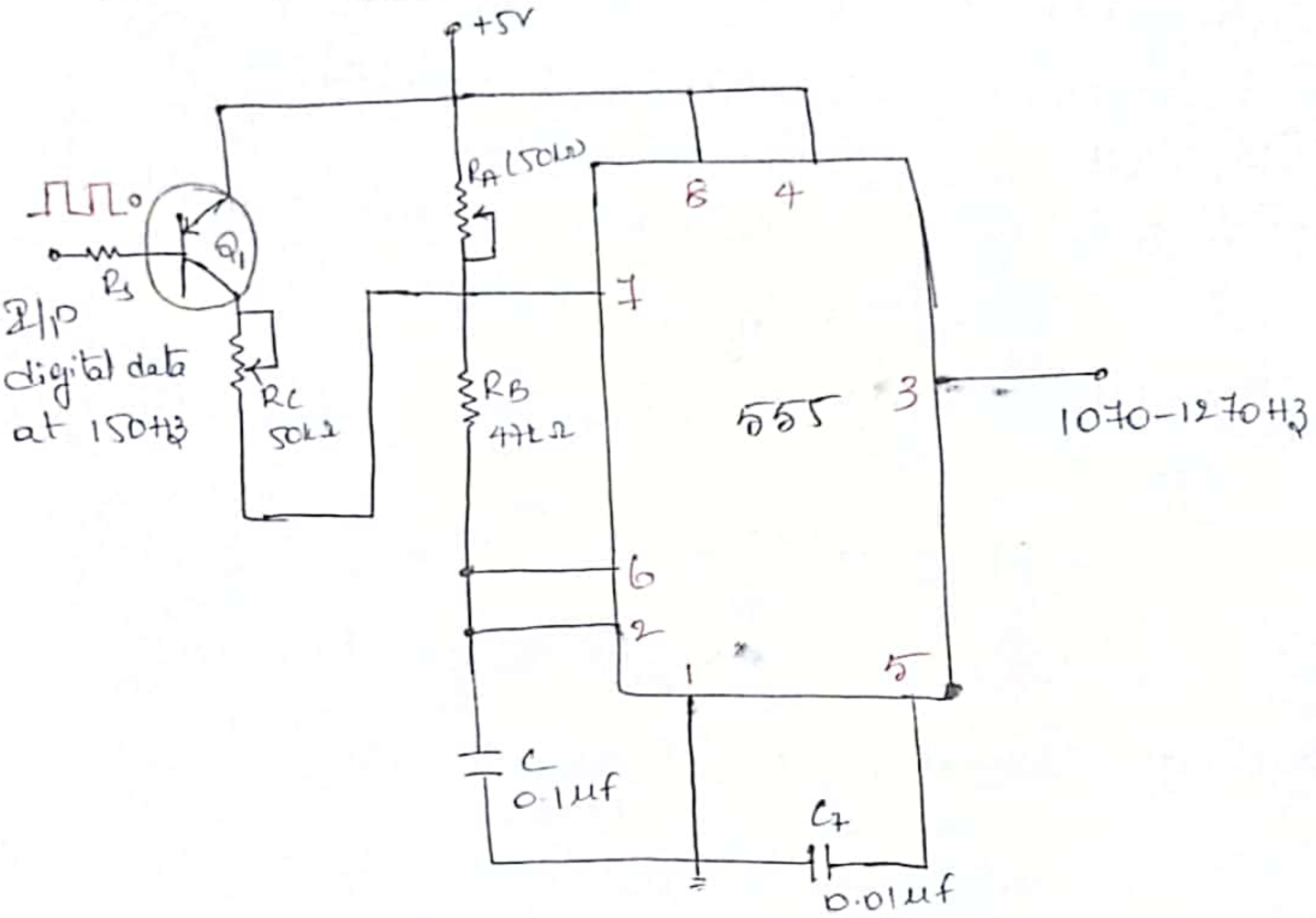
and duty cycle $D = \frac{R_B}{R_A + R_B}$

* Resistors R_A and R_B should be made variable to allow adjustment of freq. and pulse width.
* A series resistor of atleast 100Ω [fixed] must be added to each R_A and R_B this will limit peak current to discharge transistor Q_1 when variable resistors are of min. value.

If $R_A = R_B$ then 50% of duty cycle is achieved

* Applications in Astable Mode :-

i) FSK Generator :-



* In digital data communication binary code is transmitted by shifting carrier freq. b/w two present frequencies this type of transmission is called frequency shift keying (FSK) technique.

* A 555 timer in astable mode can be used to generate fsk signal. The standard digital data input frequency is 150 Hz.
- When input is High, transistor Q is off and 555 timer works in normal astable mode of operation. freq. of o/p waveform given by.

$$f_o = \frac{1.45}{(R_A + 2R_B)C}$$

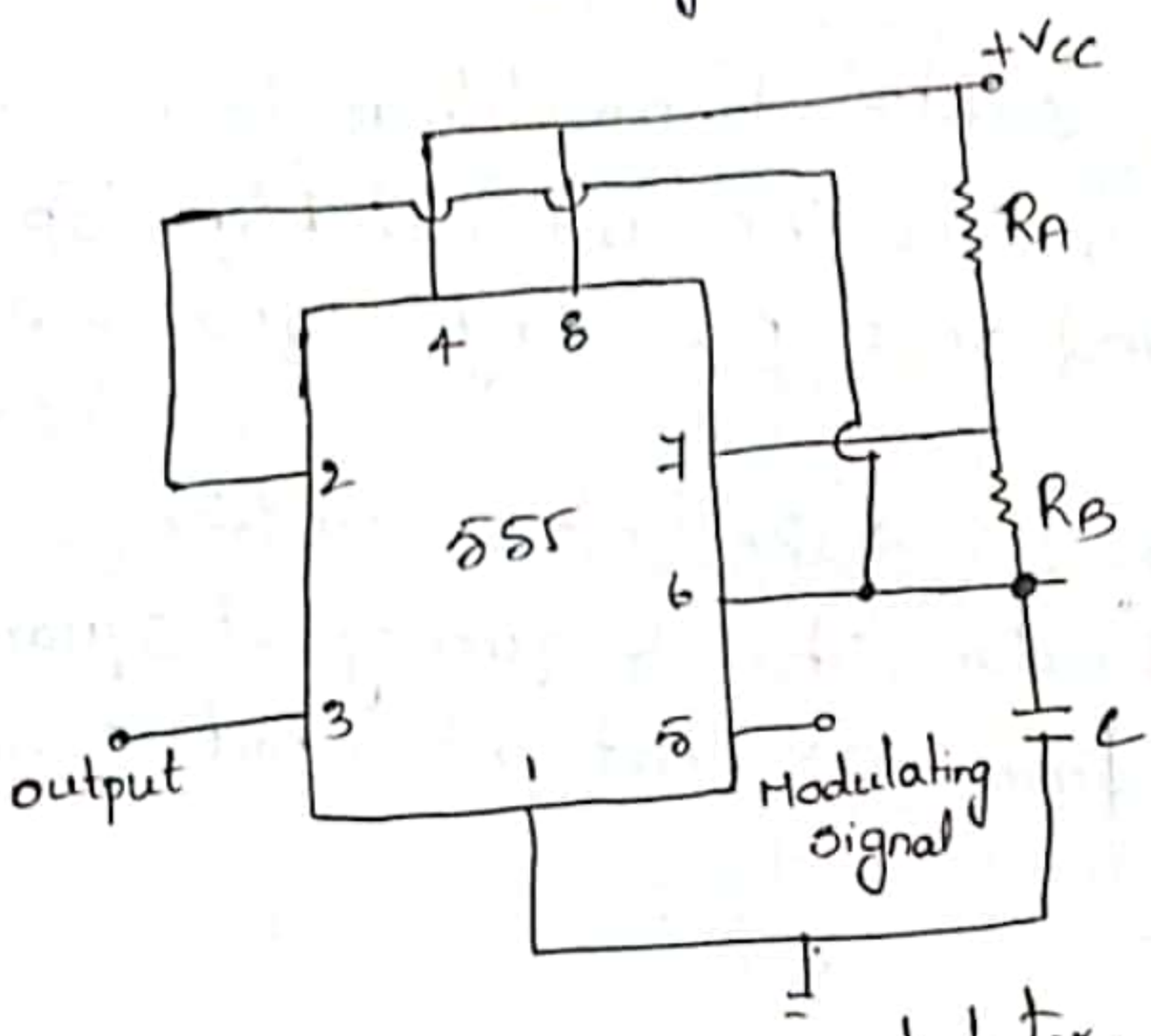
* In tele-typewriter using modular-demodulator [MODEM] freq. b/w 1070 Hz to 1270 Hz is used to as one of standard fsk signals.
The components R_A and R_B & capacitor C is selected such that f_o = 1070 Hz.
* When input is low Q goes ON and connects the resistance R_L across R_A. The output frequency is given by

$$f_o = \frac{1.45}{C[(R_A \| R_L) + 2R_B]}$$

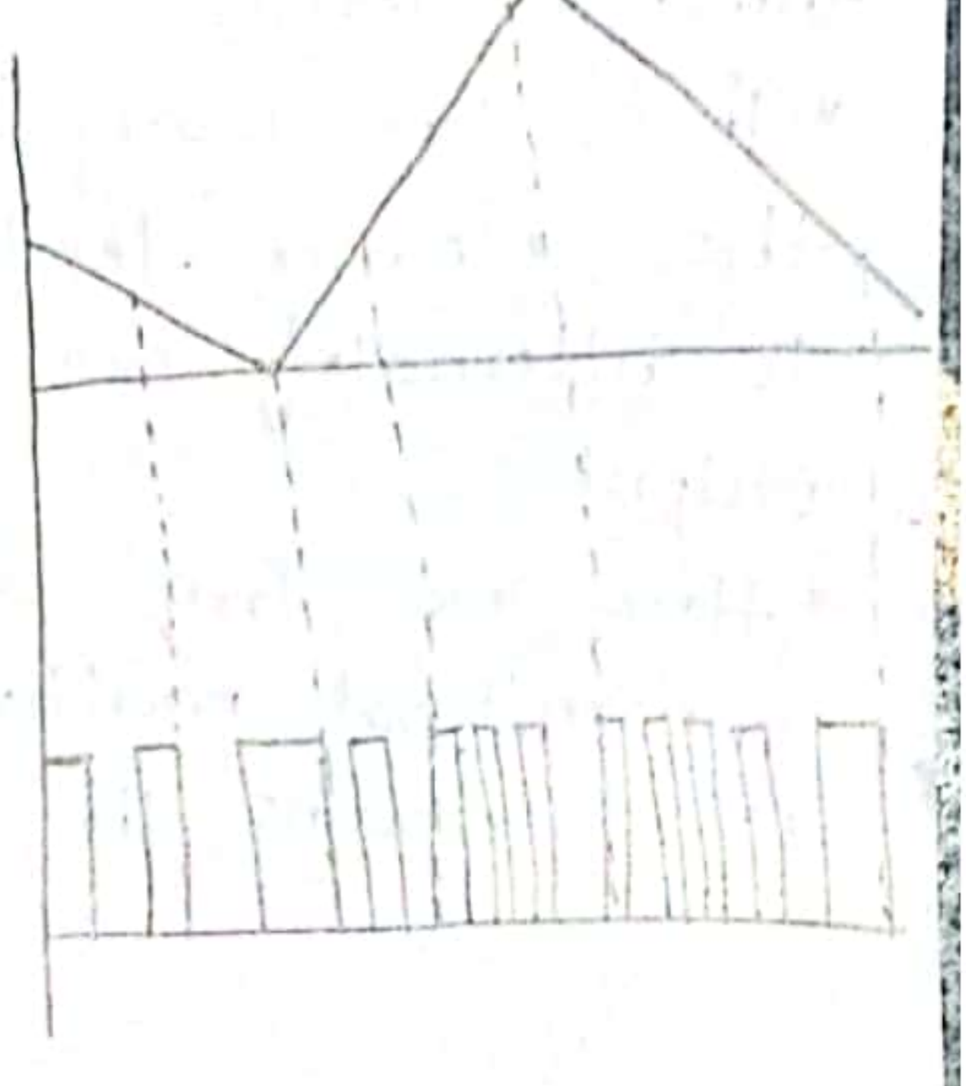
* The resistance, R_L can be adjusted to get an output frequency of 1270 Hz.

(2) Pulse-position Modulator :-

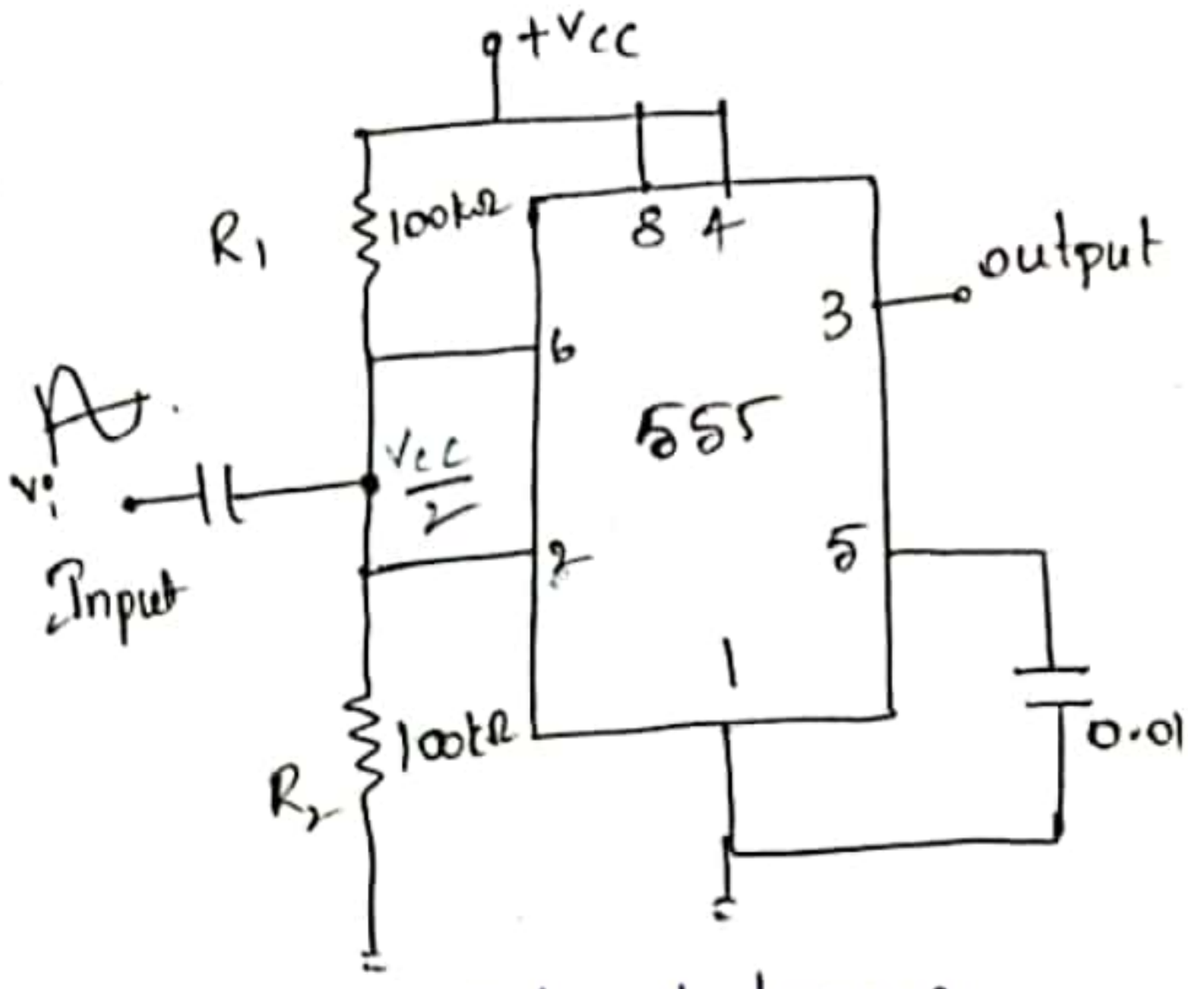
- The pulse position modulator can be constructed by applying a modulating signal to pin 5 of 555 timer connected for Astable Multivibrator.
- The output of pulse position varies with the modulating signal, since the threshold voltage and hence time delay is varied.



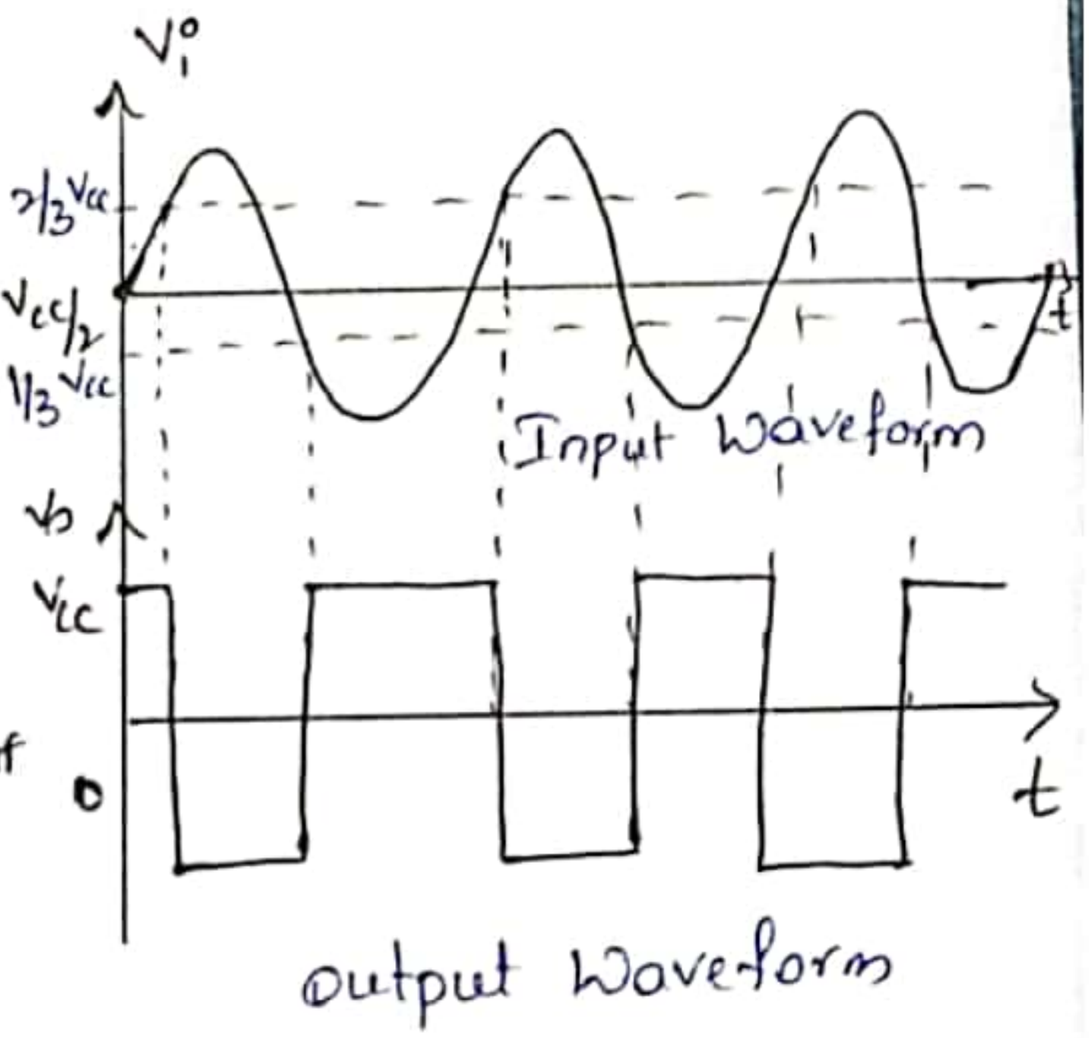
Pulse position Modulator.



* Schmitt Trigger :-



Schmitt trigger.



output Waveform

* A 555 timer can be used as Schmitt Trigger or Squaring circuit.

Here two internal comparators are tied together and externally biased at $V_{cc}/2$ through R_1 & R_2.

* Since the upper comparator will be trip at $\frac{2}{3}V_{cc}$ and lower comparator will trip at $\frac{1}{3}V_{cc}$ the bias provided by R_1 & R_2 is centered within these two threshold levels.

* Thus, sine wave of sufficient amplitude to exceed the reference levels causes the internal flip-flop to alternately set and reset providing square wave output.

* Here no freq. division takes place, unlike conventional multivibrator. The frequency of square wave remains the same as that of input signal.

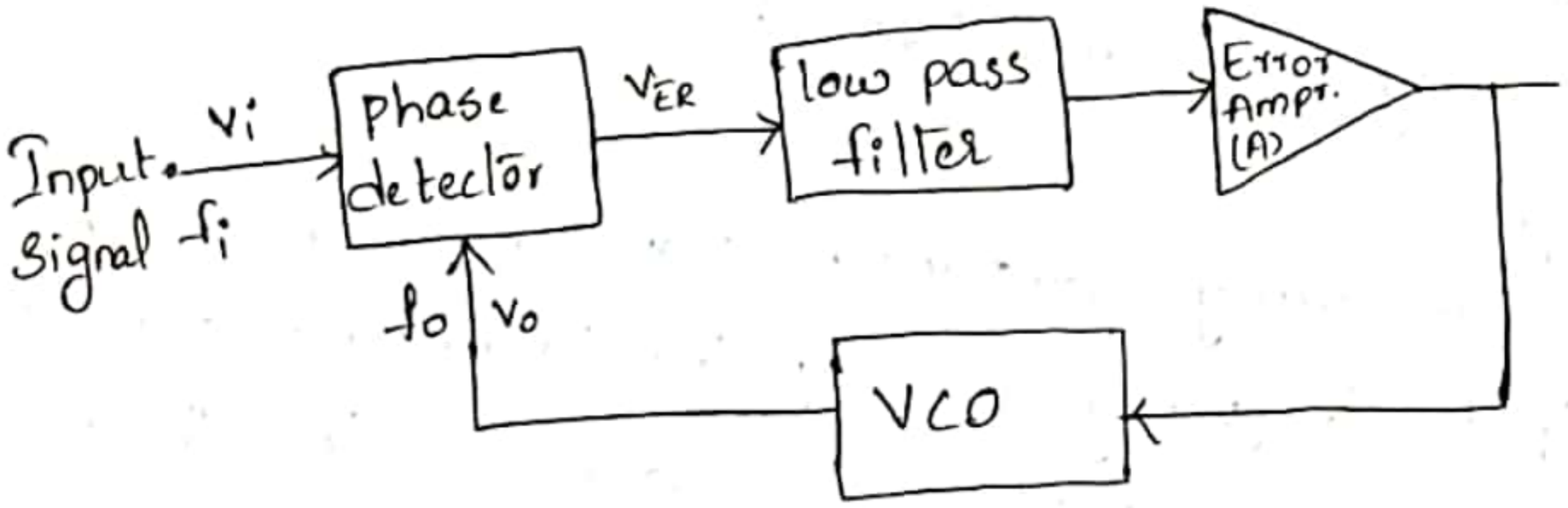
* Phase locked loop :-

- The advancement in the field of integrated circuits, PLL has become one of the main building blocks in the electronics technology.
- The phase locked loop (PLL) is an important building block of linear systems.
- In present, the PLL is available as a single IC in the SE/NE 560 Series [560, 561, 562, 564, 565 and 567]
- The discrete IC's are used to construct a PLL.

* PLL Block Diagram :-

The block diagram of PLL consists of :

(i) Phase detector / Comparator
(ii) Low pass filter.
(iii) Error Amplifier
(iv) Voltage controlled oscillator [VCO].



The input signal V_i with an input frequency f_i is passed through a phase detector. A phase detector basically a comparator which compares the input frequency f_i with the feedback frequency f_o.

*The phase detector provides an output error voltage $V_{ER} = (f_i + f_o)$ which is a DC voltage.

* This Dc voltage is then passed on to an LPF. The LPF removes the high frequency noise and produces a steady Dc level. $V_f (= f_i - f_o)$ V_f also represents the dynamic characteristics of the PLL.
* The Dc level is then passed on to a VCO. The output frequency of the VCO (f_o) is directly proportional to the input signal. Both the input frequency and output frequency are compared and adjusted through feedback loops until the output frequency equals to the input frequency.

- Thus the PLL works in these stages - free running, capture and phase lock.
- The free running stage refers to the stage when there is no input voltage applied.
- As soon as the input frequency is applied the VCO starts to change and begin producing an output frequency for comparison this stage is called capture stage.
- The frequency comparison stops as soon as the output frequency is adjusted to become equal to the input frequency. This stage is called the phase locked state.

i. Lock-in-Range :- once PLL is locked, it can track freq. changes in incoming signals. The range of freq's over which PLL can maintain lock with incoming signal is called lock-in-range or tracking range. It is expressed as percentage of f_o, VCO frequency.

(ii) Capture Range :- The range of freq's over which PLL can acquire lock with an input signal is called Capture range. It is expressed as percentage of f_o.

(iii) Pull in time :- The total time taken by PLL to establish lock is called pull in time. This depends on initial phase and freq. difference blw two signals as well as on overall loop gain and loop filter characteristics.

* Voltage Controlled oscillator (VCO) :-

. The main function of the VCO is to generate an output frequency that is directly proportional to the input voltage.

* VCO is a circuit at which output signal frequency is controlled by the input voltage.

* The frequency of oscillation for the RC oscillator is $f = \frac{1}{2\pi RC}$ $\therefore f \propto \frac{1}{C}$

"If we increase f, C decreases, If f decreases, C increases

The frequency of oscillation for the LC oscillator

$f = \frac{1}{2\pi\sqrt{LC}}$ $\therefore f \propto \frac{1}{C}$

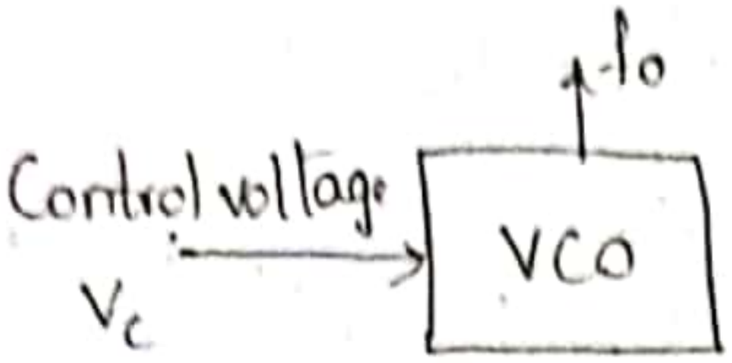
V_{in} (or) $V_c = \frac{1}{C}\int i\,dt$. [$V = \frac{1}{C}\int i\,dt$]

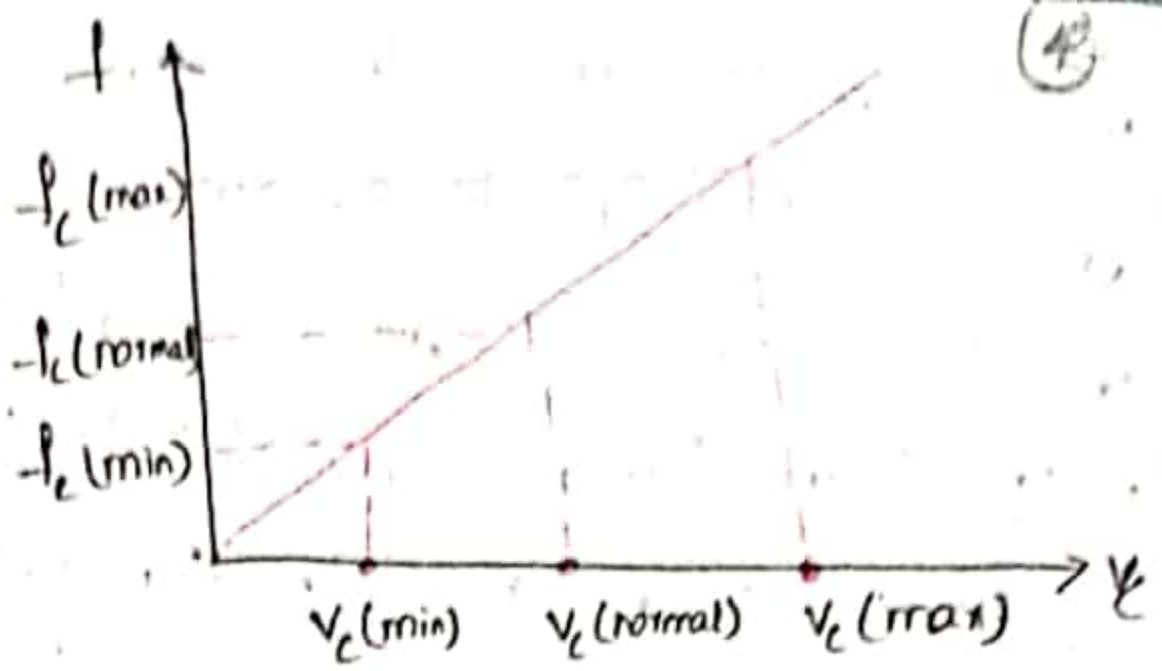
$V_c = \frac{I}{C}\int dt \Rightarrow V_c = \frac{I}{C}t$.

$V_c \propto \frac{1}{C}$. [V_{in} increases C decreases]

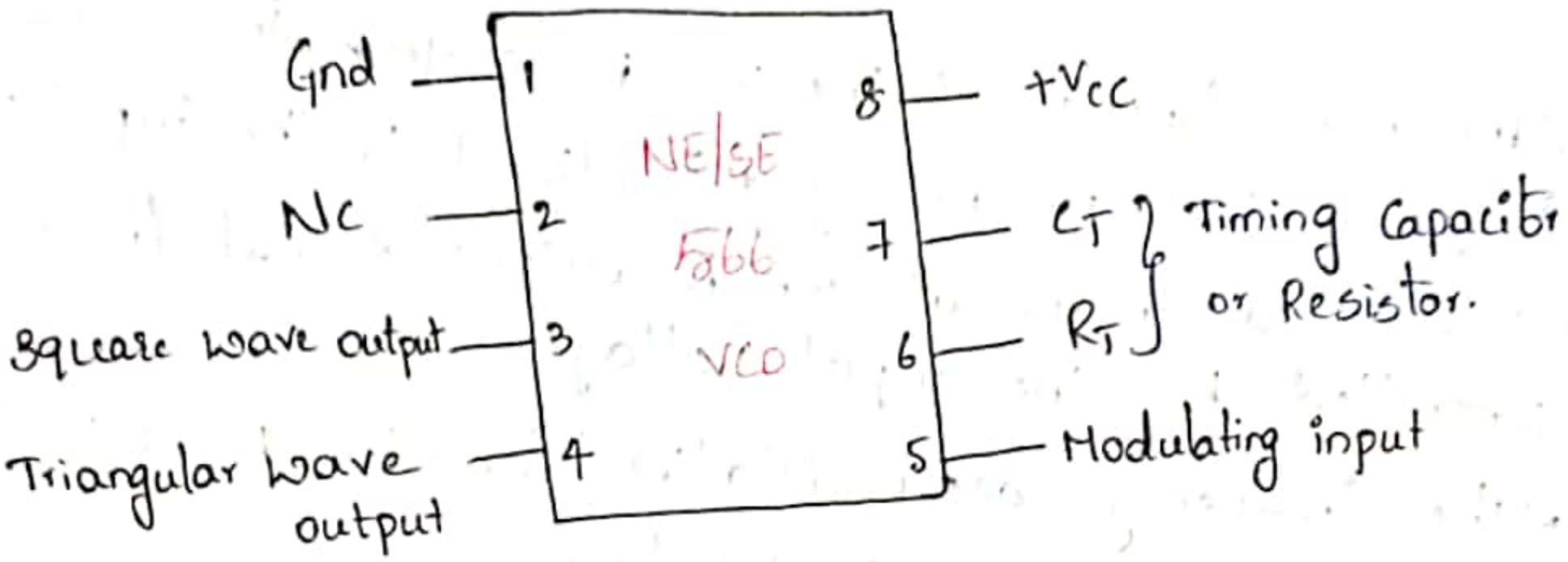
V_{in} (or) $V_c \propto f \propto \frac{1}{C}$.

$\therefore$ Hence the input voltage or control voltage and frequency of oscillation are directly proportional.



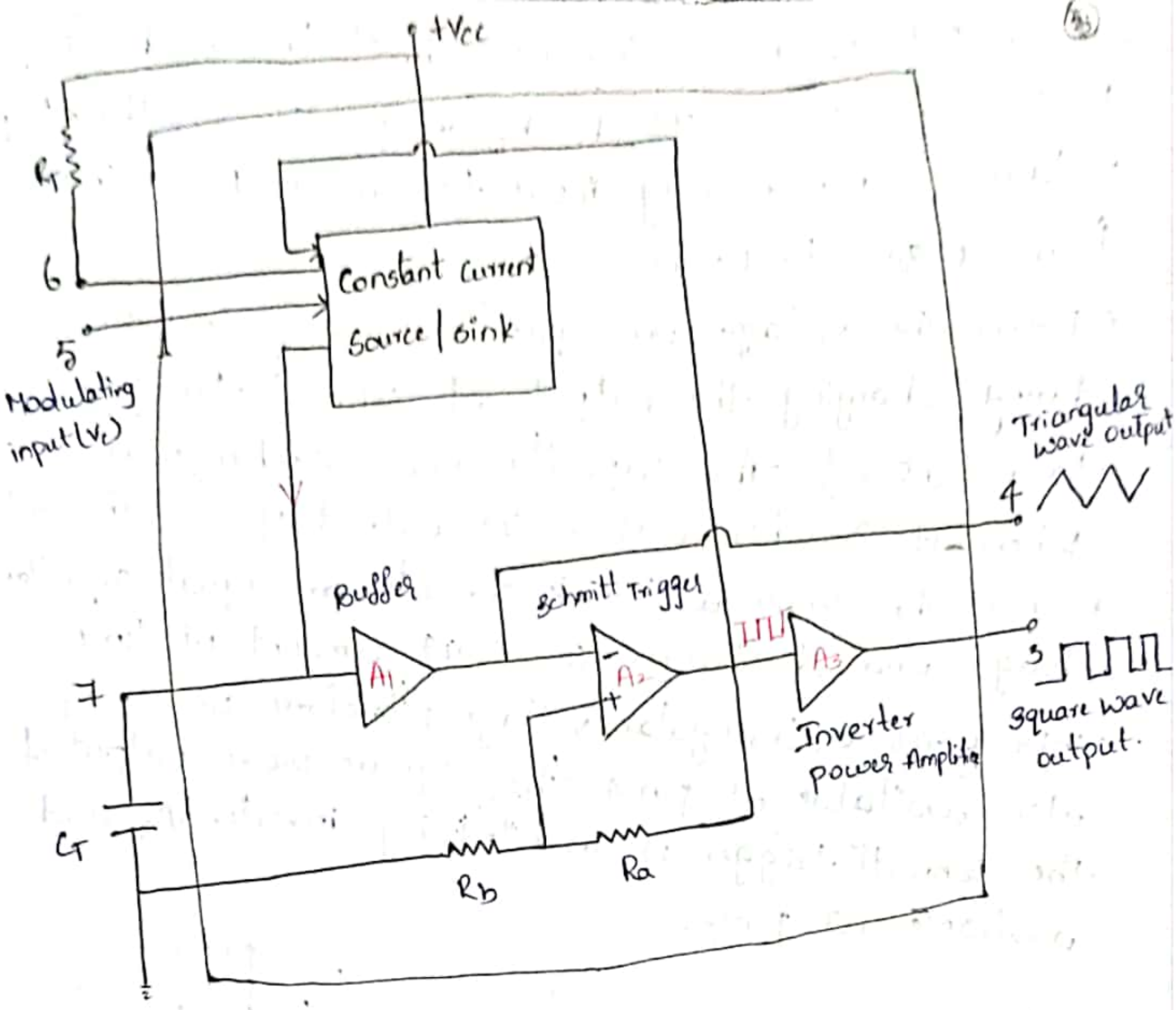


* Pin diagram :-



* VCO provides simultaneous square wave and triangular wave outputs as a function of the input voltage. The frequency of oscillation is determined by the resistor R and capacitor C along with the voltage V_c applied to the control terminal.

- A timing capacitor C_T is linearly charged (or) discharged by constant current source / sink. The amount of current can be controlled by changing the voltage V_c applied at the modulating input (pin 5) (or) by changing the timing resistor R_T external to IC chip.



Block diagram.

* Constant current source/sink will provides the constant current to buffer if they is increase or decreases in the depending on that capacitor charges or discharges.
* Same voltage should be applied to modulating input (V_c) pin 5 and to pin 6.

Then it forms loop. Apply KVL

$$V_{CC} - I R_T - V_c = 0 \Rightarrow V_c = V_{CC} - I R_T .$$

* The voltage across the capacitor C_T is applied to inverting input terminal of schmitH trigger A_2 via buffer amplifier A_1.

* The output voltage swing of schmitt trigger is designed to V_{cc} and $0.5V_{cc}$. If $R_a = R_b$ in positive feedback loop voltage at non-inverting input terminal of A_2 swings from $0.75V_{cc}$ to $0.25V_{cc}$
* When the voltage on capacitor C_T exceeds $0.5V_{cc}$ during charging the output of schmitt trigger goes low [$0.5V_{cc}$]. The capacitor now discharges and when it reaches $0.25V_{cc}$ the output goes high (V_{cc}).
* Since the source and sink currents are equal capacitor charges and discharges for same amount of time. This gives a triangular voltage waveform across C_T also available at pin 4. The square wave output of the schmitt trigger is inverted by inverter A_3 and available at pin 3.

output waveform

Connection Diagram

* Calculation of output frequency :-

The total voltage on capacitor changes from $0.25V_{cc}$ to $0.5V_{cc}$. Thus $\Delta V = 0.25V_{cc}$ [$\Delta V_c = V_2 - V_1 = 0.5 - 0.25 = 0.25V_{cc}$]

- The capacitor charges with constant current source.

$$V_c = \frac{1}{C}\int i\,dt$$

$$C\frac{dV_c}{dt} = i \Rightarrow \frac{i}{C} = \frac{dV_c}{dt}$$

$$\frac{\Delta V}{\Delta t} = \frac{i}{C_T} \Rightarrow \frac{0.25V_{cc}}{\Delta T} = \frac{i}{C_T}$$

$$\Delta T = \frac{0.25V_{cc}\,C_T}{i}$$

The time period (T) of triangular waveform $T = 2\Delta t$.

frequency of oscillator f_o given by

$$f_o = \frac{1}{T} = \frac{1}{2\Delta T} = \frac{1}{2\left[\frac{0.25V_{cc}\,C_T}{i}\right]}$$

$$f_o = \frac{i}{0.5V_{cc}\,C_T}$$

But $V_{cc} - iR_T - V_C = 0$

$$i = \frac{V_{cc} - V_C}{R}$$

$$f_o = \frac{V_{cc} - V_C}{0.5V_{cc}\,C_T R_T}$$

$$\boxed{f_o = \frac{2[V_{cc} - V_C]}{V_{cc}\,C_T R_T}}$$

* The output frequency of VCO can be charged either by changing (i) R_T (ii) C_T or (iii) voltage V_c at modulating input terminal pin 5. The voltage V_c can be varied by connecting R_1, R_2 ckt.

* Phase Detector / Comparator :-

The phase detection is most important part of PLL system. There are two types of phase detectors used - Analog and digital detectors.

(i) Analog phase Detector :-

The principle of analog phase detection uses switch type phase detector. An electronic switch 'S' is opened and closed by signal coming from VCO [square wave].

* The input signal is chopped at repetition rate determined by VCO frequency. The input signal V_s assumed to be in phase ($\phi = 0°$) with VCO output V_o.
* Since the switch 'S' is closed only when VCO output is +ve, the output waveform V_e will be half sinusoids. Similarly the output waveform for $\phi = 90°$ and $\phi = 180°$. This type of phase detector is called half wave detector. Since the phase information for only one half of input waveform is detected and averaged.
* The output of phase comparator when filtered through low pass filter gives an error signal which is average value of output waveform. Also the error voltage (V_e) is zero when the phase shift blw two inputs is 90°. Thus for perfect lock, VCO output should be 90° out of phase w.r.t input signal.

Analysis :-

A phase comparator is basically a multiplier which multiplies input signal $[V_s = V_s \sin(2\pi f_s t)]$ by VCO signal $[V_o = V_o \sin[2\pi f_o t + \phi]]$ Thus the phase comparator output.

$$\boxed{V_e = K V_s V_o \sin(2\pi f_s t) \sin(2\pi f_o t + \phi)}$$

where K - phase comparator gain

ϕ - phase shift blw input signal and VCO output

$$V_e = \frac{K V_s V_o}{2} \left[\cos(2\pi f_s t - 2\pi f_o t - \phi) - \cos(2\pi f_s t + 2\pi f_o t + \phi)\right]$$

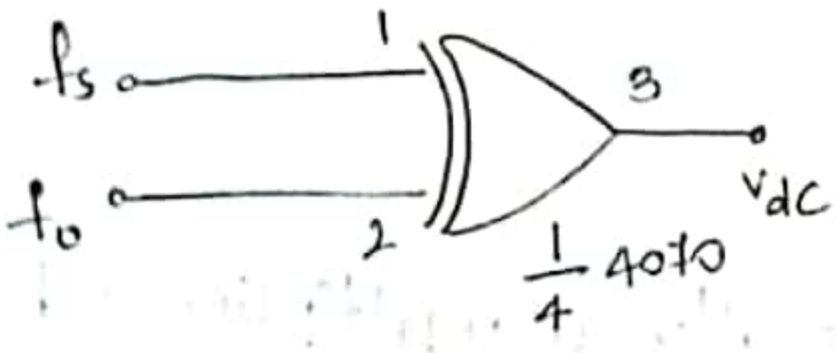
when at lock i.e $\boxed{f_s = f_o}$

$$\boxed{V_e = \frac{K V_s V_o}{2} \left[\cos(-\phi) - \cos(2\pi \times 2 f_o t + \phi)\right]}$$

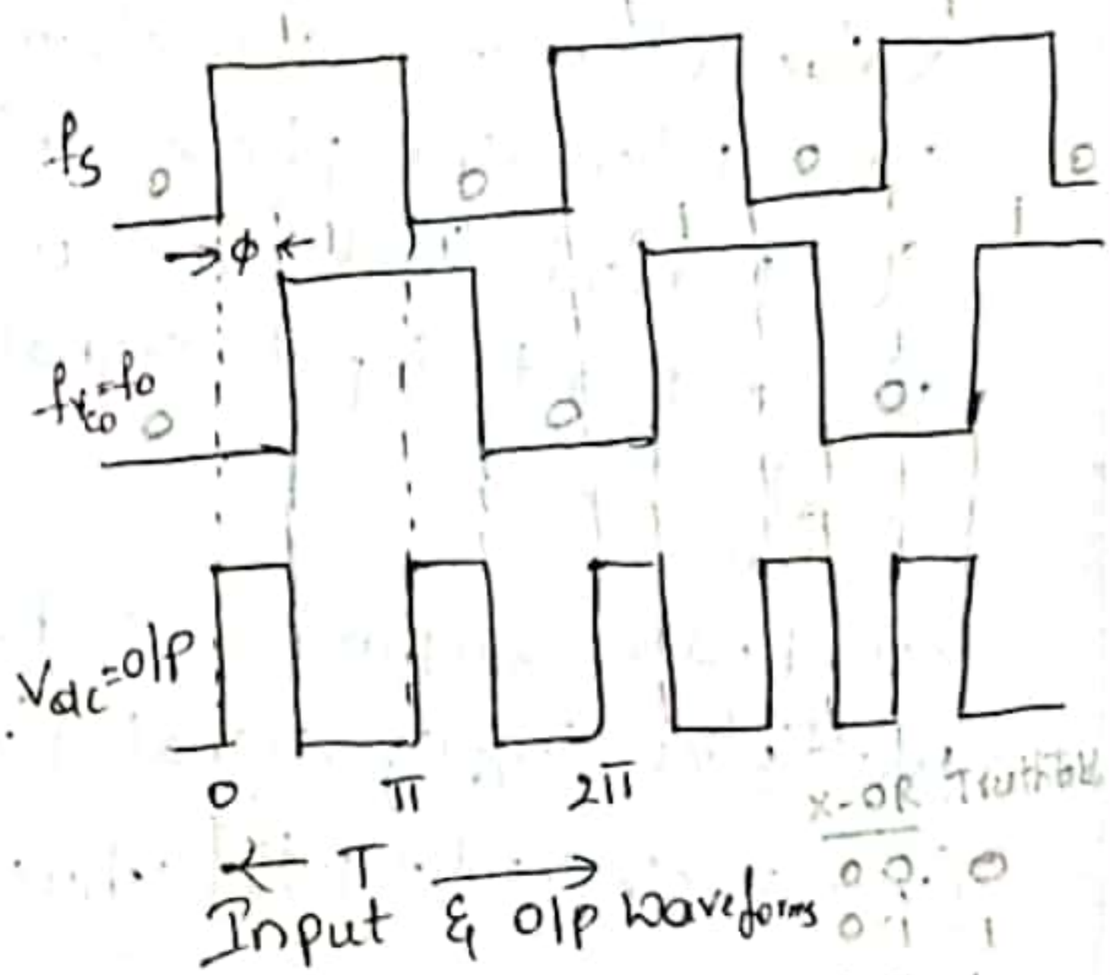
* This shows that phase comparator output contains double frequency term and dc term $\left[\frac{KV_sV_o}{2}\right]\cos\phi$ which varies as function of phase ϕ $[\cos\phi]$
* The double freq. term is eliminated by LPF and dc signal is applied to modulating i/p terminal of VCO
In perfect locked state $[f_s = f_o]$ $\phi = 90°$ $[\cos 90 = 0]$ such that we get zero ϕ error signal $[V_e = 0]$

* Digital Phase Detector :-

It uses CMOS type 4070 Quad 2-input XOR gate. The output of XOR gate is high when only one of input signal $-f_s$ or $-f_o$ is high. This type of detector is used when both input signals are square waves.

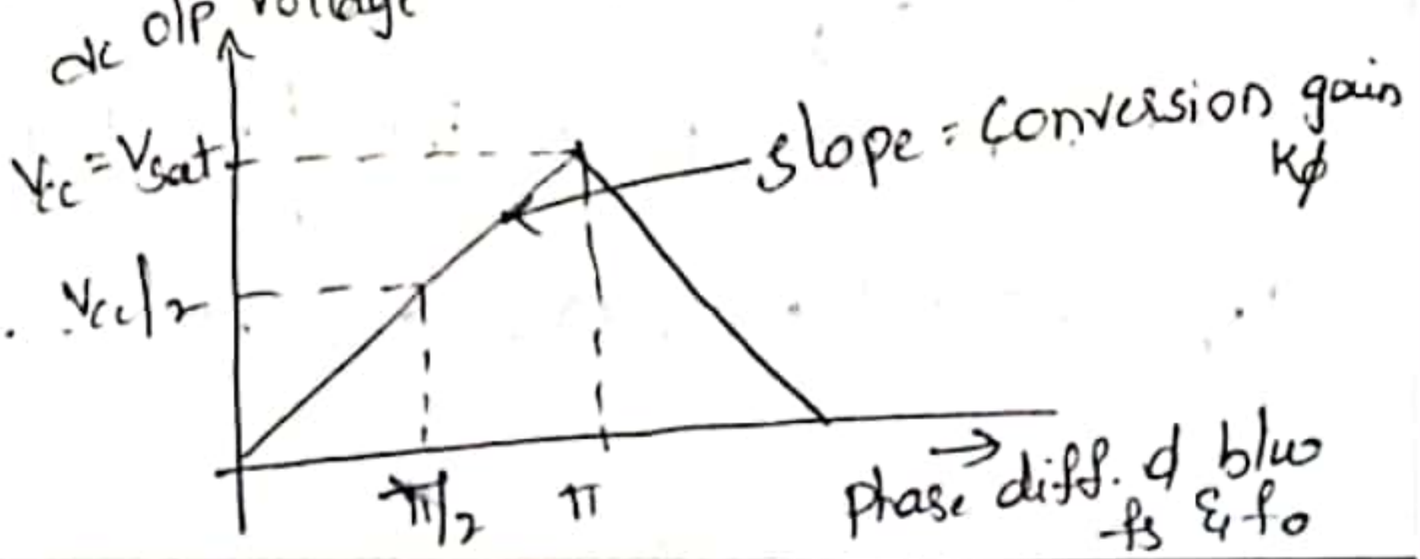


Ex-OR phase detector

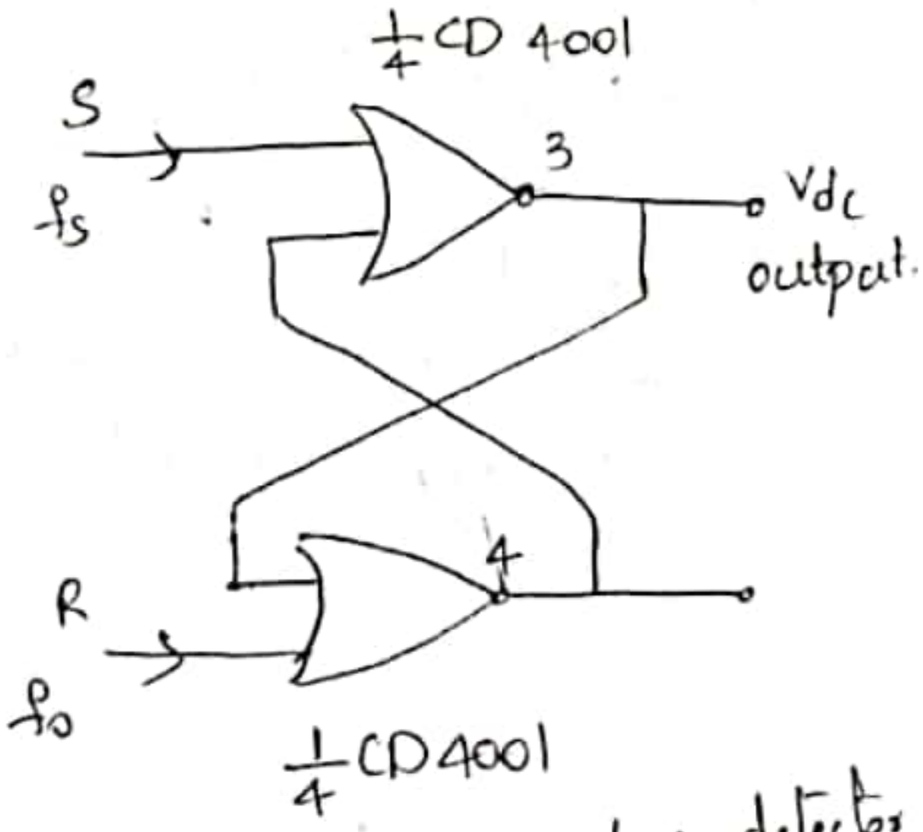


* The maximum dc o/p output voltage occurs when phase difference is π because the o/p of gate remains high throughout.
The slope of curve gives the conversion gain K_ϕ of the phase detector. So the conversion gain K_ϕ for a supply voltage $V_{cc} = 5V$.

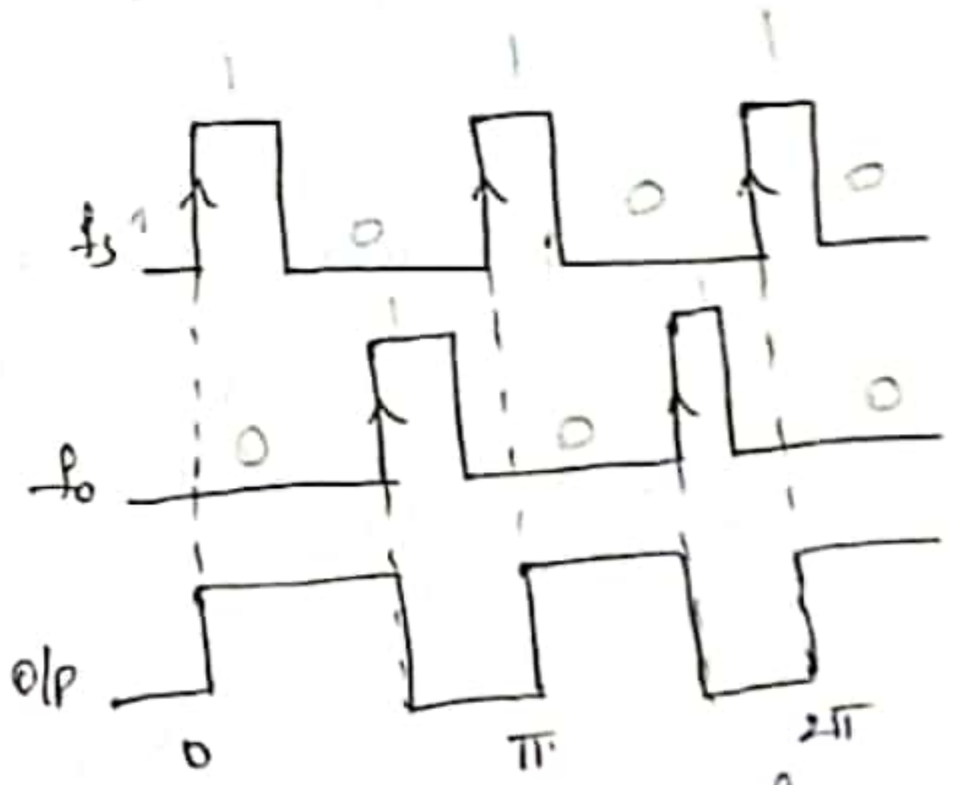
$K_\phi = \frac{5}{\pi} = 1.59\ V/rad.$



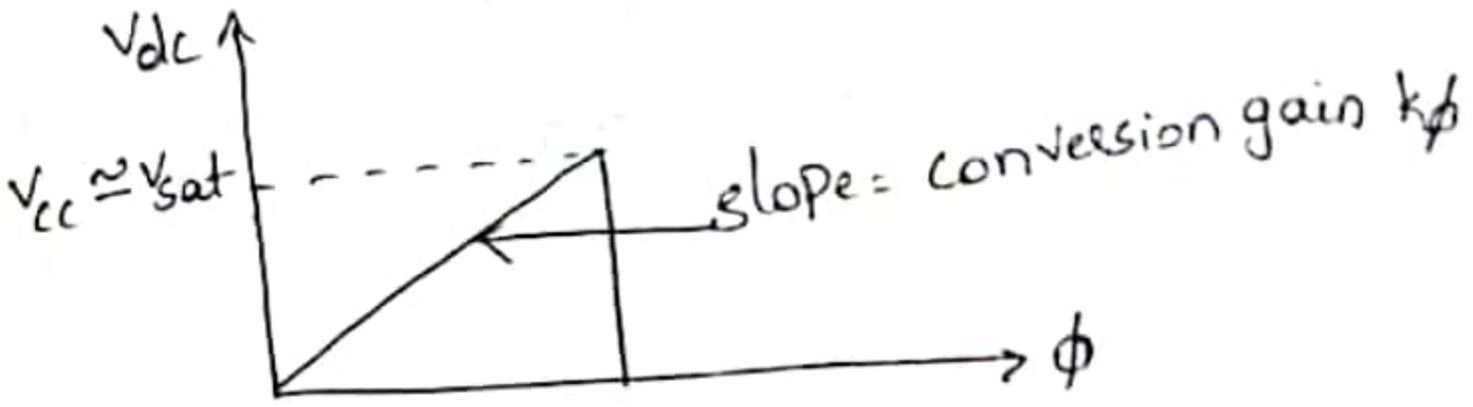
* Another type of phase digital phase detector is an Edge triggered phase detector. The ckt is an R-S flip-flop made by NOR gates [CD 4001]
* This ckt is useful when f_s [incoming signal] and f_o [output signal] of VCO] are both pulse waveform with duty cycle less than 50%.
* The o/p of RS flip-flop changes its state on leading edge of f_s and f_o. The variation of dc output voltage vs phase difference blw f_s & f_o is observed.
* This type of detector has better capture tracking and locking characteristics as dc output voltage is linear upto 360° compared to 180° in case of digital Ex-OR detector.
* This detector is also available in independent Monolithic Ic form. Ex: MC4344/4044. This Ic gives input/output transfer characteristics linear upto 4π rad or 720°.



Edge triggered phase detector



I/p & o/p waveform



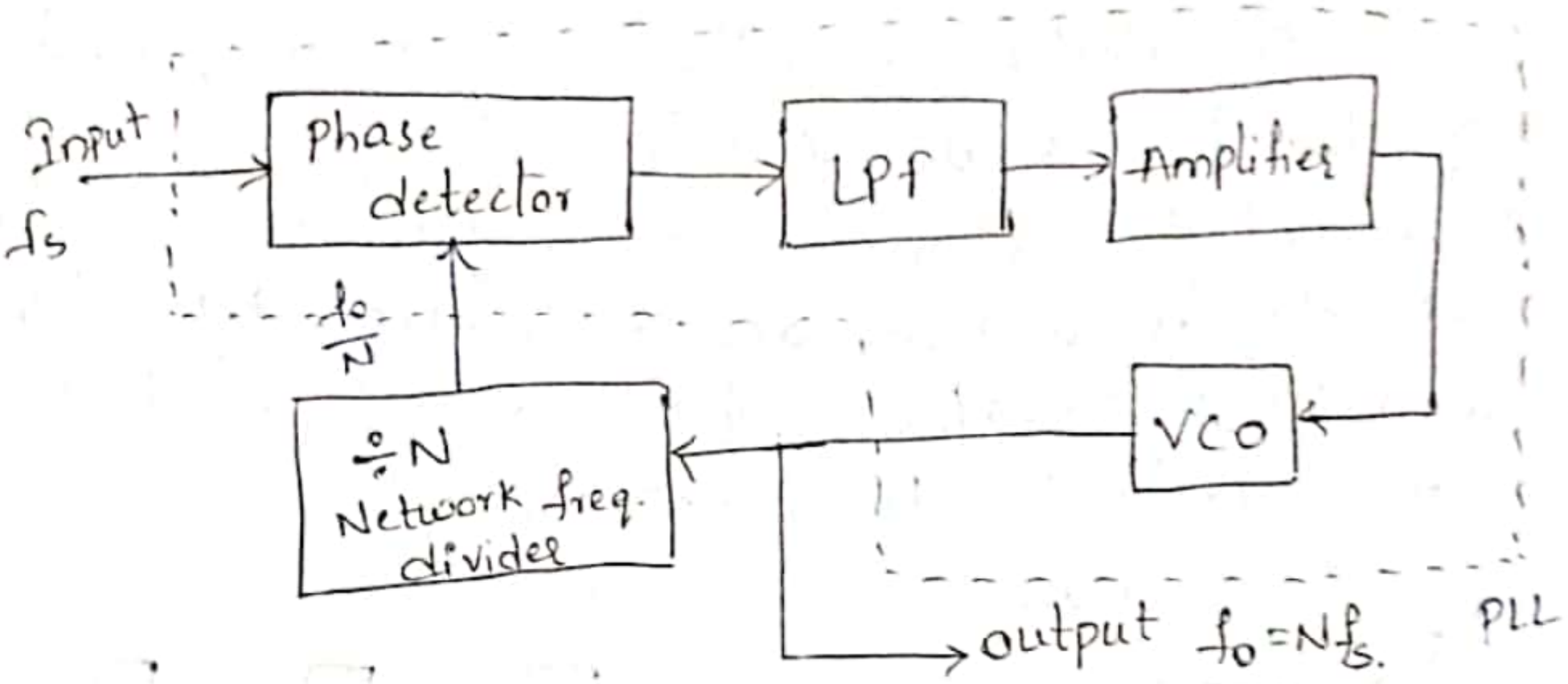
phase diff. blw f_s & f_o.

* Application of PLL :-

The output from PLL system can be obtained either as voltage signal $V_c(t)$ corresponding to error voltage in feedback loop or as frequency signal at VCO output terminal.

* The voltage output is used in freq. discriminator applications while the freq. o/p is used in signal conditioning, freq. synthesis or clk recovery applications.

* Frequency Multiplication / Division :-



Frequency Multiplier using PLL

A divide by 'N network is inserted b/w VCO and phase comparator input. In locked state, VCO output freq. f_o is given by

$$\boxed{f_o = Nf_s}$$

The multiplication factor can be obtained by selecting proper scaling factor N of counter.

* freq. Multiplication can also be obtained by using PLL in its harmonic locking mode. If the input signal is rich in harmonics

Ex: Square wave, pulse train etc. Then VCO can be directly locked to n^{th} harmonic of i/p signal without

connecting any freq. divider in between.

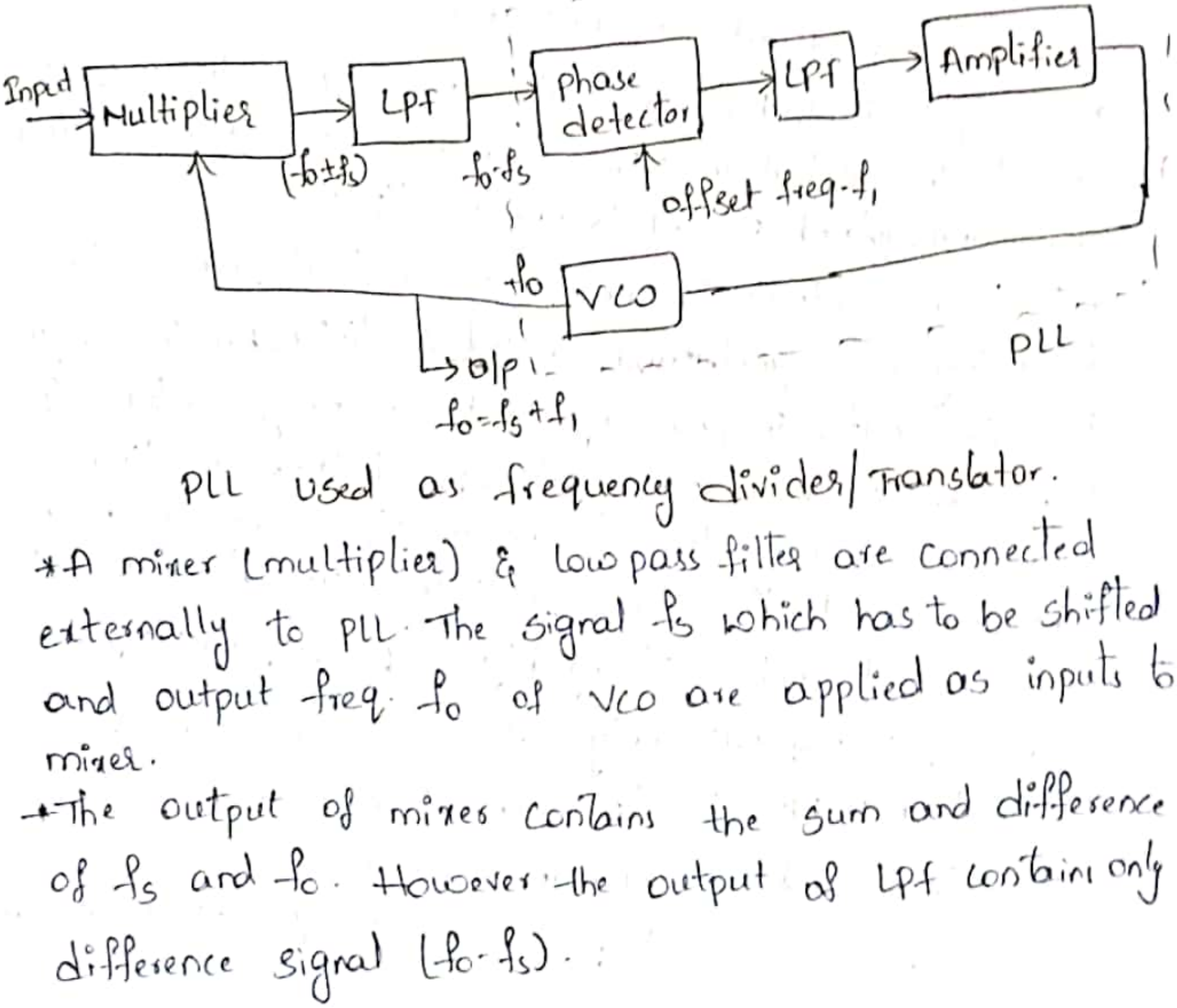
* As amplitude of higher order harmonics becomes less effective locking may not take place for higher values of 'n'. Typically n<10.

* The ckt can be used for freq. division. Since vco o/p [square wave] is rich in harmonics it is possible to lock mth harmonic of vco o/p with I/p signal f_s. The o/p f_o of VCO is given by:

$$f_o = \frac{f_s}{m}$$

* Frequency Translation :-

A schematic for shifting the freq. of an oscillator by small factor.



PLL used as frequency divider/ Translator.

* A mixer (multiplier) & low pass filter are connected externally to PLL. The signal f_s which has to be shifted and output freq. f_o of VCO are applied as inputs to mixer.

* The output of mixer contains the sum and difference of f_s and f_o. However the output of LPF contains only difference signal ($f_o - f_s$).

* The translation (or) offset frequency (f_1 <- f_s) is applied to phase comparator. When PLL is in locked state.

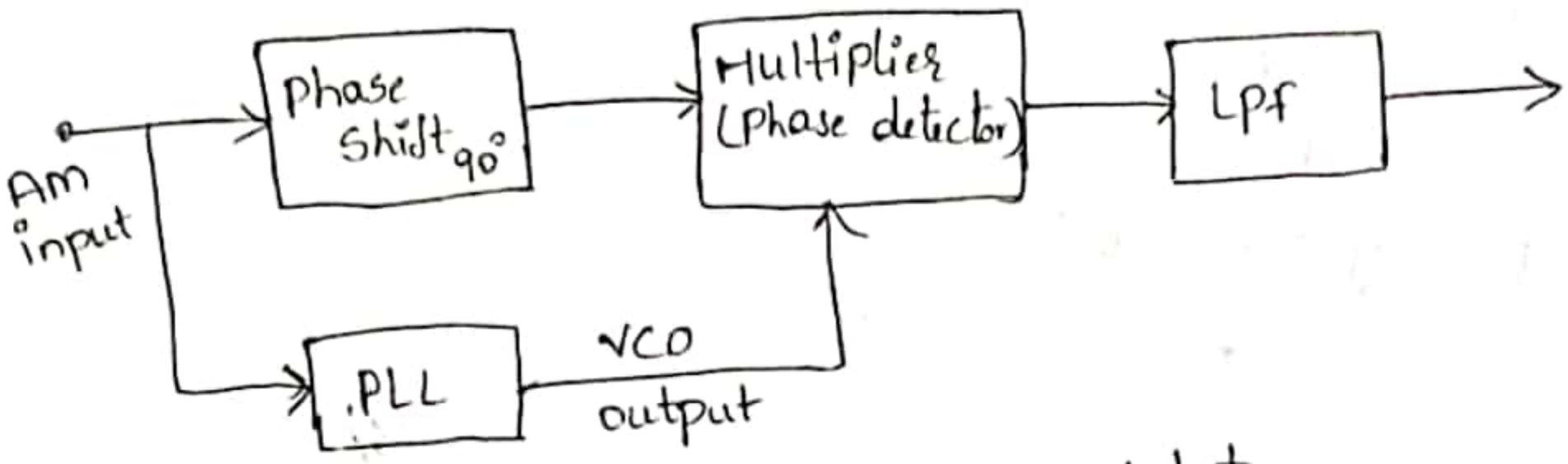
$$f_o - f_s = f_1$$

$$\boxed{f_o = f_s + f_1}$$

It is possible to shift incoming freq. f_s by f_1

(iii) AM Detection:-

A PLL Maybe used to demodulate AM signals.

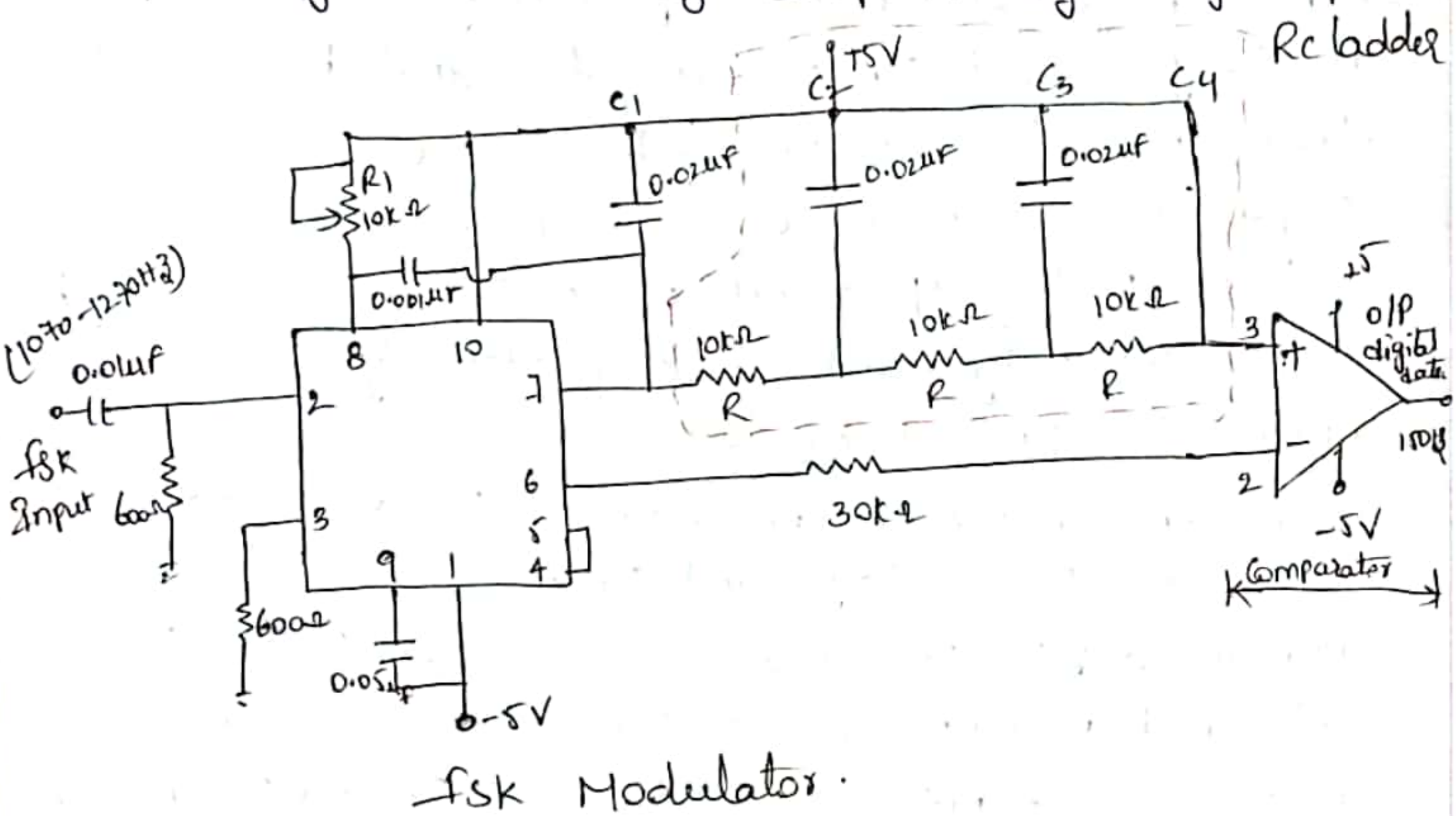


PLL used as AM demodulator.

* The PLL is locked to carrier frequency of incoming AM signal. The output of VCO which has same freq. as carrier but unmodulated is fed to the multiplier.
* Since VCO output is always 90° out of phase with the incoming AM signal under locked condition, AM input signal is also shifted in phase by 90° before being fed to multiplier.
* This makes both the signals applied to the multiplier in same phase. The output of the multiplier contains both the sum and difference signals, the demodulated output is obtained after filtering high freq. components by LPF.
* Since PLL responds only to carrier freq's. close to VCO output, PLL AM detector exhibits high degree of selectivity and noise immunity which is not possible with the Conventional peak detector type AM modulator.

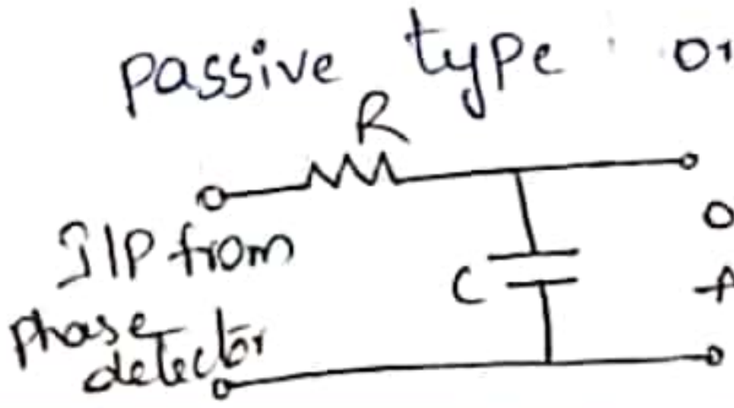
iv) Frequency shift keying [FSK] Demodulator:-

* In digital data communication and computer peripheral, binary data is transmitted by means of carrier frequency which is shifted between two preset frequencies.
* This type of data transmission is called frequency shift keying (FSK) technique. The binary data can be retrieved using FSK demodulator at receiving end. 565 PLL is very useful as FSK demodulator.
* As the signal appears at input, the loop locks to i/p freq. and tracks it between two frequencies with corresp. dc shift at the output.
* A three stage filter removes the carrier component and output signal is made logic compatible by voltage comparator.

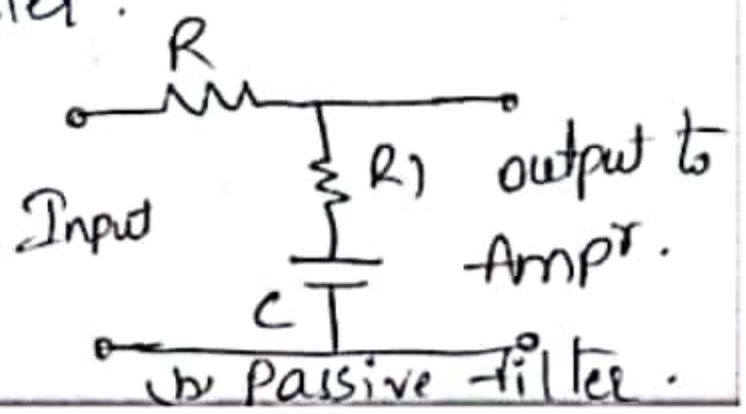


FSK Modulator.

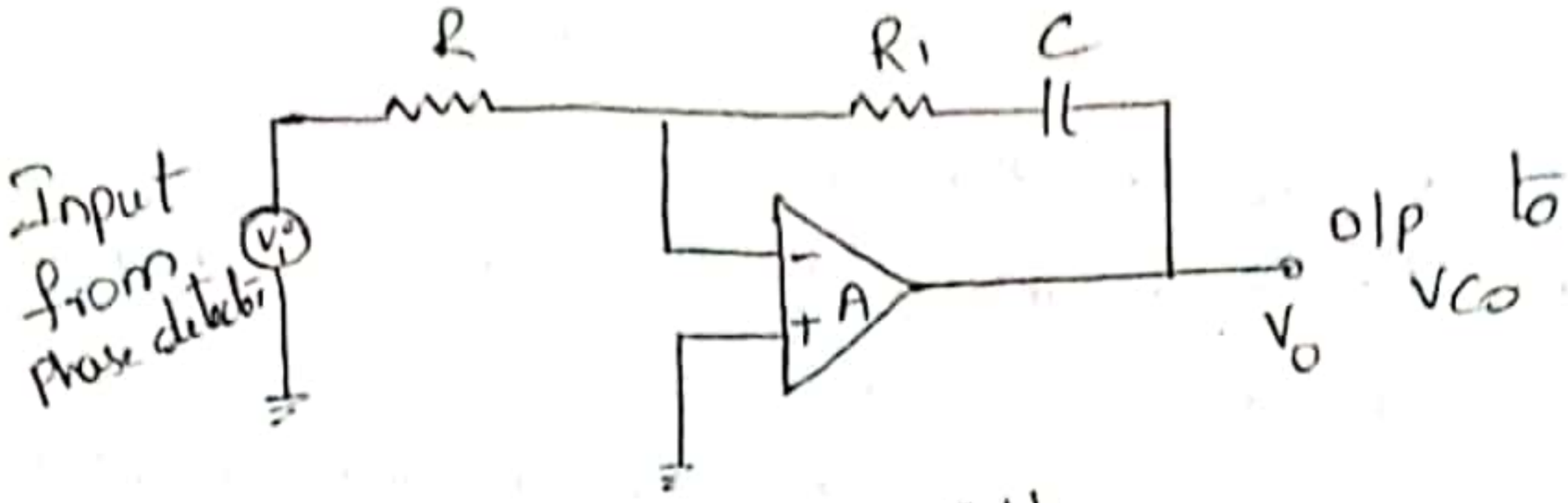
* Low pass filter:- The filter used in PLL may be either passive type or active type of filter.



(a) Low pass filter



(b) Passive filter.



(c) Active filter.

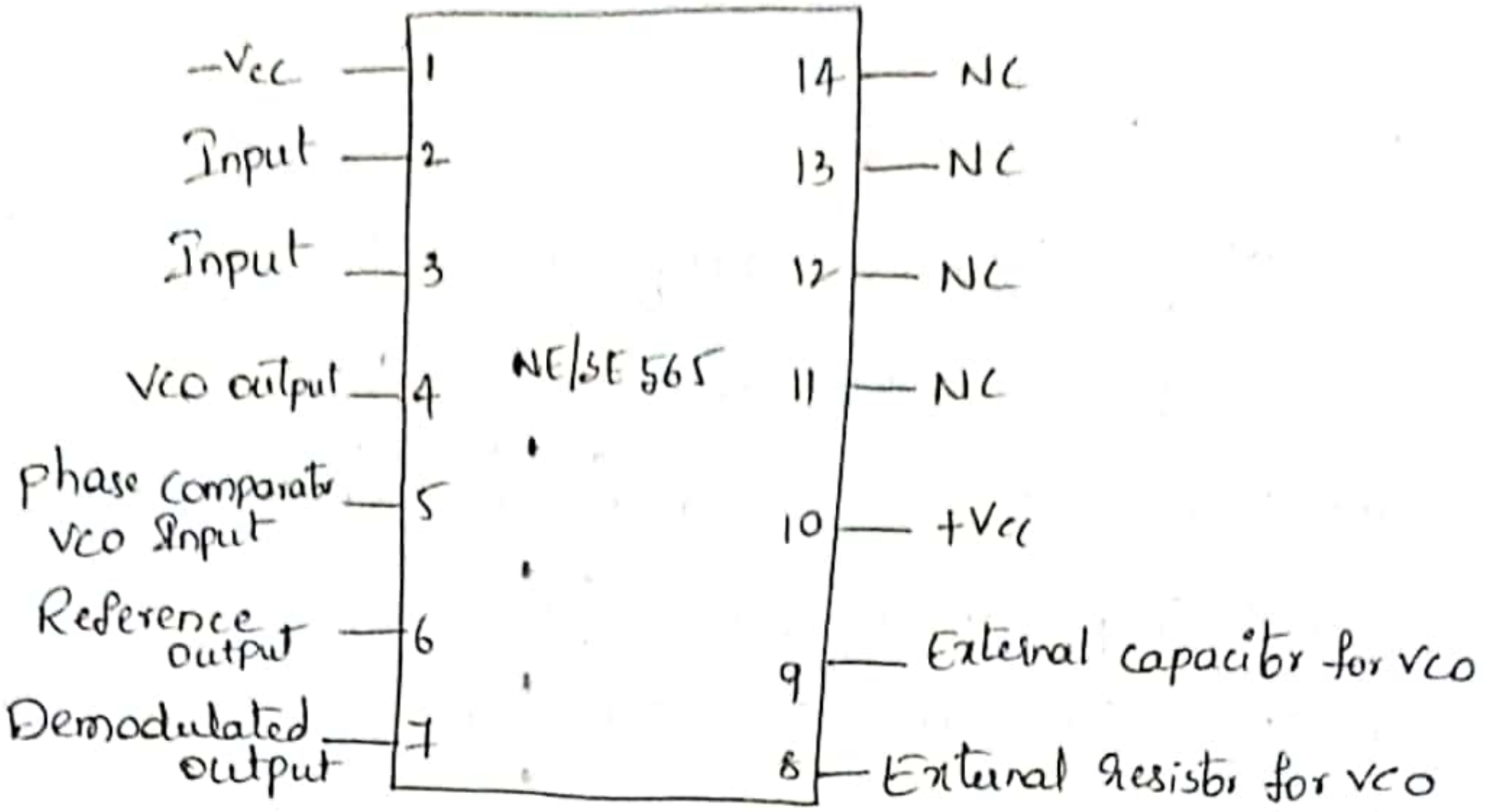
*The low pass filter not only removes the high frequency components and noise, but also controls the dynamic characteristics of PLL. These characteristics include capture and lock range, bandwidth and transient response.

*If filter bandwidth is reduced the response time increases But reducing the bandwidth of the filter also reduces the capture range of the PLL.

*The charge on filter capacitor gives short time memory to PLL. Thus, even if signal becomes less than the noise for few cycles, the dc voltage on capacitor continues to shift the frequency of VCO till it picks up signal again. This produces high noise immunity and locking stability.

* Monolithic phase locked loop:-

All the different building blocks of PLL are available as independent Ic packages and can be externally interconnected to make a PLL. However a number of manufacturers have introduced monolithic PLLs too. Some of the important monolithic PLLs are SE/NE 560, 561, 562, 564, 565 and 567 mainly differ in operating frequency range, power supply requirement, frequency and bandwidth adjustment ranges. Since 565 is the most commonly used PLL.



Pin diagram.

565 is available as a 14-pin DIP package and as 10-pin metal can package. The pin configuration and the block diagram are shown in fig.

The output of frequency of the VCO can be rewritten as

$$f_0 = \frac{0.25}{R_T C_T} \text{ Hz}.$$

* The value of R_T is b/w 2kΩ to 20kΩ. The VCO free running frequency is adjusted with R_T & C_T to be at the centre of the input frequency range.

* The phase locked loop is internally broken b/w the VCO output and the phase comparator input.

* A short circuit b/w pin 4 & 5 connects the VCO o/p to the phase comparator so as to compare f_0 with input signal f_s.

* A capacitor C is connected b/w pin 7 and pin 10 to make a low pass filter with the integral resistance of 3.6kΩ.

Characteristics:

Operating frequency rang: 0.001 Hz to 500 kHz

Operating voltage range: ±6V to ±12V

Input level: 10mV rms min. to 3V pp max.

Input impedance: 10kΩ typical

Output Sink Current: 1mA typical

~~Drift~~

Bandwidth adjustment range: ∠±1 to ± 60%.

Triangular wave amplitude: 2.4 V_{pp} at ±6V supply voltg

Square wave amplitude: 5.4 V_{pp} at ±6V supply voltg.