Code No: **R1641022** **R16** **Set No. 1**

IV B.Tech I Semester Regular/Supplementary Examinations, March - 2021

LINEAR IC APPLICATIONS

(Electrical and Electronics Engineering)

Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any FOUR questions from Part-B
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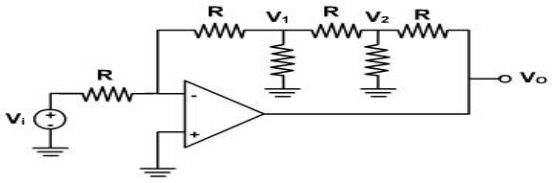
PART–A *(14 Marks)*

1. a) What is meant by D.C Coupling? [2]
   b) Explain the significance of relatively large value of CMRR. [2]
   c) Design an amplifier with a gain of -10 and input resistance equal to 10KΩ. [3]
   d) Give the schematic of Sample and Hold circuit and mention its applications. [3]
   e) PLL act as a frequency translator. Justify? [2]
   f) The digital input for a 4-bit DAC is 0110. Calculate the output voltage? [2]

PART–B *(4x14 = 56 Marks)*

2. a) Derive the expressions for input resistance and output resistance of a single input unbalanced output differential amplifier. [7]
   b) Sketch the circuit diagram of level translator using emitter follower and explain it. [7]

3. a) Find the gain V_O / V_i of the circuit shown in Figure**?** All resistors are equal and Op-Amp is ideal



[7]

   b) Explain the operation of Op-Amp under ideal and practical considerations. [7]

4. a) Derive the expression for closed loop voltage gain, input resistance, output resistance and bandwidth of inverting amplifier. [7]
   b) Illustrate the operation of integrator circuits using Op-Amps with neat sketches. [7]

5. a) Discuss the operation of 2nd order band reject filter along with circuit diagram. [7]
   b) Analyze the operation of four-quadrant multiplier with a neat schematic. [7]

6. a) Design a stable mode circuit having an output frequency of 10kHz with a duty cycle of 25%. [7]
   b) Describe the block diagram of PLL and derive the expression for Lock range and capture range. [7]

7. a) Implement a binary weighted type DAC and explain its operation with a neat circuit diagram. [7]
   b) With the help of circuit diagram, illustrate the operation of parallel comparator type ADC. [7]

Code No:**R1641022** **R16** **Set No. 2**

IV B.Tech I Semester Regular/Supplementary Examinations, March - 2021

LINEAR IC APPLICATIONS

(Electrical and Electronics Engineering)

Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any FOUR questions from Part-B
*****

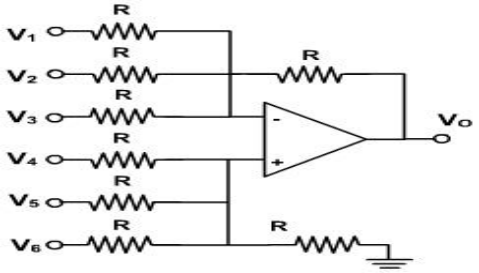
PART–A *(14 Marks)*

1. a) Give the significance of level translator in Op-amp? [2]
   b) Define the input offset voltage and how it can be eliminated. [2]
   c) Design a circuit for $V_0 = 3(V_1 - V_2)$ using op-amp. [3]
   d) Draw and list the applications of all pass filter. [3]
   e) VCO is an important building block in PLL. Justify? [2]
   f) List out the advantages of R-2R Ladder type DAC? [2]

PART–B *(4x14 = 56 Marks)*

2. a) Draw the circuit diagram of differential amplifier with single input and balanced output. Derive expressions for differential gain A_d,input resistance R_i, and output resistance R_o. [7]
   b) Sketch the circuit diagram of differential amplifier in common mode configuration and explain it. [7]

3. a) Find a relationship between V_O and V_1 through V_6 in the circuit of shown Figure. Op-Amp is ideal.



[7]

   b) What is meant by frequency compensation? Explain in detail about pole-zero compensation. [7]

4. a) Illustrate the operation of Instrumentation amplifier using neat diagram and obtain the expression of output voltage. [7]
   b) Design a differentiator that differentiate an input signal with fmax=100Hz. [7]

5. a) Implement the first order high-pass filter using op-amp and explain its operation. [7]
   b) Explain the operation of comparator in inverting mode using wave forms. [7]

6. a) Derive the expression for time period of monostable multi-vibrator using 555 timer with relevant waveforms. [7]
   b) Design a square wave generator of frequency 100 Hz and duty cycle of 75% using 555 timer. [7]

7. a) Analyze the operation of dual slope ADC with a neat schematic. [7]
   b) Discuss about IC 1408 D/A converter. [7]

Code No:**R1641022** **R16** **Set No. 3**

IV B.Tech I Semester Regular/Supplementary Examinations, March - 2021

LINEAR IC APPLICATIONS

(Electrical and Electronics Engineering)

Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any FOUR questions from Part-B

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PART–A *(14 Marks)*

1. a) Write a short note on level translator. [2]
   b) What is frequency compensation? Explain. [2]
   c) Draw the equivalent circuit of an Op-Amp. [2]
   d) Compare differentiator and integrator. [3]
   e) Write the expression for time period of astable multivibrator using a 555 timer. [2]
   f) Evaluate the conversion time of counter type ADC. [3]

PART–B *(4x14 = 56 Marks)*

2. a) Explain the operation of two-stage differential amplifier with a neat diagram. [7]
   b) A BJT differential amplifier is biased from a 1mA constant resistor in each emitter. The collectors are connect to a voltage of 0.1V is applied between the two bases.
   (i) Find the signal current in the emitter
   (ii) What is the total emitter current in each BJT?
   (iii) What is the signal voltage at each collector? Assume α=1
   (iv) What is the voltage gain realized when the output is taken between the two collectors? [7]

3. a) Give the high frequency model of an Op-Amp with single break frequency and analyze the open loop voltage gain as a function of frequency. [7]
   b) What is meant by an integrated circuit? Give the classification of ICs based on number of components integrated on the same chip. [7]

4. a) Draw and explain the operation of precision full-wave rectifier? [7]
   b) Derive the expression for frequency of oscillations for a triangular wave generator with a neat circuit diagram. [7]

5. a) Illustrate the operation of Four-Quadrant multiplier. [7]
   b) With the neat circuit diagram of second order generalized active filter derive the expression for transfer function. [7]

6. a) Describe the important parameters of PLL, which make it suitable for frequency multiplication and division applications? [7]
   b) Explain the operation of FSK generator using 555 Timer. [7]

7. a) Analyze the operation of successive approximation type ADC. [7]
   b) Find out step size and analog output of 4-bit R-2R ladder type DAC when input is 0100 and 1100. Assume Vref= +5V. [7]

Code No:**R1641022** **R16** **Set No. 4**

IV B.Tech I Semester Regular/Supplementary Examinations, March - 2021

LINEAR IC APPLICATIONS

(Electrical and Electronics Engineering)

Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any FOUR questions from Part-B

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PART–A *(14 Marks)*

1. a) What is meant by balanced output and unbalanced output in differential amplifier? [2]
   b) List the ideal characteristics of an Op-Amp. [2]
   c) Define total output offset voltage and thermal drift. [2]
   d) Draw the circuit diagram and frequency response of wide band-pass filter. [3]
   e) What are the basic building blocks of PLL? [2]
   f) How dual slope ADC provides noise rejection. [3]

PART–B *(4x14 = 56 Marks)*

2. a) Draw the circuit diagrams of all four differential amplifier configurations. [7]
   b) Explain the concept of level translator in detail. [7]

3. a) i) A 100 PF capacitor has a maximum charging current of 150 µA. What is the slew rate?
      ii) An operational amplifier has a slew rate of 2 V / µs. If the peak output is 12 V, what is the power bandwidth? [7]
   b) What are the DC characteristics of op amp and describe them briefly. [7]

4. a) Sketch the circuit of Log amplifier and explain its operation and derive the relation between input and output with temperature compensation also. [7]
   b) Design and write the working principle of square wave generator for a frequency of 5KHz and supply voltages of +12V and -12V. [7]

5. a) Explain the operation of Sample & Hold circuit with a neat circuit diagram. [7]
   b) Design and plot the frequency response of a first order high pass filter for pass band gain of 2 and lower cut-off frequency of 1 KHz. [7]

6. a) Illustrate the operation of Schmitt trigger using a 555 timer. [7]
   b) Give the block diagram of IC 566 VCO and explain its operation. [7]

7. a) Evaluate the circuit of R-2R ladder DAC with any two possible combinations and mention the drawbacks of it. [7]
   b) List out the DAC and ADC specifications and compare them in detail. [7]