Code No: R19ES1213 **R19** SET - 1

I B. Tech II Semester Supplementary Examinations, July/August - 2021
DIGITAL LOGIC DESIGN
(Com. to CSE, IT)

Time: 3 hours Max. Marks: 75

Answer any five Questions one Question from Each Unit
All Questions Carry Equal Marks

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1. a) Explain various number systems and codes and their conversion with examples for each. (8M)

   b) Perform the subtraction in binary using 1's and 2's complement methods. (7M)
   (i) $(97)_{10} - (255)_{10}$ (ii) $(1111101)_2 - (100111110)_2$ (iii) $(255)_{10} - (408)_{10}$

Or

2. a) Convert the following: (8M)
   (i) $(53.625)_{10}$ to $(?)_2$ (ii) $(3FD)_{16}$ to $(?)_2$ (iii) $(A69.8)_{16}$ to $(?)_{10}$

   b) With suitable examples discuss the subtraction of two numbers using radix complement and diminished radix complement forms. (7M)

3. a) Simplify the following using K- map and implement the same using NAND gates. (8M)
   $Y(A, B, C) = \sum (0, 2, 4, 5, 6, 7)$

   b) Derive and Implement Exclusive OR function involving three variables using only NAND function. (7M)

Or

4. a) Simplify the following using K- map and implement the same using NOR gate. (8M)
   $Y(A,B,C,D) = \sum (0,2,5,7,8,10,13,15)$

   b) Obtain the simplified expression in product of sums. (7M)
   (i) $F(A,B,C,D) = \pi(0,1,2,3,4,10,11)$
   (ii) $F(A,B,C,D) = \pi(1,3,5,7,13,15)$

5. a) Draw the logic diagram of a 2 to 4 line decoder using NOR gates including an enable input. (8M)

   b) Give circuit implementation of 4 Bit Ripple adder and Ripple Adder/Subtractor using ones and twos complement method. (7M)

Or

6. a) Design a combinational circuit using ROM. The circuit accepts a 3 bit number and generates an O/p binary number equal to square of input number. (8M)

   b) Design and draw the logic circuit diagram for full adder/subtractor. Let us consider a control variable w and the designed circuit that functions as a full adder when w=0, as a full subtractor when w= 1. (7M)

7. a) Design a JK flip flop using AND gates and NOR gates. Explain the operation of the JK flip flop with the help of characteristic table and characteristic equation. Explain the Race around condition and also explain how to eliminate it. (8M)

   b) Draw the circuit diagram of clocked D-flip-flop with NAND gates and explain its operation using truth table. Give its timing diagram. (7M)

Or

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8. a) Draw the schematic circuit of a T flip flop with negative edge triggering using NAND gates. Give its truth table and explain its operation. (8M)

   b) Implement RS-latch using NAND and NOR gates. Explain its operation. (7M)

9. a) With suitable logic diagrams explain about Buffer register and Controlled buffer register. (8M)

   b) Explain the operation of 5-stage twisted ring counter with circuit diagram, state transition diagram and state table. (7M)

Or

10. a) Write the design steps of synchronous counters with suitable examples. (8M)

    b) What is a register? Discuss the applications of shift registers. (7M)