Code No: 138AQ **R16**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech IV Year II Semester Examinations, September - 2020
ANALOG CMOS IC DESIGN
(Electronics and Communication Engineering)

Time: 2 Hours **Max. Marks: 75**

Answer any Five Questions
All Questions Carry Equal Marks
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1.a) How to construct a resistor using MOS transistor?
b) With the help of required expressions explain Sub-threshold MOS Model. [10+5]

2.a) Discuss about current and voltage references and band gap reference in detail with suitable diagrams.
b) Draw the circuit diagram of cascade current mirror. [8+7]

3.a) List different types of inverting CMOS amplifiers and draw any one of it.
b) Draw the High gain amplifier architecture and explain its working. [7+8]

4.a) What is beta helper? How it used in current mirrors?
b) Design a differential amplifier using CMOS transistors and explain its working. [7+8]

5.a) Explain the method of calculation of power supply rejection ratio of two stage Op Amp.
b) What are the advantages of two-stage Op-Amp? [10+5]

6. List various compensation techniques of Op Amps, explain feed forward compensation. [15]

7. Explain the following terms with neat sketch:
a) Switched capacitor comparators.
b) Regenerative comparators. [7+8]

8. Define discrete – time comparators and derive the expression for output voltage of switched capacitor comparator. [15]

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JNTUH USED PAPER Sep-2020