JNTUH USED PAPER SEP-2020

Code No: 138FE **R16**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech IV Year II Semester Examinations, September - 2020
VLSI DESIGN
(Electrical and Electronics Engineering)

Time: 2 Hours **Max. Marks: 75**

Answer any Five Questions
All Questions Carry Equal Marks
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1. With neat sketches explain BICMOS fabrication process in a P well. [15]

2.a) What is the latch up problem that arises in bulk CMOS technology? How is it overcome?
b) Explain the operation of BiCMOS inverter. [8+7]

3.a) Derive the expressions for effective resistance estimation using Elmore's RC delay model
b) Define the principle of constant field scaling and also write its effect on device characterization. [7+8]

4.a) Construct a 4 input pseudo nMOS NAND gates.
b) Classify gates and explain the GaAs growth techniques. [8+7]

5.a) Describe the special features of twin-tube process.
b) Draw and explain the D.C. transfer characteristics of CMOS inverter. [7+8]

6. Design a stick diagram for the full adder. [15]

7. Describe in detail about memory architectures and its building blocks. [15]

8.a) Distinguish between PAL and PLA.
b) Summarize the functions of Programmable Interconnect Points in FPGA. [6+9]

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