

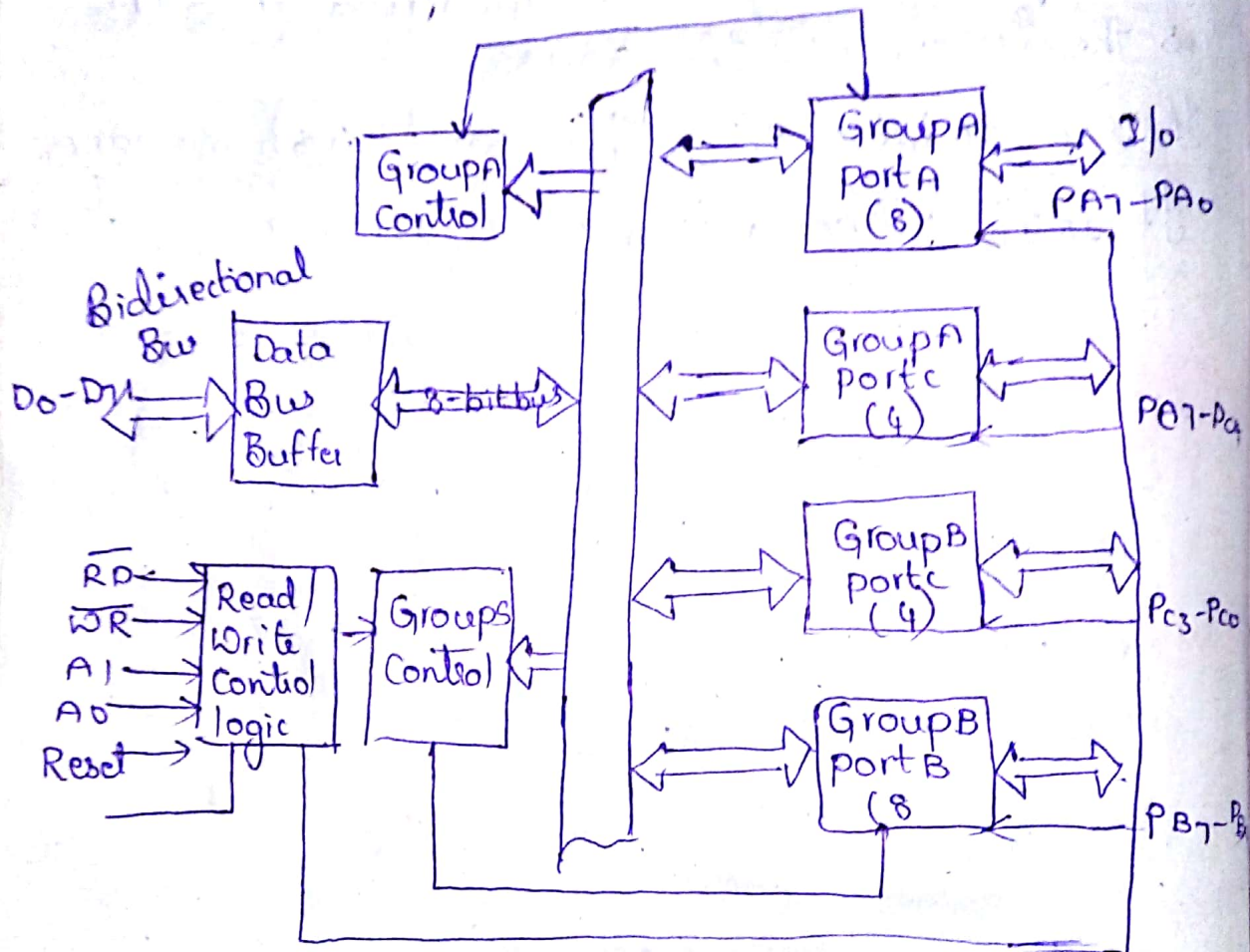
Unit III

Interfacing of 8086

Parallel peripheral Interface 8255

8255 is input output interfacing device Or PPI

It acts as a mediator between CPU to external world



Features of 8255

- 1) It is a 40pin device.
- 2) It contains four ports A, B, C upper port C lower port A - PA_7-PA_0
port C upper - PC_7-PC_4
port C lower - PC_3-PC_0
port B - PB_7-PB_0

3. In this ports one port acts as a control port i.e. ports PC3-PC0 and PC7-PC4

4. The 24 I/O lines divided into two groups i.e. Group A and Group B

Group A Controls the 12 I/O signals i.e. 8 lines of group A and 4 lines of Group A port C upper.

Similarly Group B also controls the 12 I/O signals

8255 Operating On two modes i.e. BSR (Bit Set/Reset mode)

I/O mode

I/O mode have again 3 modes

mode 0 mode 1 mode 2

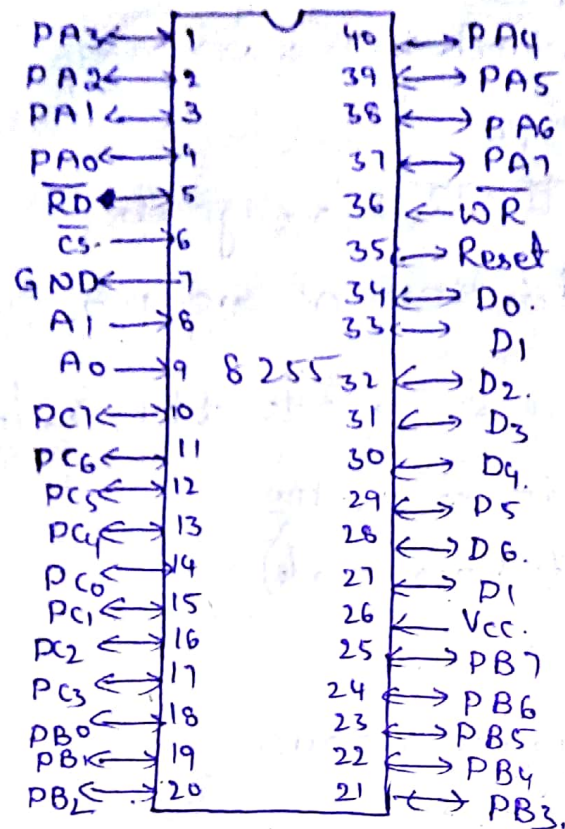
mode 0 called as Simple I/O mode.

mode 1 called as Hand Shaking mode

mode 2 called as Bidirectional mode.

A ₀	A ₁	parameter
0	0	port A
0	1	port B
1	0	port C
1	1	Control logic

Pin diagram of 8255



Pin number

D0-D7 (27-34)

Vcc (26)

GND (7)

A0, A1 (8, 9)

$\overline{RD}$ (5)

$\overline{WR}$ (36)

$\overline{CS}$

RESET

PA7-PA4 (37-40)

PB0-PB7 (18-25)

PC0-PC7 (10-17)

Description

Bidirectional data lines

Vcc +5V Supply (Input)

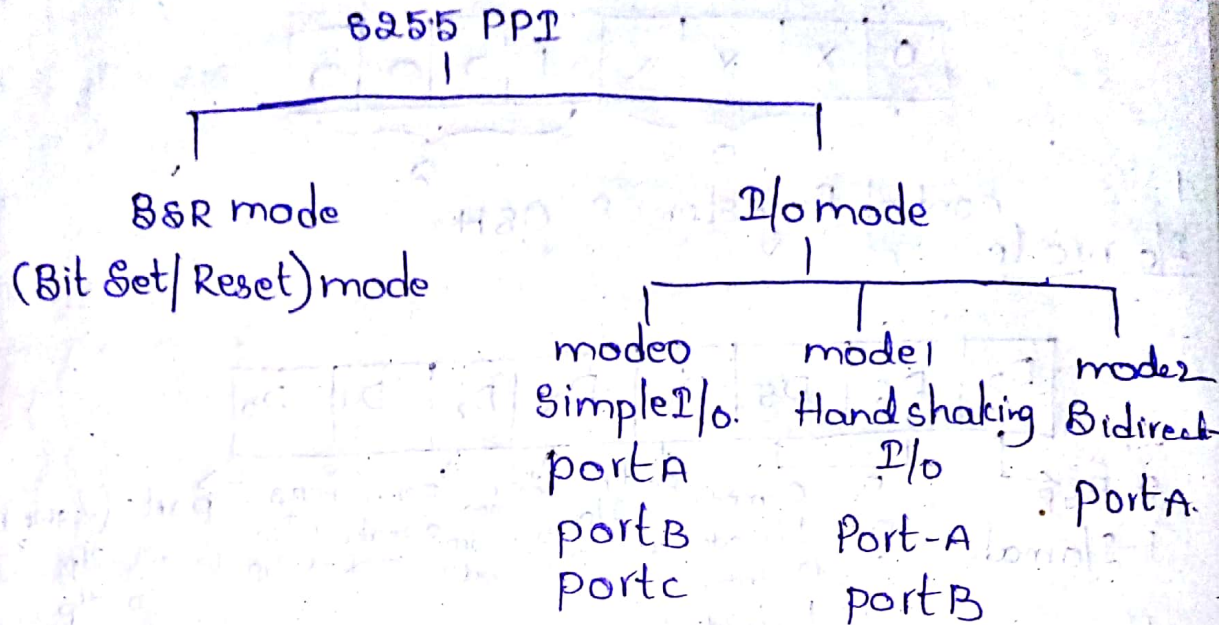
It is a Output pin. It is Used to measure the Signal port Selection.

Read, It is an input Signal to 8255
Write

chip Selection. The Signal is Coming from the decoder.
Reinitialising the data.

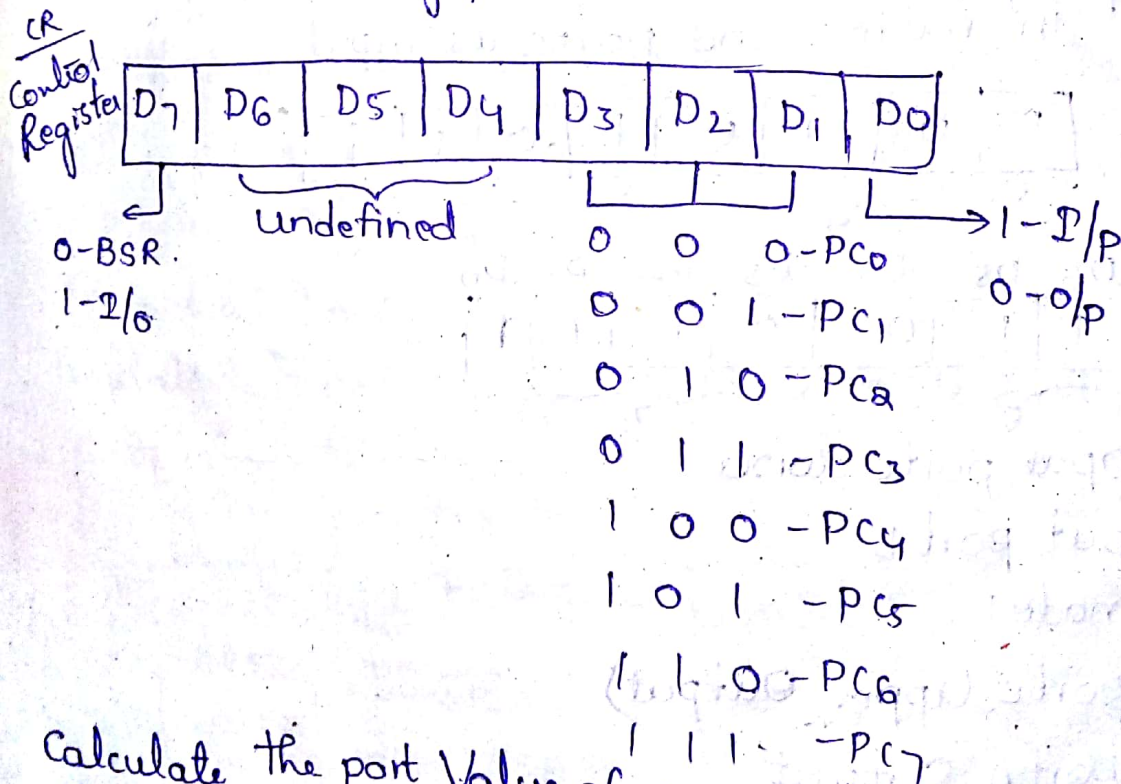
Bidirectional 8 I/O lines
8 Bidirectional I/O line
8 portc I/O line

Modes of 8255 classification of 8255 mode

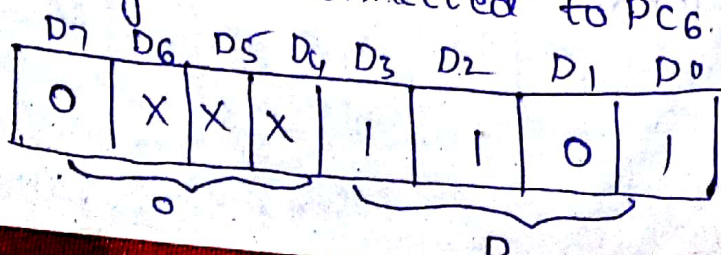


BSR mode +

In BSR mode Only port C is Used for Data transferring

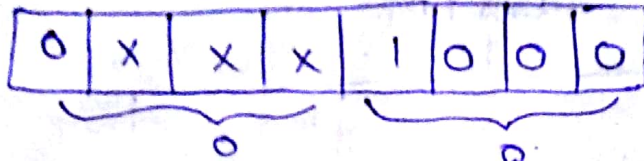


Calculate the port Value of BSR mode in 8255 where the input Signal is Connected to PC₆.

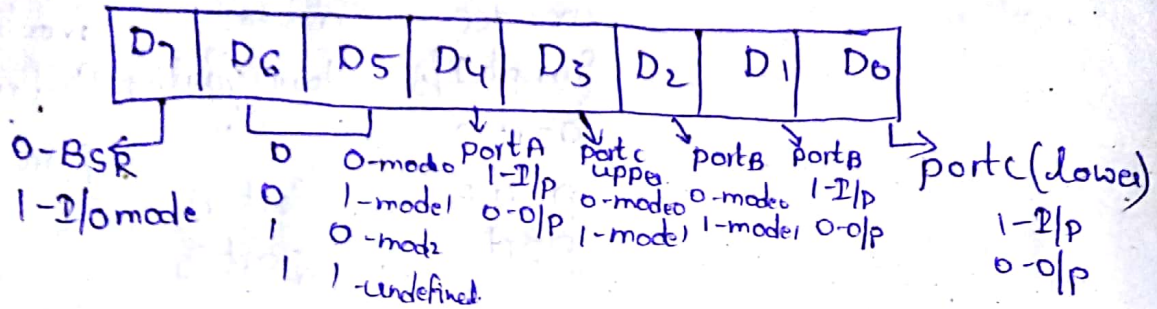


CR = 0D

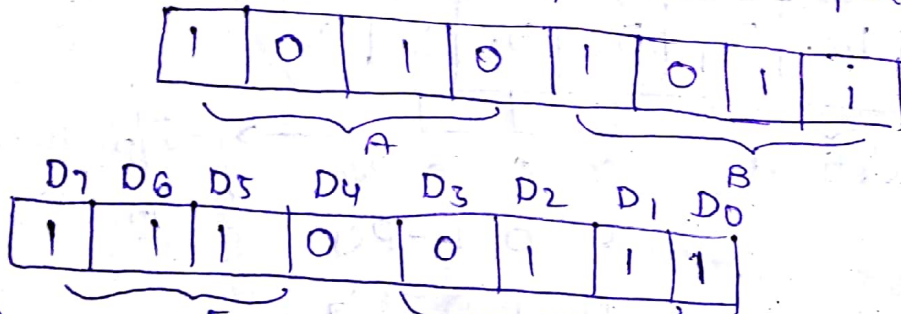
The micro processor of 8086 generates data from SRAM to a monitor through port of 4th line.



I/O mode control Register CR = 08H



Calculate the Control mode register of 8255 when port A Handshaking acts as an input in mode 1 and port B Output in mode 0 and port C is input.



D₀ - Input ports lower

D₁ - Input port B

D_2 -mode 1

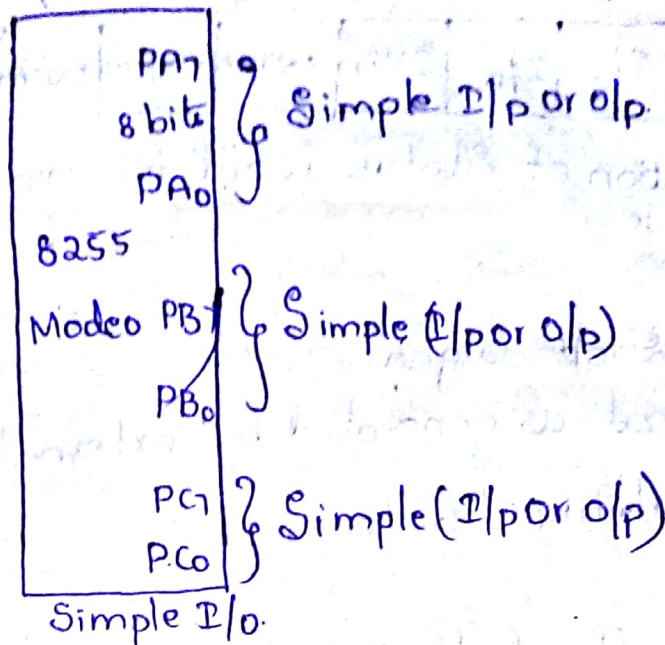
D₃ - portc Upper (Output)

D₄ - port A Output

$D_6, D_5 = \text{Undefined.}$

$D_7 = 2/0$

Mode 0 Configuration



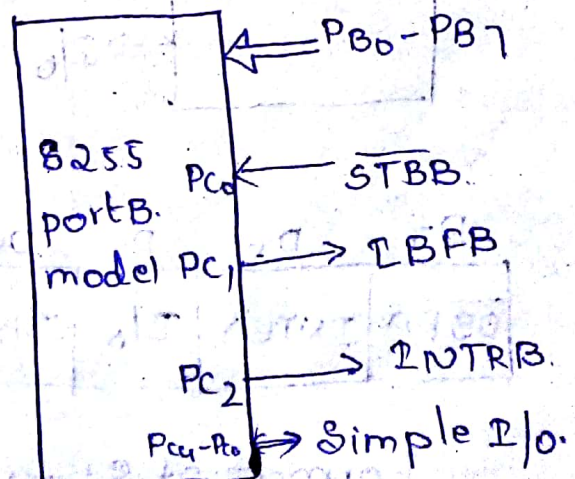
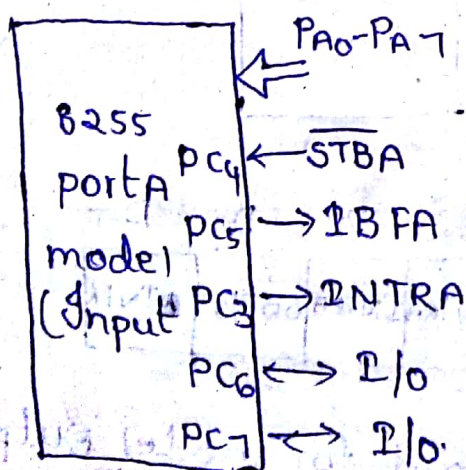
In mode 0 8255 can access any one of the port (port A or B or C) for Simple input Output Operation.

Mode 1 Configuration of 8255 Used for data transferring between I/O devices through 8086.

In this Configuration the data is accessed by Using port A or port B with handshaking signal.

Mode 1 Input Configuration

In mode 1 Input Configuration 8255 allows port A or port B for data transfer and port C is used for Controlling the data transfer.



8255 mode 1 Configuration

	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
CWR (oi)	I/O	I/O	IBFA	INTEA	INTRB	INTEB	IBFB	INTRB

Formation of Status word for model input Operation.
Status register.

STBA - Strobe Signal

This Signal is generated by external I/O devices, indicates the availability of data

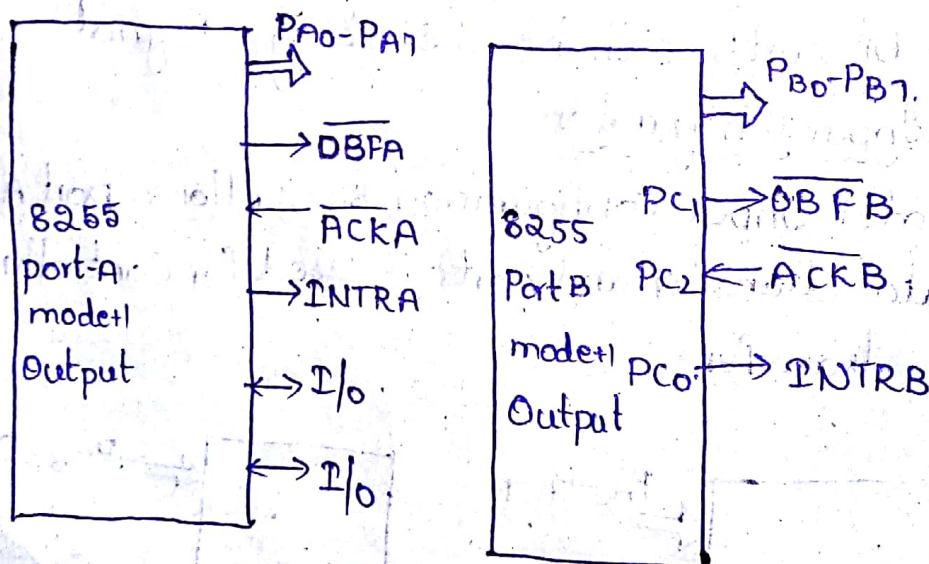
IBFA

Input buffer full. This Signal shows that the buffer is ^{full}

INTRA

Interrupt request Signal.

Model Output Configuration.



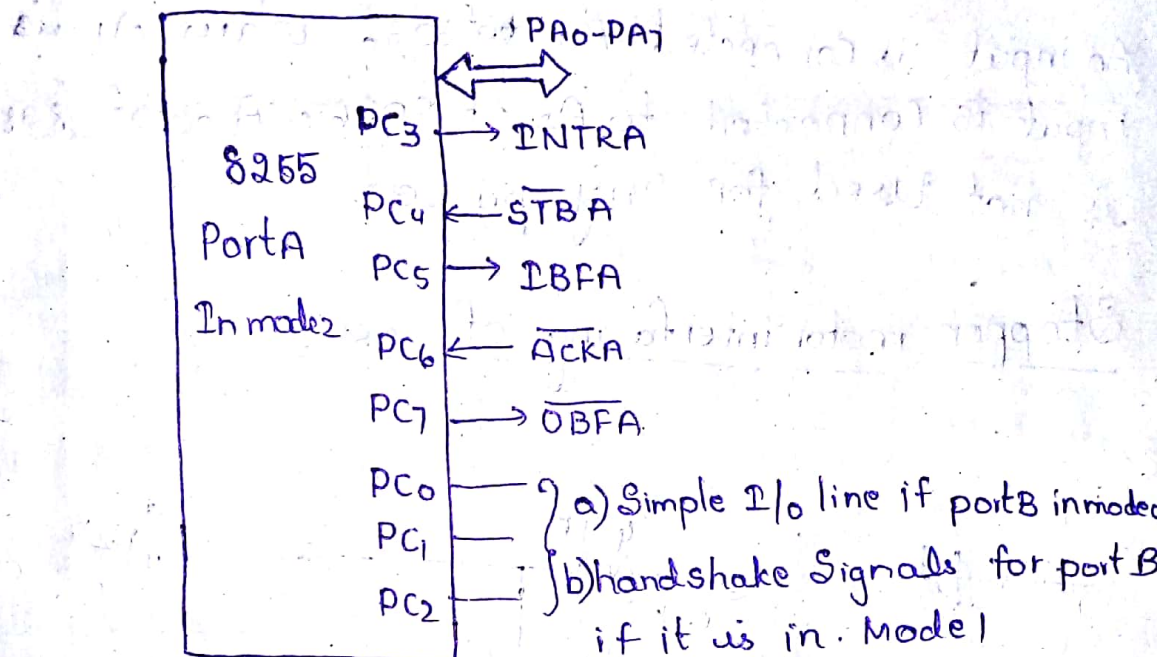
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
DBFA	INTEA	I/O	I/O	INTRA	INTEB	DBFB	INTRB

Format of Status word for model Output Operation.

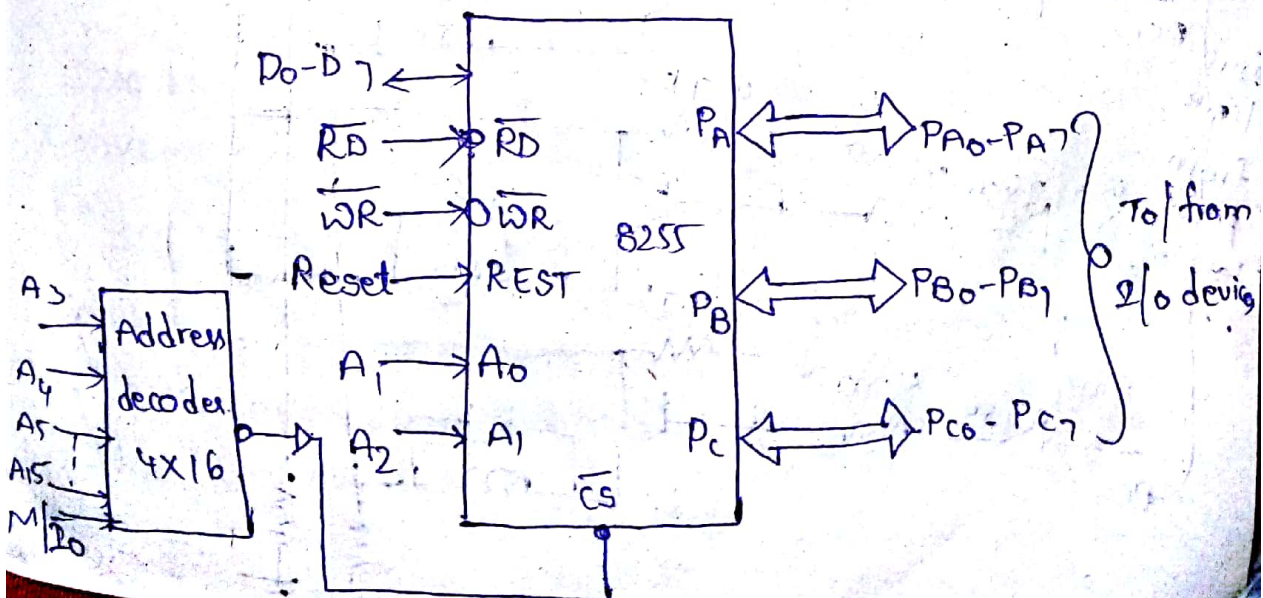
Mode 2 Configuration

In this mode bidirectional data transfer by using port A that means transmitted and received data in same lines.

Here port A can be used for data transferring and 5 bits of port C used for handshaking.



Input Output interfacing of 8255 with 8086



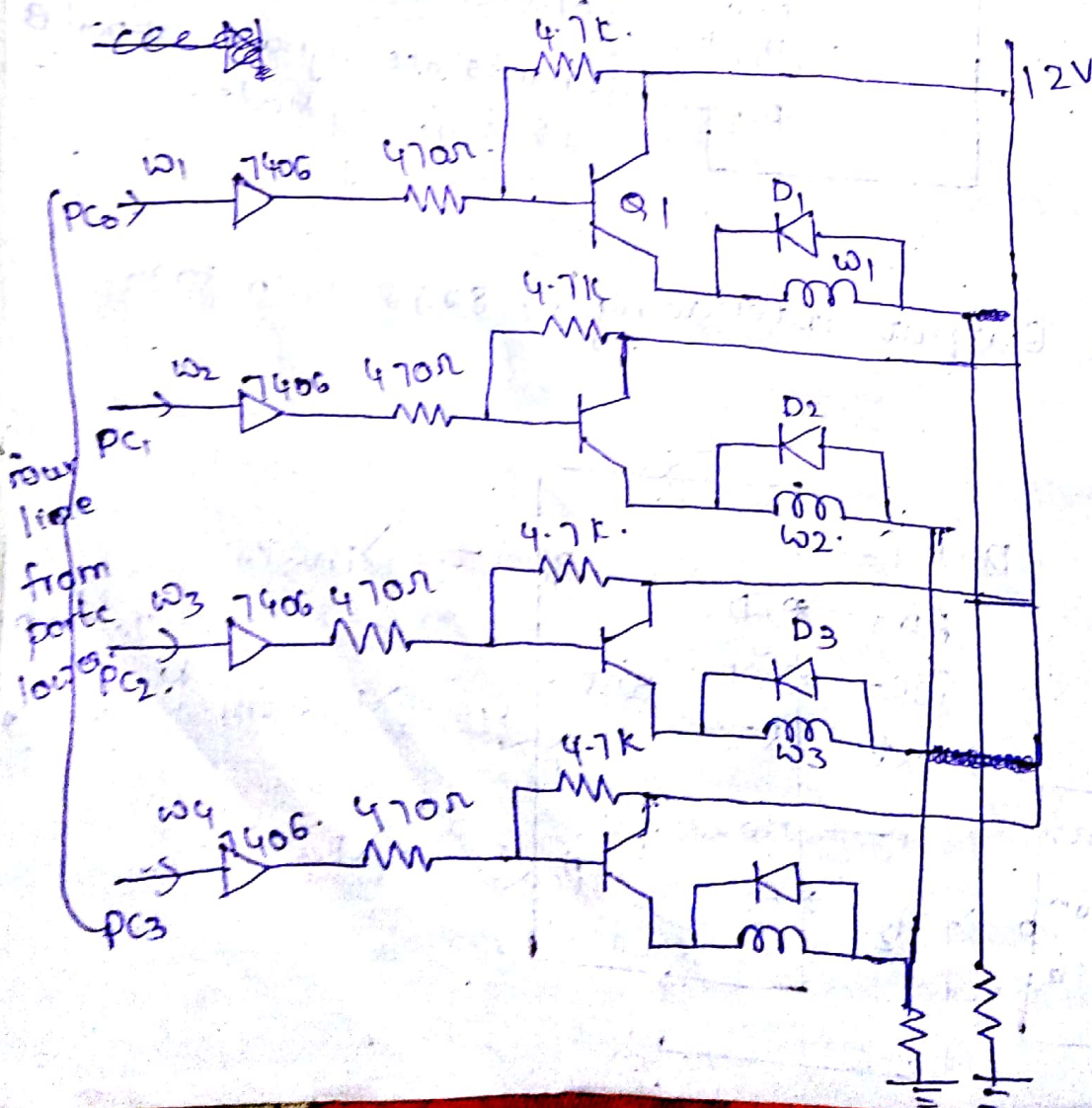
$\overline{CS}$ = chip Selection.

A_1	A_0	Operation
0	0	port A
0	1	port B
1	0	port C
1	1	No operation.

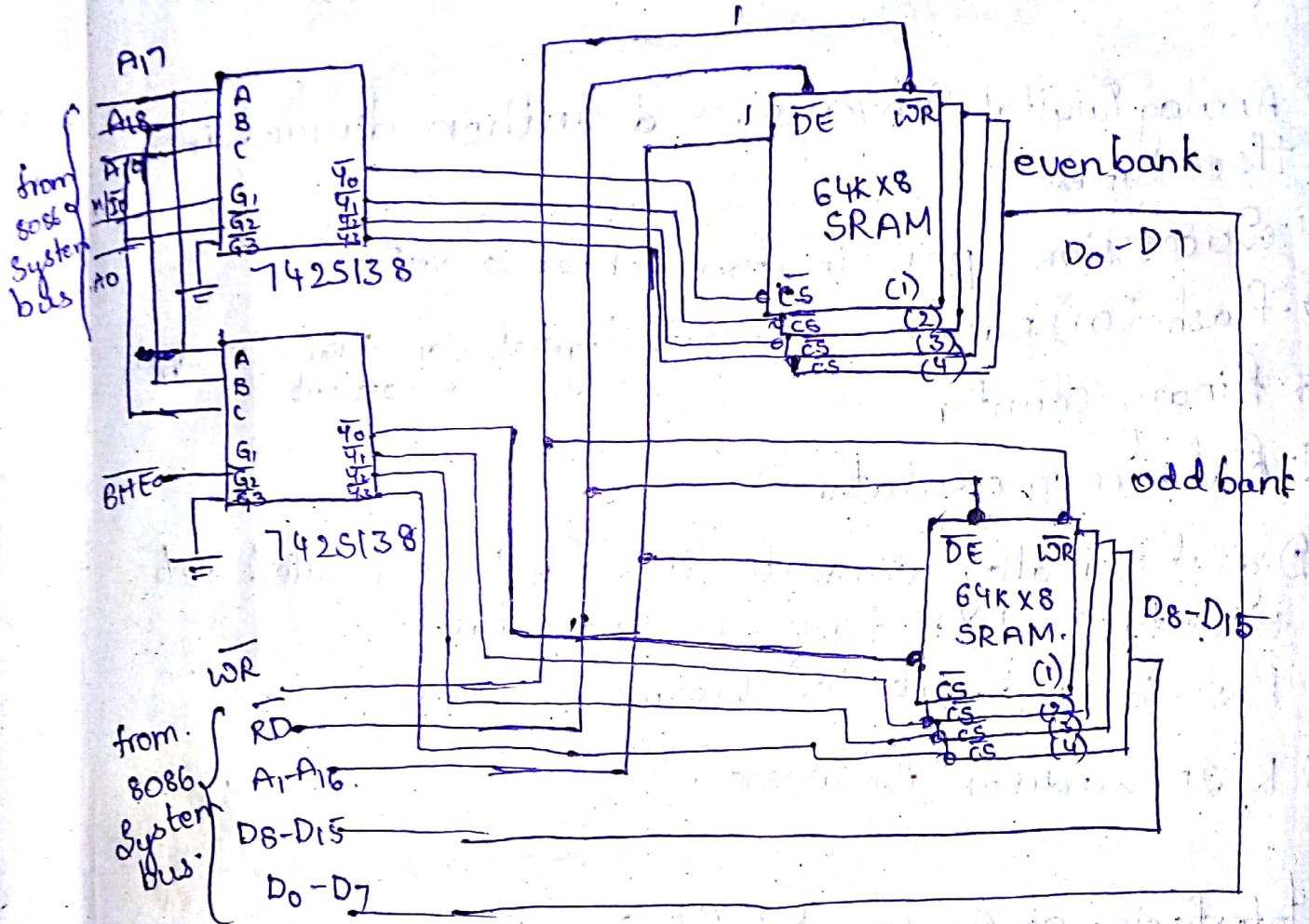
A_0 input is connected to A_1 of 8086 where A_1 is input is connected to A_2 of 8086. A_0 of 8086 is not used for any purpose.

from 8086 system bus

Stepper motor interfacing of 8086.



Static memory interfacing



Converters

Converter converts One form of energy into another form
Examples, transducers

Converters are two types

In microprocessor technology converters are 2 types

1. Analog-Digital Converter
2. Digital-Analog Converter

Analog Signal:-

A Signal changes w.r.t time changes is called Analog Signal

Digital Signal:-

A Signal represented in binary form is called as Digital Signal.

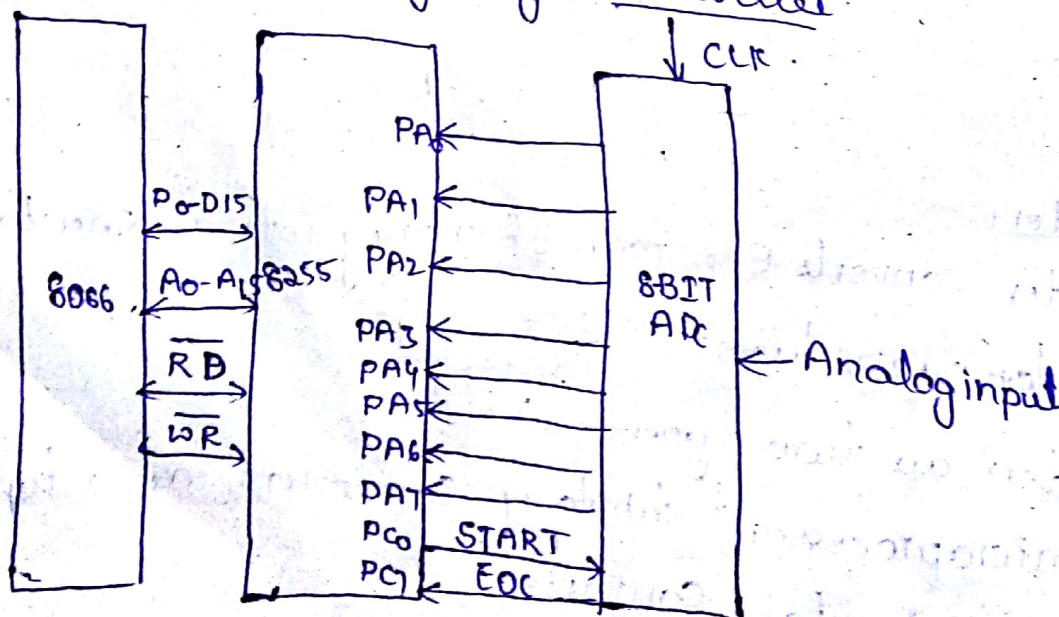
1) Analog-Digital Converter is further divided into three types.

1. Successive approximation - cheap converter
2. Flash (or) parallel - fastest digital converter Ext. Appl.
3. Binary Counter - costliest
4. Balance modulator

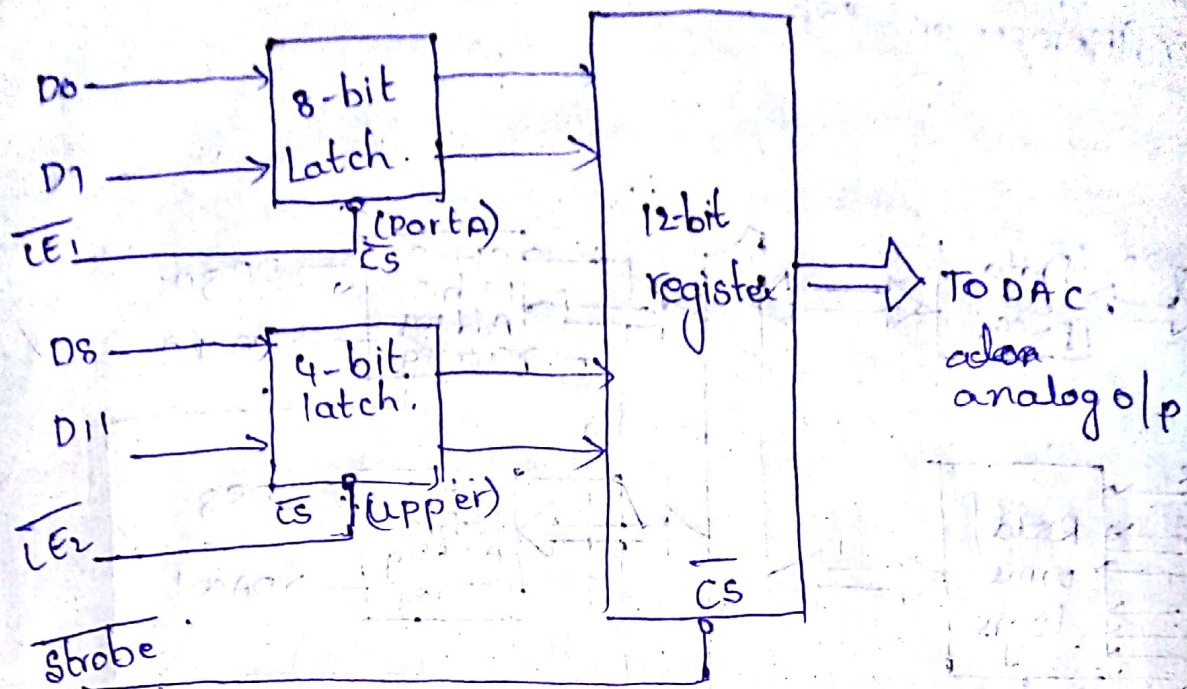
2) Digital-Analog Converter is further divided into three types but two are important

- 1) Resistive network (or) weighted resistor
- 2) R/2R Ladder Network.

Interfacing of Analog-Digital Converter



Latches for 12-bit D/A converter



8255 is having two ports
Latches for the Output
Buffers for the input

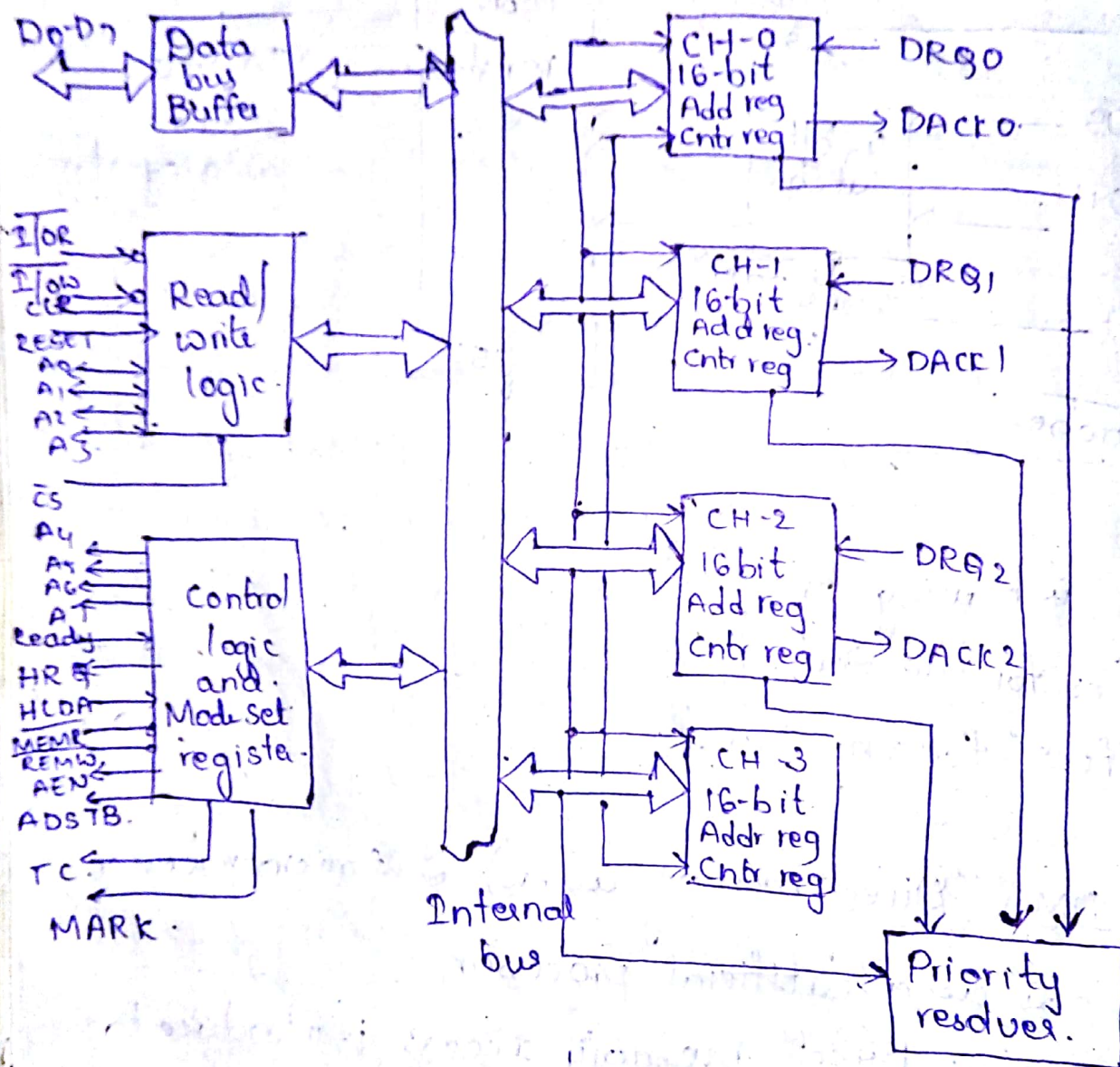
8257 DMA (Direct memory access) Self microprocessor

- 1) DMA acts as a artificial processor
- 2) DMA means Direct memory access is introduce to Speed up the data transfer b/w CPU and peripherals
- 3) Normally in a programmed I/O data transfer an interrupting driven happen by CPU. (without CPU the data will not be transfered b/w peripheral to peripheral)
- 4) This Situation is Solved by using DMA Controller. to enable data transfer b/w peripheral devices and memory without involvement of Microprocessor.

Block diagram of 8257.

Single processor - 8257

Multiprocessor - 8237.



Pin diagram of 8257

<u>IOR</u>	1	40	AT
<u>IOW</u>	2	39	A6
<u>MEMR</u>	3	38	A5
<u>MEMW</u>	4	37	A4
<u>HARK</u>	5	36	TC
<u>READY</u>	6	35	A3
<u>H LDA</u>	7	34	A2
<u>ADSTB</u>	8	33	A1
<u>AEN</u>	9	32	A0
<u>HRG</u>	10	31	VCC
<u>CS</u>	11	30	D6
<u>CLK</u>	12	29	D1
<u>RESET</u>	13	28	D2
<u>DACK2</u>	14	27	D3
<u>DACK3</u>	15	26	D4
<u>DRQ3</u>	16	25	<u>DACK0</u>
<u>DRQ2</u>	17	24	<u>DACK1</u>
<u>DRQ1</u>	18	23	D5
<u>DRQ0</u>	19	22	D6
<u>GND</u>	20	21	D7

8257 Supports 3 types of data transfer i.e

1. Single bit transfer
2. Double bit transfer
3. Demand bit transfer.

DMA Controller is Used to provide an interfacing Memory to I/O. it also Supports I/O to I/O.

DMA is Self programmable IC

The 8257 have different functional blocks named

1. Data bus buffer
2. Read and Write logic
3. Control logic Modeset register
4. Address register
5. Priority resolver.

D0-D7 bidirectional data Used for Read and Write operation b/w Memory to I/O and I/O memory.

I/O Read, I/O Write Memory Write Memory Read performs Read and Write operations b/w Memory ~~and~~ to I/O and I/O memory

CLK Signal is Used to Synchronises the DMA Operation.

DMA Operates in 3 modes

1. ~~Ideal State~~

2. DMA State

1. Ideal mode $\rightarrow$ DMA is not performed

2. Slave mode $\rightarrow$ It is taking Conditions from microprocessor

3. Master mode $\rightarrow$ DMA Controller takes the decision

RESET reinitialises the Condition to 0

A₀, A₁, A₂, A₃ address Signal.

These address Signals are Used to Select channels for data transfer

A ₃	A ₂	A ₁	A ₀	channels
0	0	0	0	CH-0 address register
0	0	0	1	CH-0 Control register
0	0	1	0	CH-1 address register
0	0	1	1	CH-1 Control register
0	1	0	0	CH-2 address register
0	1	0	1	CH-2 Control register
0	1	1	0	CH-3 address register
0	1	1	1	CH-3 Control register
1	0	0	0	Control-Status register

Memory is Connected to A_4, A_5, A_6, A_7
Ready Signal will provide information about whether the DMA Controller is ready to Send the Signal.

Address Strobe ADSTB

This Output from 8257 Used to latch 8 bit data from I/O to memory device.

Memory read Memory write

Memory read Used to read the data from I/O to Memory.

HRQ (Hold Request)

TC - Terminal Count

MARK - It is a pointer decides the Starting and ending of data.

DRQO

Registers of 8257

There are 2 registers Supported by 8257 Controller is
1) Control Word register

2) Status word register

Control Word Register

B7	B6	B5	B4	B3	B2	B1	B0
EAL	ETCS	EEW	ERP	ECH3	ECH2	ECH1	ECH0

FORMAT OF CWR

$B_6 - B_3$ Bit 0 to Bit 3 Used for enabling, or disabling the channels.

Bit-4 (ERP)

Enable Rotating priority

If the bit is 0 fixed priority if it is 1 automatic priority

EEW - Enable extended write

ETCS - Enable Terminal Count Stop

EAL - Enable Auto load

If the bit is 1, it performs repeated operation

Status word Register

B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀
0	0	0		TC ₃	TC ₂	TC ₁	TC ₀

Update flag

FORMAT OF SWR

B₀ - B₃ - These 4 bits are used to indicate status of terminal count of corresponding channel.

B₄ - Update flag

0 - Reset

1 - Auto reload.

Programmable Interrupt Controller 8259

8259 is an interrupt Controller used to call or divert or switch microprocessor to user applications. PIC generates hardware software interrupt control signals for subroutine programs.

Without Interrupt Controller the buses won't share bus signals for multi tasking.

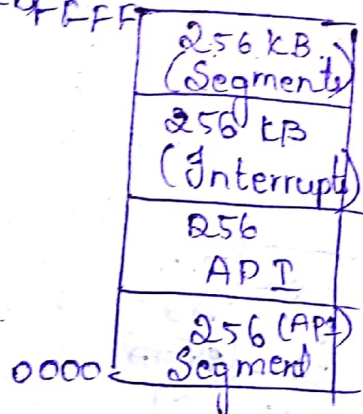
Interrupt is nothing but a task driver to executes multiple tasks in Sequence.

There are 2 types of interrupts namely hardware interrupts and Software interrupt.

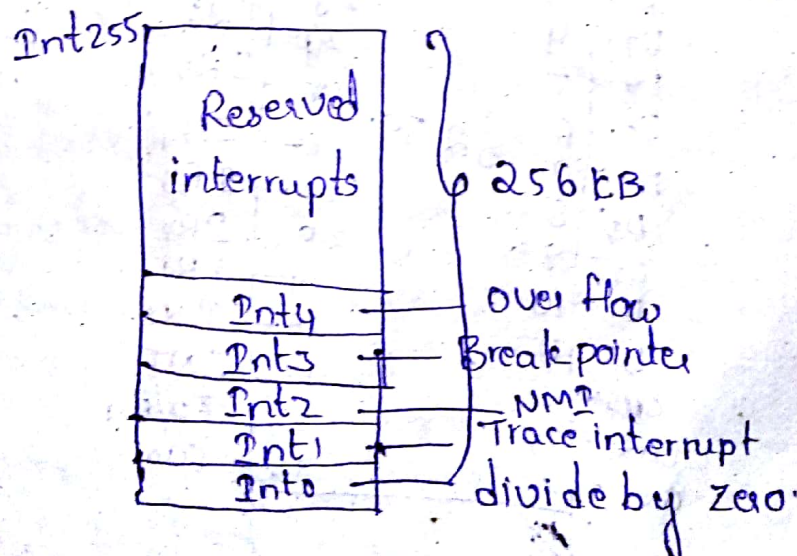
- 1) Maskable :- It diverts processor for subprogram.
- 2) Non maskable execution permanently.
- 3) Non maskable for a time it executes the sub program and continue the main program.

Software interrupts

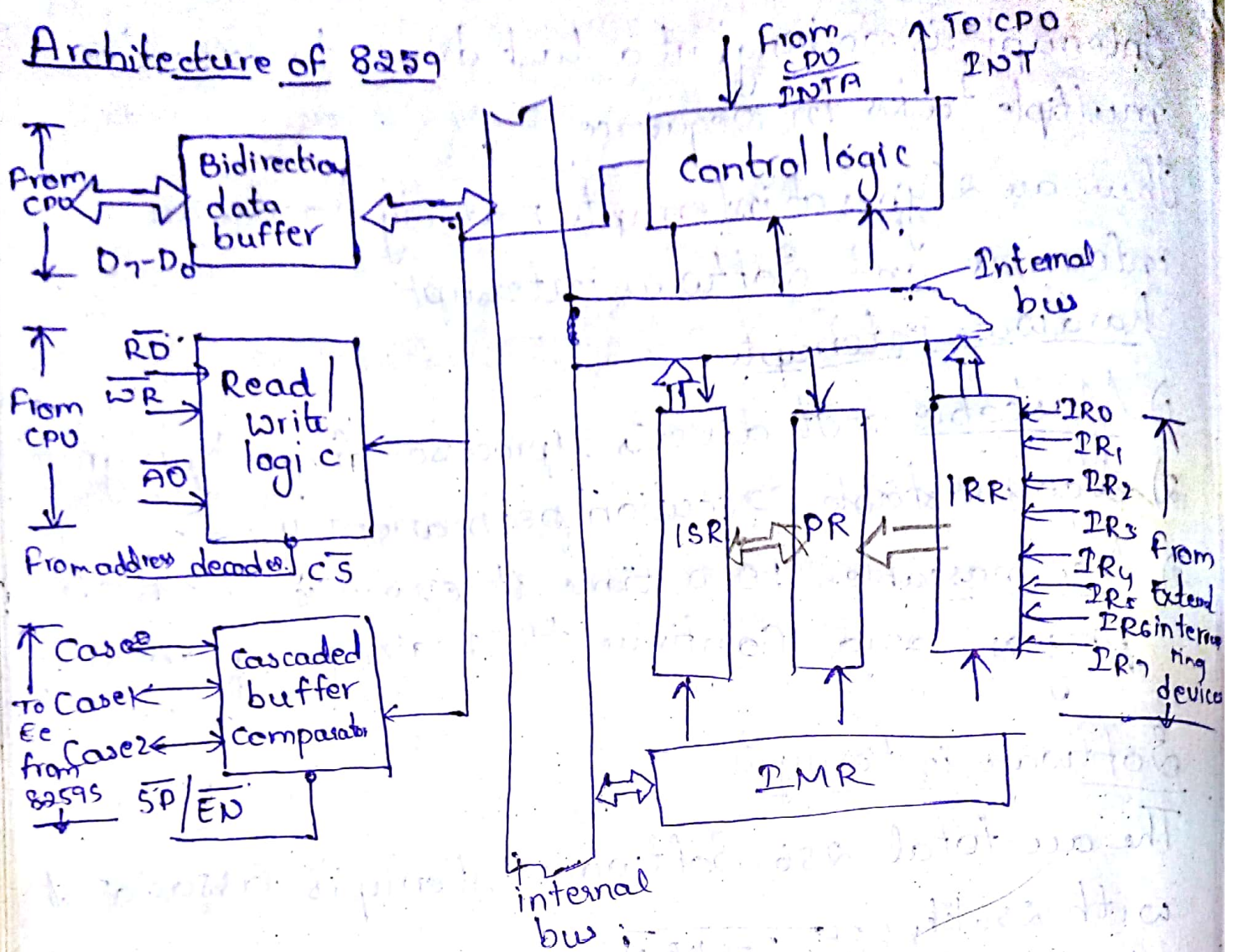
There are total 256 Software interrupts associated with 256 KB FFFF.



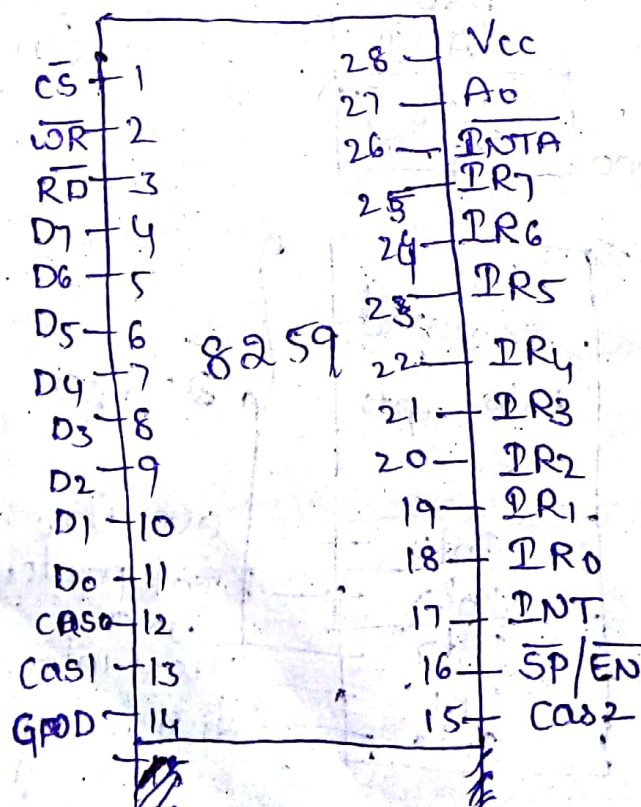
API - Application Specified Interrupt



Architecture of 8259



Pin diagram of 8259



8259 Can be divided into 8 functional blocks.
Bidirectional data buffer:

Read and Write logic:

It controls the data transfer.

$\overline{A0}$:

It is an input signal to 8259 to enable the address signal.

$\overline{cs}$:

chip selection.

cascaded buffer of comparator:

This block provides interfacing b/w one 8259 to another 8259 (or) master 8259 to slave 8259 to expand the interrupts.

Control logic block:

Controls the timing and activities of other blocks.

IRR Interrupt request register.

This block accepts 8 interrupts from external devices.

PR Priority resolver.

It determines the priorities of active interrupt and decides which interrupt should be service and when.

There are different priority schemes which can be selected by software.

1. fixed priority $IR_0 - IR_7$
2. ISR - Service register.

IMR Interrupt mask register
This register is used to mask or disable the interrupt request.

The diagram illustrates the hardware configuration for an 8086 microprocessor system with an 8255 PPI and an 8259 interrupt controller. The 8086 microprocessor is shown on the left with its control and data buses. The 8255 PPI is in the center, and the 8259 interrupt controller is on the right.

8086 Microprocessor Connections:

- Control Signals:** $\overline{RD}$, $\overline{WR}$, $\overline{INTA}$, $M/\overline{IO}$, ALE , and $\overline{AD}_{15}/\overline{D}_{15}$ are connected to the 8255 PPI.
- Address Bus:** $\overline{AD}_{15}/\overline{D}_{15}$ is connected to the 8255 PPI.
- Data Bus:** $\overline{D}_{15}/\overline{D}_0$ is connected to the 8255 PPI.
- Interrupts:** $\overline{INTR}$ is connected to the 8259 interrupt controller. $\overline{IR}_0$ and $\overline{IR}_7$ are also shown.

8255 PPI Connections:

- Control Signals:** $\overline{RD}$, $\overline{WR}$, $\overline{INTA}$, $M/\overline{IO}$, ALE , and $\overline{AD}_{15}/\overline{D}_{15}$ are connected to the 8255 PPI.
- Address Bus:** $\overline{AD}_{15}/\overline{D}_{15}$ is connected to the 8255 PPI.
- Data Bus:** $\overline{D}_{15}/\overline{D}_0$ is connected to the 8255 PPI.
- Interrupts:** $\overline{INTR}$ is connected to the 8259 interrupt controller. $\overline{IR}_0$ and $\overline{IR}_7$ are also shown.

8259 Interrupt Controller Connections:

- Control Signals:** $\overline{RD}$, $\overline{WR}$, $\overline{INTA}$, $M/\overline{IO}$, ALE , and $\overline{AD}_{15}/\overline{D}_{15}$ are connected to the 8259.
- Address Bus:** $\overline{AD}_{15}/\overline{D}_{15}$ is connected to the 8259.
- Data Bus:** $\overline{D}_{15}/\overline{D}_0$ is connected to the 8259.
- Interrupts:** $\overline{INTR}$ is connected to the 8259. $\overline{IR}_0$ and $\overline{IR}_7$ are also shown.

In this mode the highest priority is given by PR_0 and PR_1 has lowest priority.

2) Specific rotation mode
In this mode the priority is assigned to lowest priority and then its interrupts takes in cyclic manner.