1/3/17

Unit -4

Design for Testability

Need of Testing:-

→ According to moore's law feature size is decreasing.
→ As more no of transistors increasing, the feature design coming closer together, they are becoming thinner.
→ There may be chance of wires touching together and may cause faults.
→ We use testing to determine the presence of fault in a chip / circuit.
→ Using testing we increase our confidence in correct working of chip / ckt.

General definitions:-

Defect:- The term defect generally refers to the physical imperfection in the processed wafer.
Some defects are observable through optical or electron microscope. Others are not visible and can only be detected by electrical tests.

Fault:- A representation of a defect at the abstracted function level is called fault.

Error:- A wrong o/p signal produced by a defective system is called an error.

Failure:- Repeated occurrance of the same defect indicates the need for improvements in the manufacturing process or the design of the device.

Procedures for diagnosing defects and finding their causes are known as failure mode Analysis (FMA)

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Fault types and models:-

→ Fault may be arise at fabrication prouss, design and at Stressful operating conditions.

→ A Test vector is a set of inputs provided to a system inorder to test that system.

→ DUT / CUT (Device Under Test / Ckt under test) - A device that is to be tested to determine performance and proficiency.



Measured o/p's are compared with the expected correct responses to check whether DUT is good (go) or bad (no-go).

Operating clock frequency of the chip increased, the speed test has also become a difficult problem.

→ The generation of correct test vectors to detect faults and design errors through ATPG (Automatic Test Pattern Generation).

Physical defects:- (at the time of fabrication prouss)

Includes

→ Defect in silicon substrate
→ Photolithographic defects
→ Mask contamination and Scratches
→ Process variations and abnormality
→ Oxide defect

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Note: Physical defects may cause Electrical-faults and logical-faults

Electrical-faults

They include

→ Short (bridging)
→ Opens
→ Transistor shorts and opens
→ Resistive shorts & opens

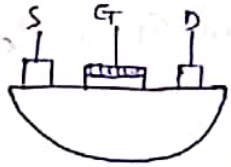
Electrical-faults cause logical-faults

logical fault defects:-

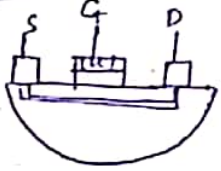
⇒ logical stuck-at-0 or stuck-at-1

→ Slow speed transition (delay-fault)

Stuck at faults:-



Stuck at-0:- It means the line is fixed to logic 0 for any combination of applied I/p's

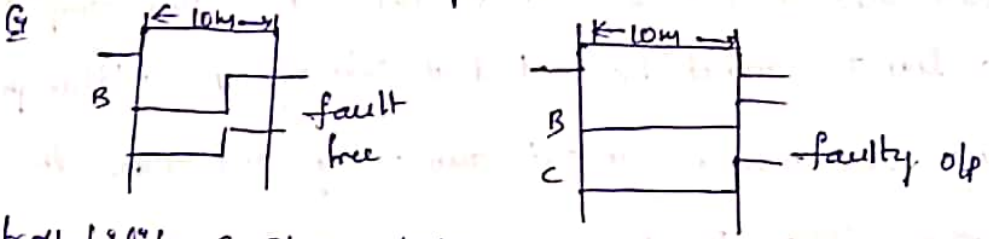


Stuck at-1:- It means the line is fixed to logic 1 for any combination of applied inputs

Delay-fault:-

Due to the cause of propagation delay we may have faulty o/p





Controllability & Observability:-

→ Controllability is the ease of setting the o/p node to either '0' or '1' just by driving I/p lines of chip.

→ Observability is the ease of watching o/p pins of a chip.

Testability:- It is a metric to measure the degree of difficulty to the ckt.

→ The degree of above three are measured w.r.to test vectors.

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→ for a randomly generated test vector the o/p node is set to have low controllability and hence it is have low testability.

→ The deterministic procedure for test vectors generation is D-algorithm

D- algorithm:- 1) Target a specific stuck at fault.

2) Drive fault side to opposite value.

3) propagate error to primary o/p.

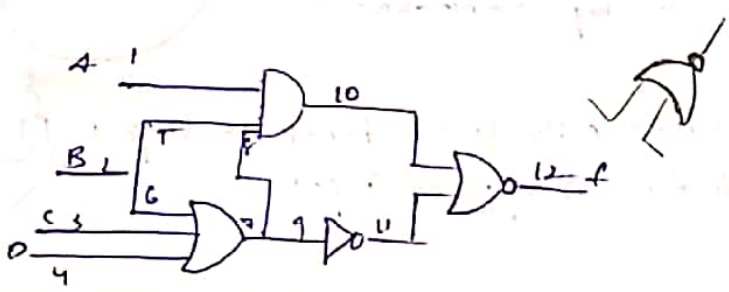
4) Generate pattern for one stuck at fault at a time involve design at almost every step.

Disadvantage:-

It is time taking process.

To overcome time consuming drawback we use advanced technique called path oriented Design Making process (PODEM).

Sequential ckts are more difficult to test and generate is also difficult. So to ease the task ATPG (Automatic Test Pattern Generation) and DFT (Design for Testability) are used.



To detect any defect on line 8, primary i/p's A, B are set to 1 such a setting forces line 7 to 1. Thus any stuck-at 1 on line 7 can not be tested at primary o/p. Although the absence of such a fan out also fully controllable through primary i/p's B, C, D.

∴ The ckt is not fully testable.

The main cause is line B fan out 5,6 and then OR3 and then AND3 such a fan out is called Reconvergent fan out it makes the ckt much more difficult

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Path sensitization method :-

→ It is used to detect stuck at faults

The main aim is to generate the test vectors and it is based on

The fault line is to be forced with a opposite value

is stucked to

Then propagate the error to one of the o/p line. If o/p is

different from expected o/p then we can say fault is

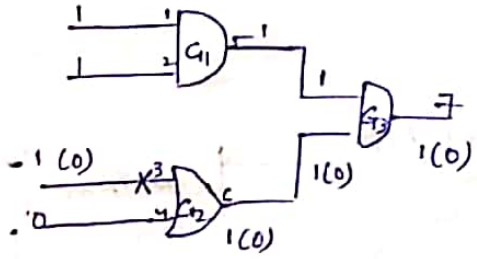
present.

Steps to find test vectors through path sensitization method :-

1. fault excitation
2. fault propagation
3. Back tracking

Let the following diagram is having stuck at-0 at node 3.

Test vector → 1110



Scan based technique for testing :-

(Design for Testability)

This technique is most widely used DFT technique.

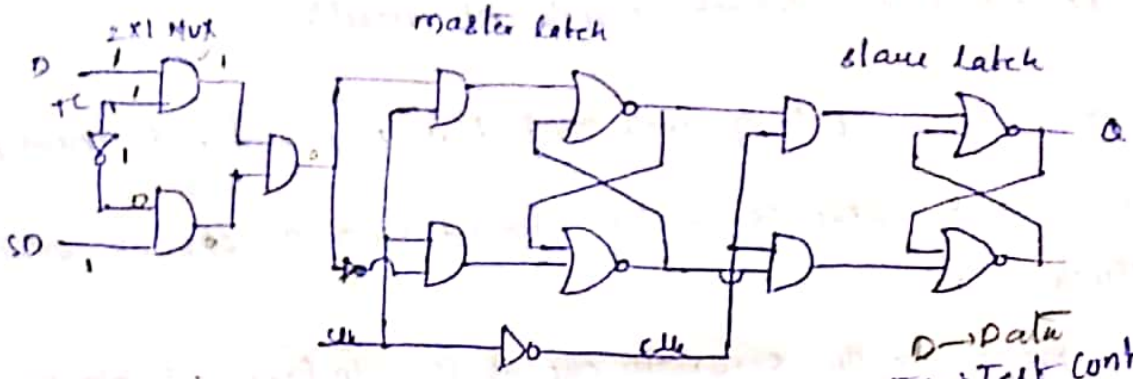
Scan path can be inserted in a non-scan sequential ckt netlist in an automated way

Steps :-

1) All flip-flops are replaced by scanned flipflops
2) Connect the scan flipflops as configurable ~~shift~~ registers shift

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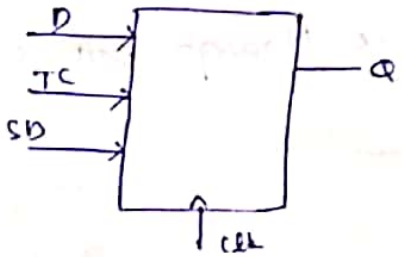
3) Add scan i/p & o/p for shift registers and add test control as primary i/p.



D → Data
TC → Test control
SD → Scanned data

Master - slave D - flip flop

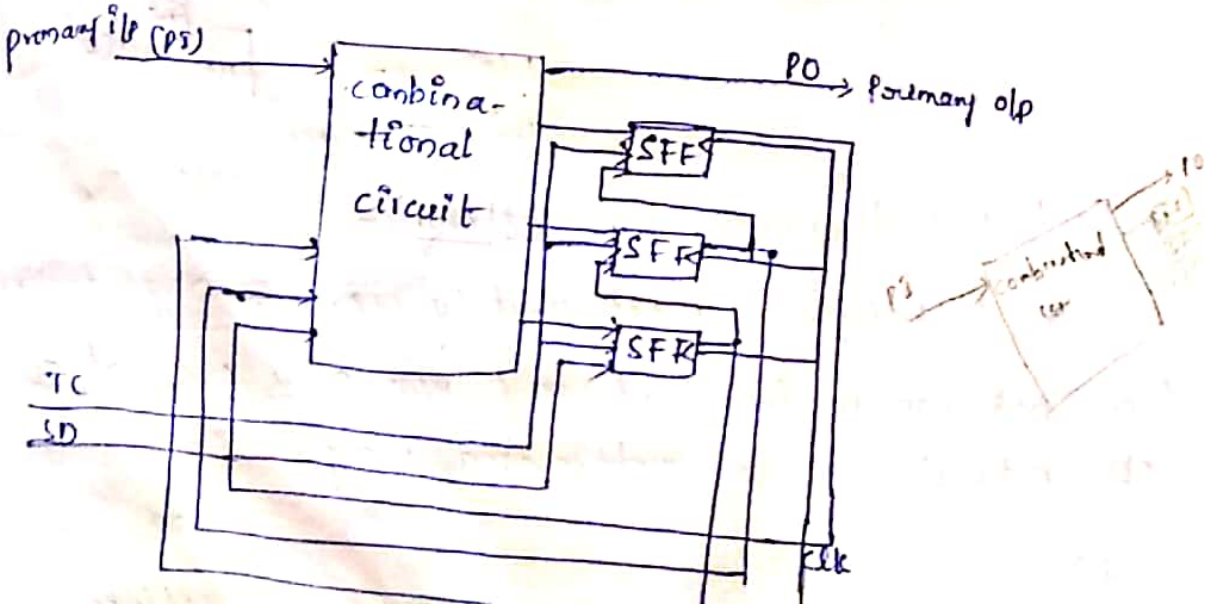
- Clocked flip flops
- Scanned flip flops



Schematic diagram of scanned flip flop

→ when TC=1, the ckt is in normal mode and no. of gates operated are 10 (10)

→ when TC=0, the ckt is in test mode and no. of gates operated are 14. (14)



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Scanned design rules:-

1. Use only clocked flip flops as storage elements.
2. Atleast one primary i/p pin must be available for test.
3. All clocks must be directly fed from i/p's, so the scanned flip flops can work properly in a scanned register.
4. Clock signal must not fed data i/p's to the flip-flops (to avoid race around condition).

Scanned path:-

In scanned base design, storage elements are connected to form long serial shift registers and so called as scanned path.

BIST (Built in Self Test):-

BIST is a technique where a ckt can test itself

→ We add extra hardware to the chip for test generation and for response evaluation.

→ The ckt consists of

1. Pseudo Random Pattern generator (PRPG)
2. O/p response analyzer (ORA)

→ The procedure of BIST can be explained with the following diagram.

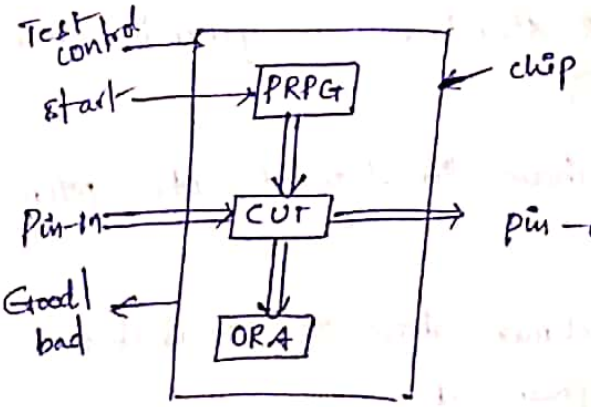
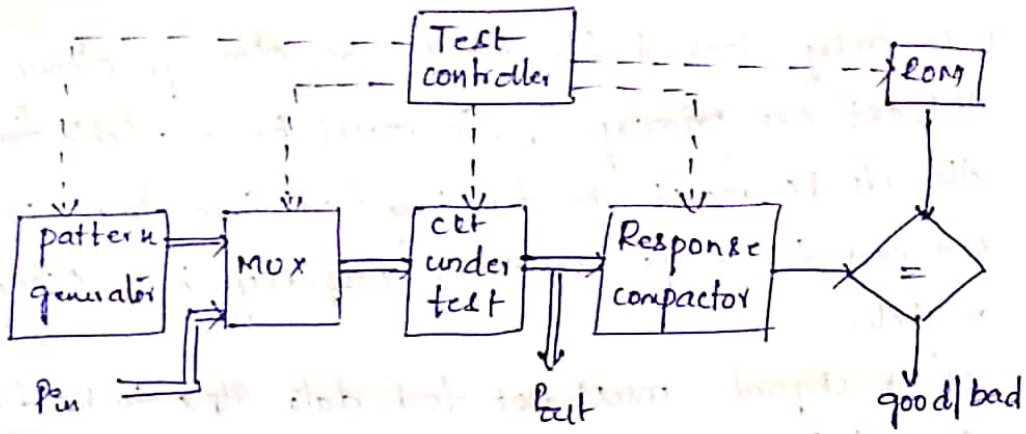


fig: procedure for BIST

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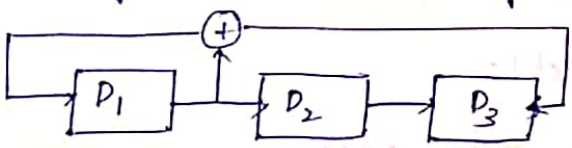
Architecture of BIST :-



Pseudo random pattern Generator (PRPG):-

→ In PRPG we use random patterns as i/p test vectors and it can be implemented using LFSR (linear feedback shift registers) and X-OR gates.

Ex:



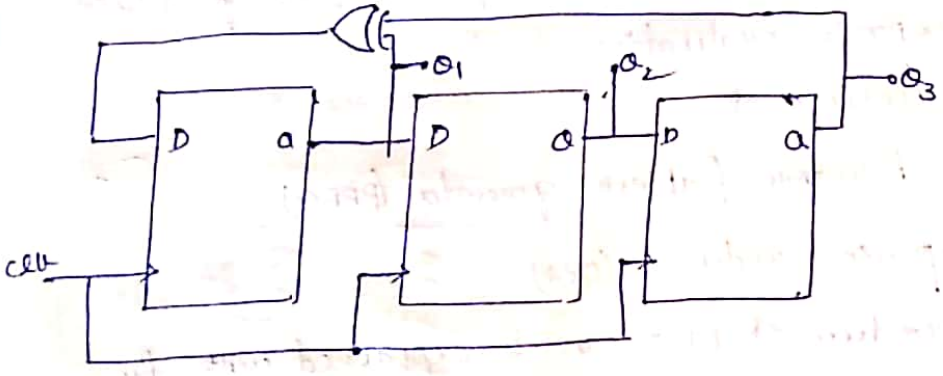


fig: PRPG using LFSR

→ Based on the LFSR structure we generate characteristic polynomials.

→ For the fig. shown above the characteristic polynomial

$$P(x) = x^3 + x + 1$$

→ Based on the fig. shown above the generated random patterns can be given as.

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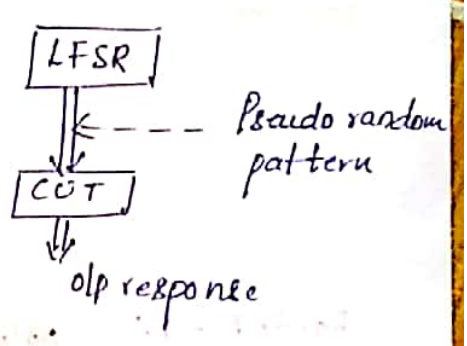
D_3	D_2	D_1	
1	0	0	→ 4
0	0	1	→ 1
0	1	1	→ 3
1	1	1	→ 7
1	1	0	→ 6
1	0	1	→ 5
0	1	0	→ 2

Note :- Here all zeroes pattern is missing i.e, if we load LFSR with all zeroes pattern then it remains in all zeroes pattern i.e, the reason all zeroes pattern is neglected.

→ Having random pattern generations is a good thing because if any of the pattern fails and remain all functions properly.

Output Response Analyzer :- (ORA)

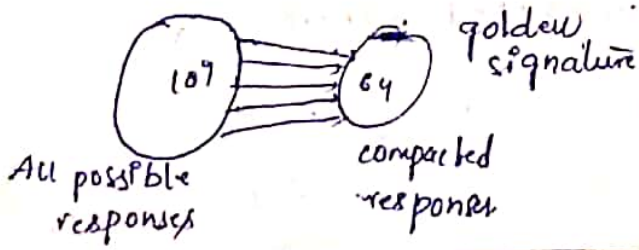
The LFSR as o/p response analyzer is shown below Suppose a ckt of 100 no of i/p's with a billion no of test patterns, then the o/p is of 100 lines each of billion size.



→ So the o/p is so huge to store in a ROM and it should have greater capacity which is expensive.

→ So we need to reduce the o/p i.e, o/p response compression is done and this process is called Signature Analysis.

→ Large volume of response is compacted into a signature before comparison and the golden signature is stored on-chip.



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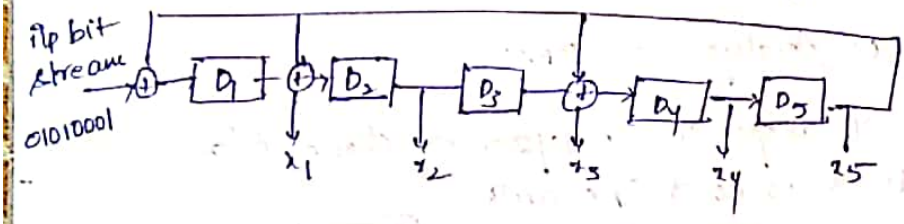
In the above eq. the mapping is between one billion to 64bit it is a huge compaction due to huge compaction there may be a possibility such that some errors may get mapped to golden response and those faults may get undetectable and is called as aliasing.

Aliasing :- The signature in presence of faults matched with the golden signal and the faults goes undetectable.

LFSR based response compaction :-

It is having 2 approaches.

1. compact a single serial bit into a LFSR based compactor called as signature analyzer.
2. Compact several serial bit stream into a special LFSR based compactor, called as multiple i/p signature register (MISR).



eq: polynomial division using LFSR signature analyzer

characteristic polynomial $P(x) = x^5 + x^3 + x + 1$

i/p polynomial from the bit pattern

$$F(x) = x^7 + x^3 + x$$

$$P(x) = x^5 + x^3 + x + 1$$

Divide $F(x)$ by $P(x)$ and then take the remainder then it is treated as compacted response.

∴ The remainder $R(x)$ can be given as

$$x^3 + x^2 + 1$$

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Adhoc testable design technique:-

→ If large no of ilp test vectors are required to set a particular node to either '0' or '1' then testability is low.

→ Adhoc design techniques are those which are used to have increased testability.

Some of the Adhoc testable designs are explained below.

1. Partition and MUX technique:-

Sequence of many serial gates, functional blocks are difficult to test, such ckts can be partitioned and MUX's can be inserted such that primary ilps can be fed to partition nlws through MUX's.

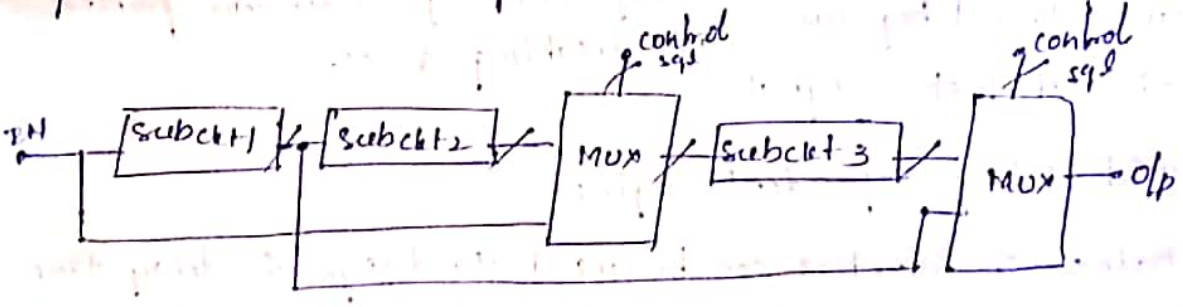


Fig: partition and MUX method for a large ckt.

Ex: Using this technique no of accesible nodes can be increased and no of test patterns can be reduced. Hence testability is more.

Drawback:-

Using MUX's in this technique may lead to increased delay and ckt area.

2. Initialization of Sequential Circuits:-

When Sequential ckts are latched, its initial state is random.

In this case, it is not possible to start the test-

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sequence correctly.

→ Hence the state can be brought to known state by initialization.

→ Initialization can be done by connecting all latches or flip-flops to clear i/p.

3. Disable internal oscillators and clocks :-

→ To avoid synchronization problems, during testing, internal oscillators & clocks should be disabled.

→ Rather than connecting the clk directly to the on-chip oscillator, clk can be ORed with a disabling signal followed by an insertion of test signal

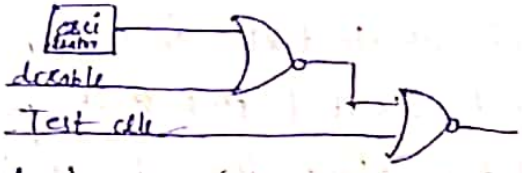


fig: avoid synchronization problem via disabling of osc.

4. Avoid delay dependent logic :-

Chains of inverters can be used to design in delay time and use AND operation of their o/ps along with i/p to generate pulse.

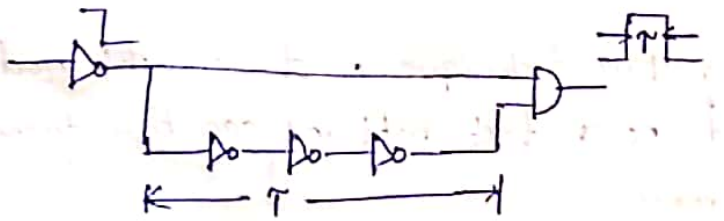


fig: pulse generator ckt using a delay chain of three inverters

→ Most ATPG (Automatic Test Pattern Generation) programs do not include logic delays to minimize the complexity of the program.

→ Such a delay dependent logic can be viewed as redundant combinational logic, and these are avoided in the design for testability.

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