UNIT – IV: ADVANCED MICROPROCESSORS

SALIENT FEATURES OF 80386:

80386 is a 32bit microprocessor

Two versions of 80386 are commonly available:

1) 80386DX

2) 80386SX

80386DX	80386SX
1) 32-bit address bus, 32-bit data bus	1) 24-bit address bus, 16-bit data bus
2) Packaged in 132 pin ceramic pin grid array(PGA)	2) 100 pin flat package
3) Address 4GB of memory	3) 16 MB of Memory

80386SX was developed after the DX for application that didn't require the full 32-bit bus version. It is found in many PCs use the same basic mother board design as the 80286.Most application less than the 16MB of memory, so the SX is popular and less costly version of the 80386 microprocessor.

- The 80386 CPU supports 16k no of segments and thus total virtual memory space is 4GB *16 k=64 tera bytes
- Memory management section supports
  - Virtual memory
  - Paging
  - 4 levels of protection
  - 20-33 MHz frequency

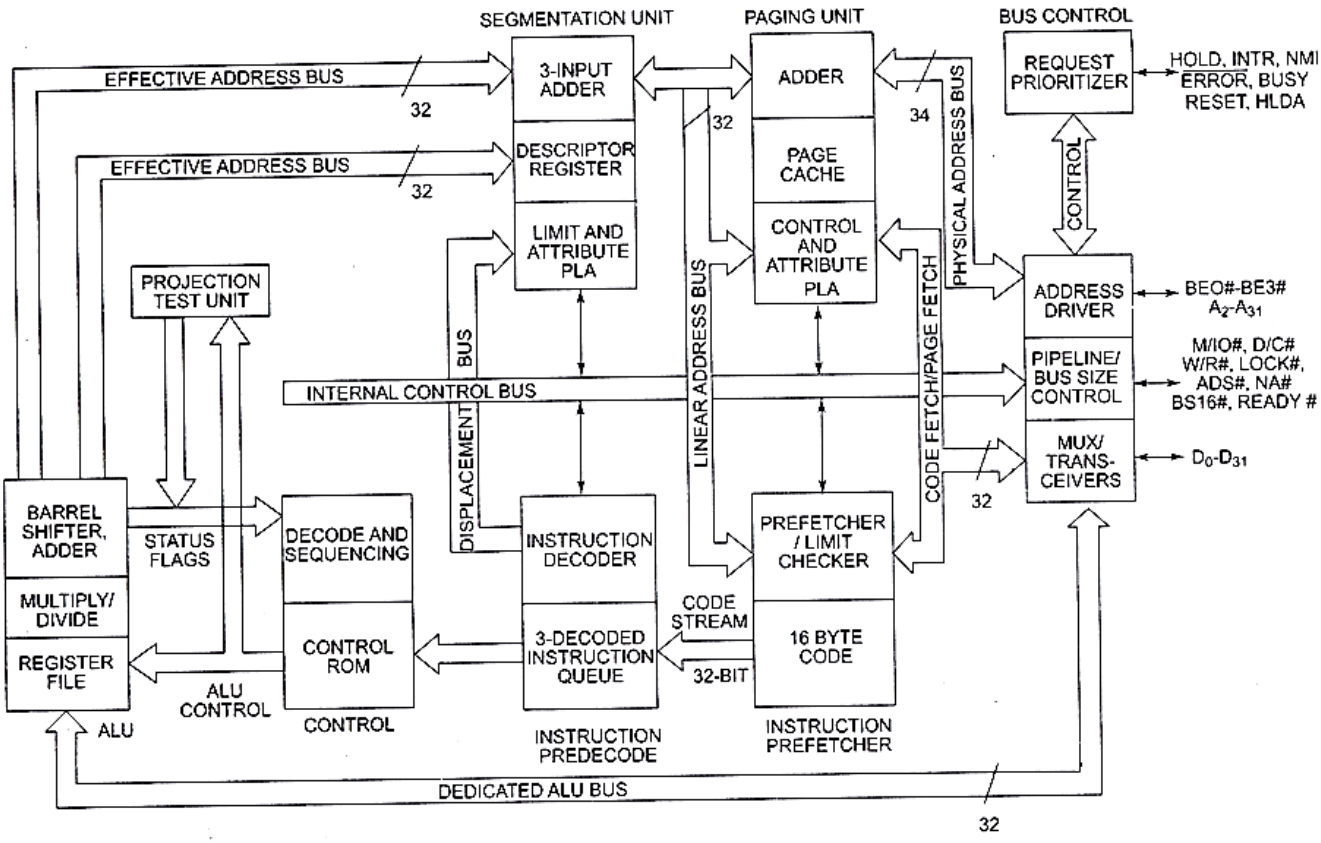
Architecture of 80386:

The Internal Architecture of 80386 is divided into 3 sections.

- Central processing unit(CPU)
- Memory management unit(MMU)
- Bus interface unit(BIU)

✓ Central processing unit is further divided into Execution unit(EU) and Instruction unit(IU)

✓ Execution unit has 8 General purpose and 8 Special purpose registers which are either used for handling data or calculating offset addresses.



80386 Architecture

✓ The Instruction unit decodes the opcode bytes received from the 16-byte instruction code queue and arranges them in a 3- instruction decoded instruction queue.

✓ After decoding them pass it to the control section for deriving the necessary control signals. The barrel shifter increases the speed of all shift and rotate operations.

- ✓ The multiply / divide logic implements the bit-shift-rotate algorithms to complete the operations in minimum time.
- ✓ Even 32- bit multiplications can be executed within one microsecond by the multiply / divide logic.
- ✓ The Memory management unit consists of
    - ➢ Segmentation unit
    - ➢ Paging unit.

- Segmentation unit allows the use of two address components, viz. segment and offset for re-locability and sharing of code and data.
- **Segmentation** unit allows segments of size 4Gbytes at max.
- The Paging unit organizes the physical memory in terms of pages of 4kbytes size each.
- **Paging** unit works under the control of the segmentation unit, i.e. each segment is further divided into pages. The virtual memory is also organizing in terms of segments and pages by the memory management unit.
- The Segmentation unit provides a 4-level protection mechanism for protecting and isolating the system code and data from those of the application program.
- Paging unit converts linear addresses into physical addresses.
- The control and attribute PLA checks the privileges at the page level. Each of the pages maintains the paging information of the task. The limit and attribute PLA checks segment limits and attributes at segment level to avoid invalid accesses to code and data in the memory segments.
- The Bus control unit has a prioritizer to resolve the priority of the various bus requests. This controls the access of the bus. The address driver drives the bus enable and address signal A0 – A31. The pipeline and dynamic bus sizing unit handle the related control signals.
- The data buffers interface the internal data bus with the system bus.

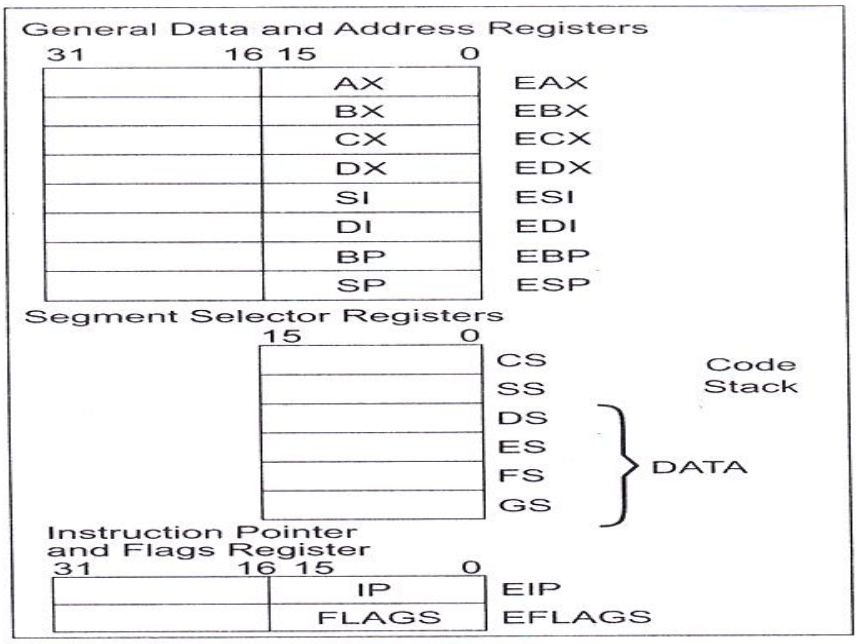
Register Organization:

- The 80386 has eight 32 - bit general purpose registers which may be used as either 8 bit or 16 bit registers.
- A 32 - bit register known as an extended register, is represented by the register name with prefix E.

Example: A 32-bit register corresponding to AX is EAX, similarly BX is EBX etc.

- The 16 bit registers BP, SP, SI and DI in 8086 are now available with their extended size of 32 bit and are names as EBP, ESP, ESI and EDI.

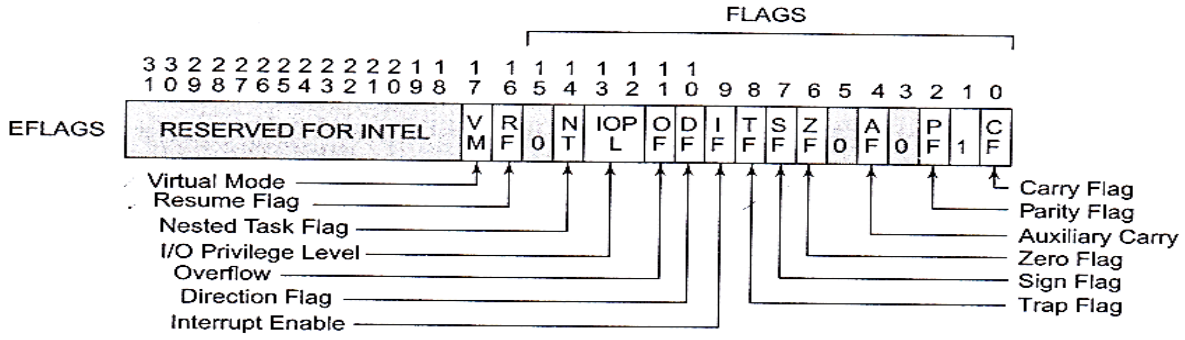
- AX represents the lower 16 bit of the 32-bit register EAX.



Registers Bank of 80386 (Intel Corp.)

- BP, SP, SI, DI represents the lower 16 bit of their 32-bit counterparts, and can be used as independent 16 bit registers.
- The six segment registers available in 80386 are CS, SS, DS, ES, FS and GS.
- The CS and SS are the code and the stack segment registers respectively, while DS, ES, FS, GS are 4 data segment registers.
- A 16-bit instruction pointer IP is available along with 32-bit counterpart EIP.

Flag Register of 80386:



Note: 0 indicates Intel reserved

Flag Register of 80386 (Intel Corp.)

The Flag register of 80386 is a 32-bit register. Out of the 32 bits, Intel has reserved bits D18 to D31, D5 and D3, while D1 is always set at 1. Two extra new flags are added to the 80286 flag to derive the flag register of 80386. They are VM and RF flags.

VM - *Virtual Mode Flag*: If this flag is set, the 80386 enters the virtual 8086 mode within the protection mode. This is to be set only when the 80386 is in protected mode. In this mode, if any privileged instruction is executed an exception 13 is generated. This bit can be set using IRET instruction or any task switch operation only in the protected mode.

***RF - Resume Flag*:** This flag is used with the debug register breakpoints. It is checked at the starting of every instruction cycle and if it is set, any debug fault is ignored during the instruction cycle. The RF is automatically reset after successful execution of every instruction, except for IRET and POPF instructions.

Also, it is not automatically cleared after the successful execution of JMP, CALL and INT instruction causing a task switch. These instructions are used to set the RF to the value specified by the memory data available at the stack.

***Segment Descriptor Registers*:**

This registers are not available for programmers, rather they are internally used to store the descriptor information, like attributes, limit and base addresses of segments.

The six segment registers have corresponding six 73-bit descriptor registers. Each of them contains 32-bit base address, 32-bit base limit and 9 bit attributes.

These are automatically loaded when the corresponding segments are loaded with selectors.

***Control Registers*:** The 80386 has three 32-bit control registers CR0, CR2 and CR3 to hold global machine status independent of the executed task. Load and store instructions are available to access these registers.

***System Address Registers*:** Four special registers are defined to refer to the descriptor tables supported by 80386.

***Debug and Test Registers*:** Intel has provided a set of 8 debug registers for hardware debugging. Out of these eight registers DR0 to DR7, two registers DR4 and DR5 are Intel reserved.

The initial four registers DR0 to DR3 store four program controllable breakpoint addresses, while DR6 and DR7 respectively hold breakpoint status and breakpoint control information.

Two more test register are provided by 80386 for page caching namely test control and test status register.

ADDRESSING MODES:

- ✓ The 80386 supports overall eleven addressing modes to facilitate efficient execution of higher level language programs.
- ✓ In case of all those modes, the 80386 can now have 32-bit immediate or 32- bit register operands or displacements.
- ✓ The 80386 has a family of scaled modes. In case of scaled modes, any of the index register values can be multiplied by a valid scale factor to obtain the displacement.
- ✓ The valid scale factor is 1, 2, 4 and 8.

The different scaled modes are as follows.

***Scaled Indexed Mode*:** Contents of an index register are multiplied by a scale factor that may be added further to get the operand offset.

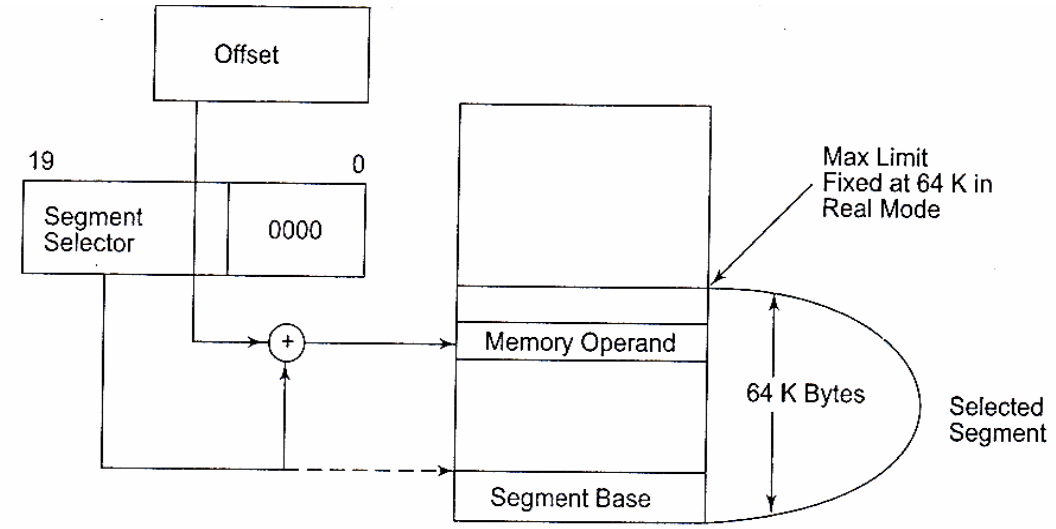
***Based Scaled Indexed Mode*:** Contents of an index register are multiplied by a scale factor and then added to base register to obtain the offset.

***Based Scaled Indexed Mode with Displacement*:** The Contents of an index register are multiplied by a scaling factor and the result is added to a base register and a displacement to get the offset of an operand.

Data Types:

- Bit
- Bit field
- Bit string
- Signed byte
- Unsigned byte
- Offset
- Pointer
- BCD
- Packed BCD
- Character
- Strings

Real Address Mode of 80386:



Physical Address Formation in Real Mode of 80386 (Intel Corp.)

- ✓ After reset, the 80386 starts from memory location FFFFFFF0H under the real address mode. In the real mode, 80386 works as a fast 8086 with 32-bit registers and data types.
- ✓ In real mode, the default operand size is 16 bit but 32- bit operands and addressing modes may be used with the help of override prefixes.
- ✓ The segment size in real mode is 64k, hence the 32-bit effective addressing must be less than 0000FFFFFH. The real mode initializes the 80386 and prepares it for protected mode.

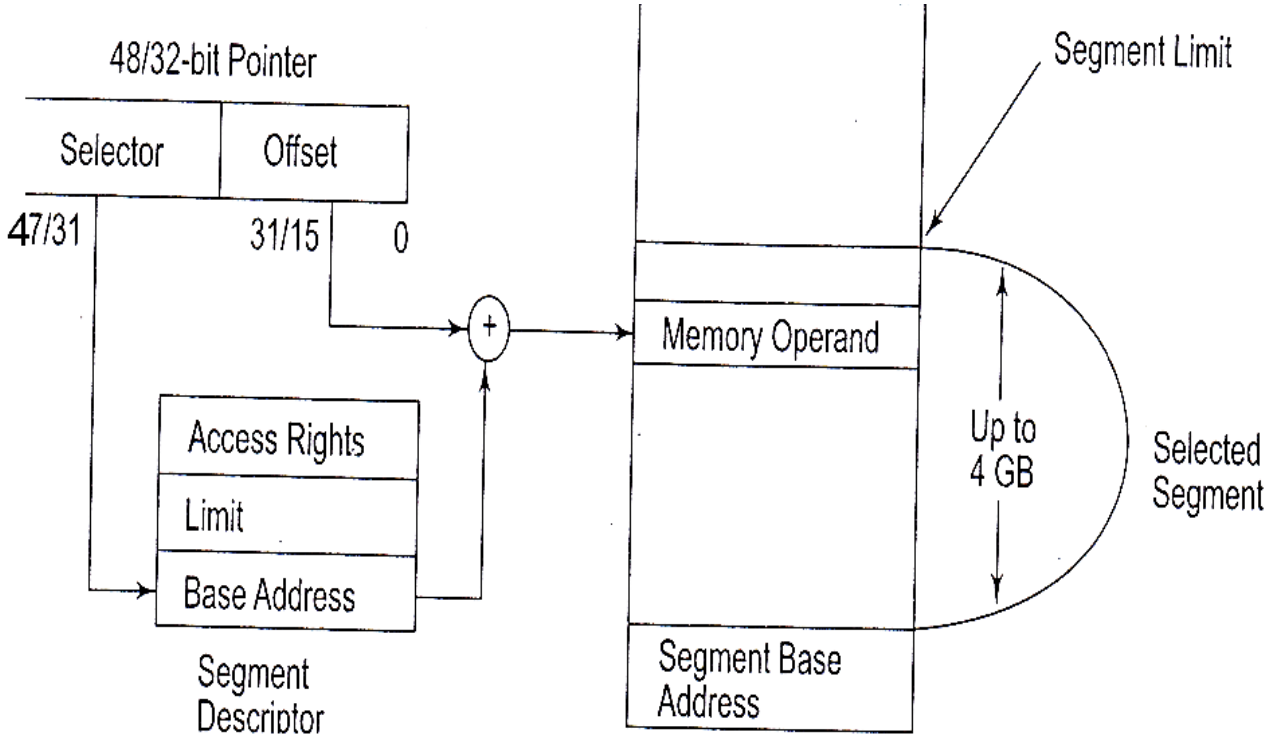
Memory Addressing in Real Mode:

In the real mode, the 80386 can address at the most1Mbytes of physical memory using address lines A0-A19.

- Paging unit is disabled in real addressing mode, and hence the real addresses are the same as the physical addresses.
- To form a physical memory address, appropriate segment registers contents (16-bits) are shifted left by four positions and then added to the 16-bit offset address formed using one of the addressing modes, in the same way as in the 80386-real address mode.
- The segment in 80386 real mode can be read, write or executed, i.e. no protection is available.
- Any fetch or access past the end of the segment limit generate exception 13 in real address mode.
- The segments in 80386 real mode may be overlapped or non-overlapped.
- The interrupt vector table of 80386 has been allocated 1Kbyte space starting from 00000H to 003FFH.

Protected Mode of 80386:

- All the capabilities of 80386 are available for utilization in its protected mode of operation.
- The 80386 in protected mode support all the software written for 80286 and 8086 to be executed under the control of memory management and protection abilities of 80386.
- The protected mode allows the use of additional instruction, addressing modes and capabilities of 80386.



Memory Addressing in Protected Mode:

In this mode, the contents of segment registers are used as selectors to address descriptors which contain the segment limit, base address and access rights byte of the segment.

- The effective address (offset) is added with segment base address to calculate linear address. This linear address is further used as physical address, if the paging unit is disabled, otherwise the paging unit converts the linear address into physical address.
- The paging unit is a memory management unit enabled only in protected mode. The paging mechanism allows handling of large segments of memory in terms of pages of 4Kbyte size.
- The paging unit operates under the control of segmentation unit. The paging unit if enabled converts linear addresses into physical address, in protected mode.

Segmentation:

- **Descriptor tables:** These descriptor tables and registers are manipulated by the operating system to ensure the correct operation of the processor, and hence the correct execution of the program.

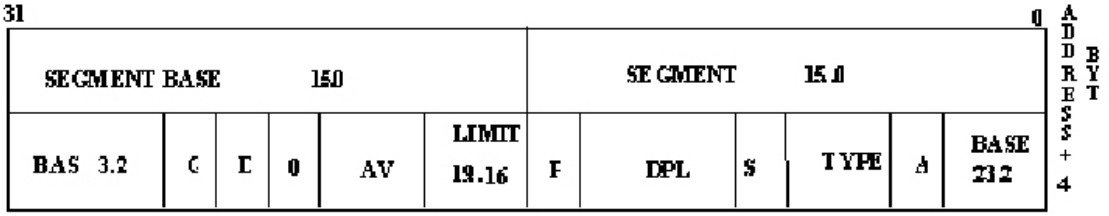
  Three types of the 80386 descriptor tables are listed as follows:

  - GLOBAL DESCRIPTOR TABLE (GDT)
  - LOCAL DESCRIPTOR TABLE (LDT)
  - INTERRUPT DESCRIPTOR TABLE (IDT)

- **Descriptors:** The 80386 descriptors have a 20-bit segment limit and 32-bit segment address. The descriptor of 80386 are 8-byte quantities access right or attribute bits along with the base and limit of the segments.

- **Descriptor Attribute Bits:** The A (accessed) attributed bit indicates whether the segment has been accessed by the CPU or not.

  - The TYPE field decides the descriptor type and hence the segment type.
  - The S bit decides whether it is a system descriptor (S=0) or code/data segment descriptor (S=1).
  - The DPL field specifies the descriptor privilege level.
  - The D bit specifies the code segment operation size. If D=1, the segment is a 32-bit operand segment, else, it is a 16-bit operand segment.
  - The P bit (present) signifies whether the segment is present in the physical memory or not. If P=1, the segment is present in the physical memory.
  - The G (granularity) bit indicates whether the segment is page addressable. The zero bit must remain zero for compatibility with future process.
  - The AVL (available) field specifies whether the descriptor is for user or for operating system.



Structure of a Descriptor

BASE Base Address of the segment
LIMIT The length of the segment
P Present Bit - 1=Present ,0 = not present
S Segment Descriptor -0 = System Descriptor,
1 = Code or data segment descriptor
TYPE Type of segment
G Granularity Bit - 1 = Segment length is page granular ,
0 = Segment length is byte granular
D Default Operation size
0 Bit must be zero
AVL Available field for user or OS

The 80386 has five types of descriptors listed as follows:

1.Code or Data Segment Descriptors.

2.System Descriptors.

3.Local descriptors.

4.TSS (Task State Segment) Descriptors.

5.GATE Descriptors.

Paging:

Paging Operation:

Paging is one of the memory management techniques used for virtual memory multitasking operating system.

- The segmentation scheme may divide the physical memory into a variable size segments but the paging divides the memory into a fixed size pages.
- The segments are supposed to be the logical segments of the program, but the pages do not have any logical relation with the program.

- The pages are just fixed size portions of the program module or data.
- The advantage of paging scheme is that the complete segment of a task need not be in the physical memory at any time.
- Only a few pages of the segments, which are required currently for the execution need to be available in the physical memory. Thus, the memory requirement of the task is substantially reduced, relinquishing the available memory for other tasks.
- Whenever the other pages of task are required for execution, they may be fetched from the secondary storage.
- The previous page which are executed, need not be available in the memory, and hence the space occupied by them may be relinquished for other tasks.
- Thus, paging mechanism provides an effective technique to manage the physical memory for multitasking systems.

Paging Unit:

The paging unit of 80386 uses a two-level table mechanism to convert a linear address provided by segmentation unit into physical addresses.

- The paging unit converts the complete map of a task into pages, each of size 4K. The task is further handled in terms of its page, rather than segments.
- The paging unit handles every task in terms of three components namely page directory, page tables and page itself.

Paging Descriptor Base Register:

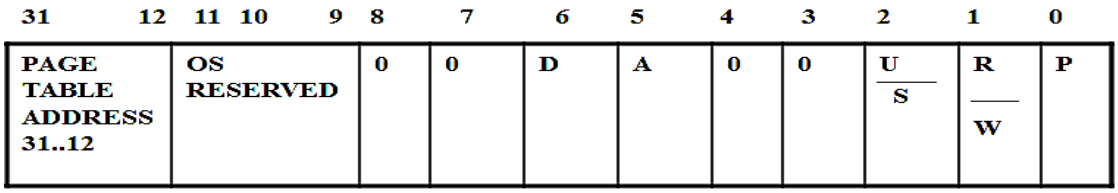
The control register CR2 is used to store the 32-bit linear address at which the previous page fault was detected.

- The CR3 is used as page directory physical base address register, to store the physical starting address of the page directory.
- The lower 12 bit of the CR3 are always zero to ensure the page size aligned directory. A move operation to CR3 automatically loads the page table entry caches and a task switch operation, to load CR0 suitably.

Page Directory*:*

This is at the most 4Kbytes in size. Each directory entry is of 4 bytes, thus a total of 1024 entries are allowed in a directory. The upper 10 bits of the linear address are used as an index to the corresponding page directory entry. The page directory entries point to page tables.

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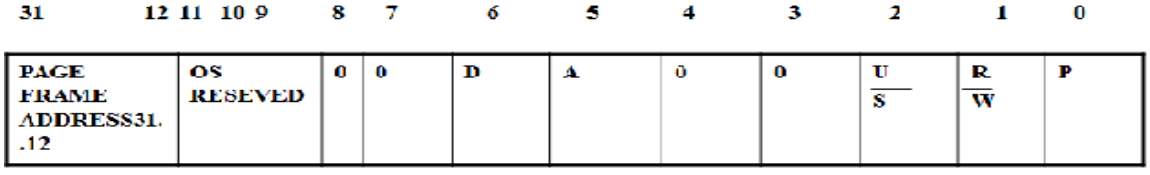
Page Directory Entry

Page Tables:

Each page table is of 4Kbytes in size and many contain a maximum of 1024 entries. The page table entries contain the starting address of the page and the statistical information about the page.

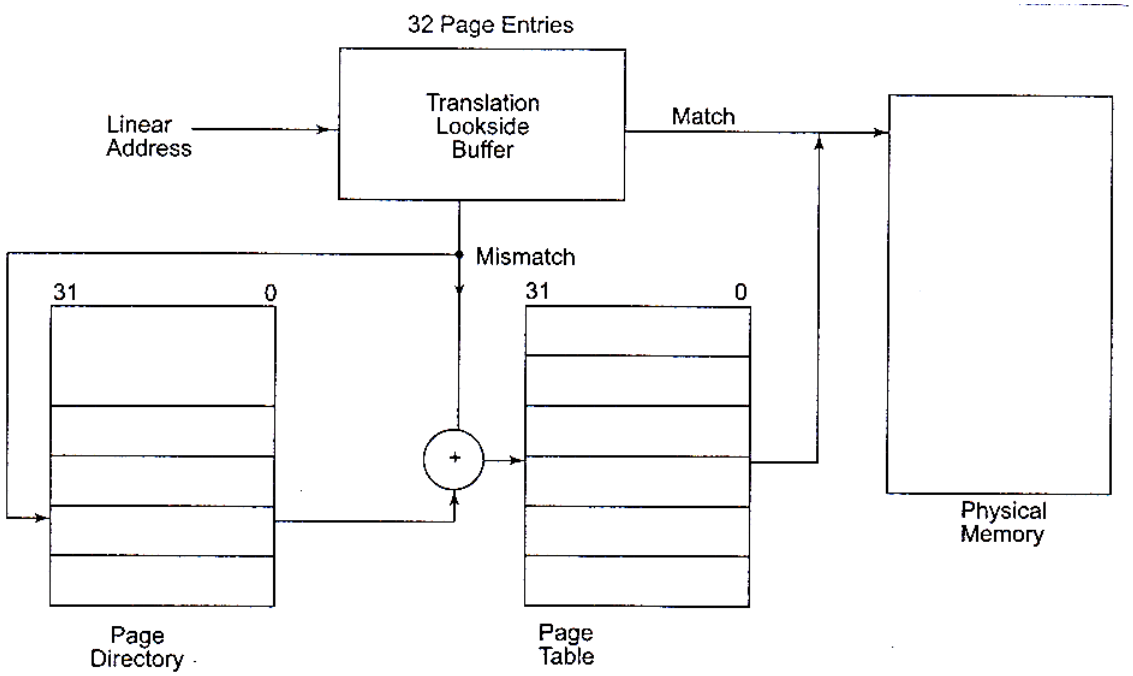
- The upper 20-bit page frame address is combined with the lower 12 bit of the linear address. The address bits A12- A21 are used to select the 1024-page table entries. The page table can be shared between the tasks.
- The P bit of the above entries indicate, if the entry can be used in address translation.

  If P=1, the entry can be used in address translation, otherwise it cannot be used.
- The P bit of the currently executed page is always high.
- The accessed bit A is set by 80386 before any access to the page. If A=1, the page is accessed, else un-accessed.
- The D bit (Dirty bit) is set before a write operation to the page is carried out. The D-bit is undefined for page director entries.
- The OS reserved bits are defined by the operating system software.
- The User / Supervisor (U/S) bit and read/write bit are used to provide protection. These bits are decoded to provide protection under the 4-level protection model.
- The level 0 is supposed to have the highest privilege, while the level 3 is supposed to have the least privilege.
- This protection provide by the paging unit is transparent to the segmentation unit.



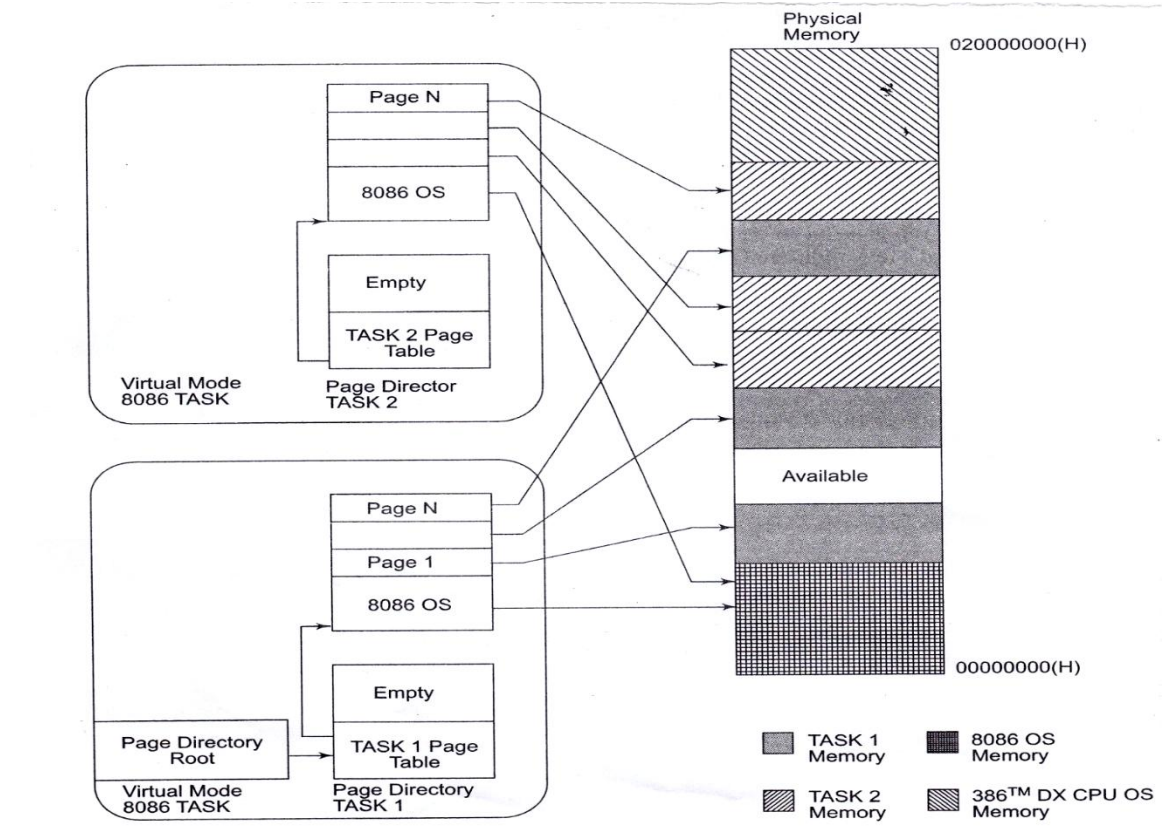
Page Table Entry

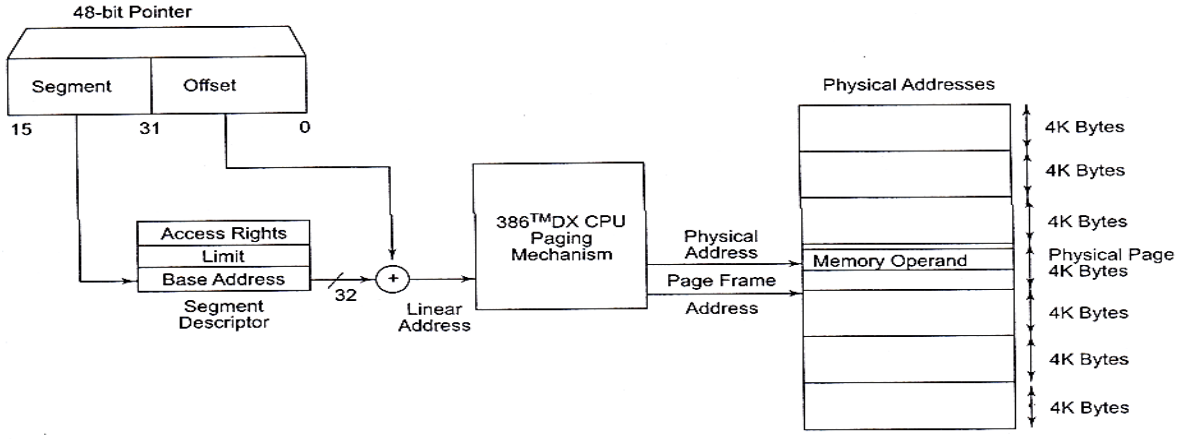
Virtual 8086 mode:



Paging Operation with TLB (Intel Corp.)

- ✓ In its protected mode of operation, 80386DX provides a virtual 8086 operating environments to execute the 8086 programs.
- ✓ The real mode can also use to execute the 8086 programs along with the capabilities of 80386, like protection and a few additional instructions.
- ✓ Once the 80386 enters the protected mode from the real mode, it cannot return back to the real mode without a reset operation.
- ✓ Thus, the virtual 8086 mode of operation of 80386, offers an advantage of executing 8086 programs while in protected mode.
- ✓ The address forming mechanism in virtual 8086 mode is exactly identical with that of 8086 real mode.
- ✓ In virtual mode, 8086 can address 1Mbytes of physical memory that may be anywhere in the 4Gbytes address space of the protected mode of 80386.
- ✓ Like 80386 real mode, the addresses in virtual 8086 mode lie within 1Mbytes of memory.
- ✓ In virtual mode, the paging mechanism and protection capabilities are available at the service of the programmers.
- ✓ The 80386 supports multiprogramming, hence more than one programmer may be use the CPU at a time.





Paging Unit Enabled in Protected Mode Addressing (Intel Corp.)