8251 – USART
(Universal Synchronous Asynchronous Receiver & Transmitter)

8251 is a USART (Universal Synchronous and Asynchronous Receiver and Transmitter) compatible with Intel's processors. This chip converts the parallel data into a serial stream of bits suitable for serial transmission. It is also able to receive a serial stream of bits and convert it into parallel data bytes to be read by a microprocessor.

Basic Modes of data transmission

a) Simplex

b) Half Duplex

c) Duplex

a) Simplex mode

Data is transmitted only in one direction over a single communication channel. For example, the processor may transmit data for a CRT display unit in this mode.

Ex:- radio station, earthquake sensor

b) Half Duplex mode

In this mode, data transmission may take place in either direction, but at a time data may be transmitted only in one direction. A computer may communicate with a terminal in this mode. It is not possible to transmit data from the computer to the terminal and terminal to computer simultaneously.

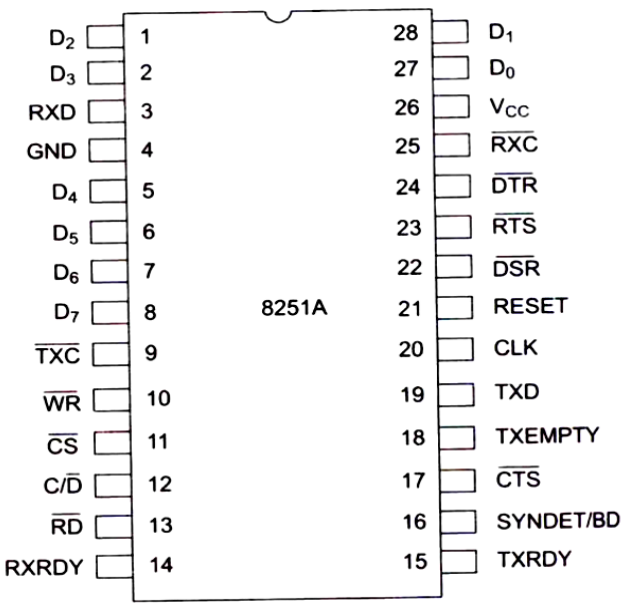
Ex:- walky-talky, push to talk (PTT) devices

c) Duplex Mode

In duplex mode, data may be transferred between two transreceivers in both directions simultaneously.

Ex:- phone conversation.

Signal Description of 8251:



D0 – D7: This is an 8-bit data bus used to read or write status, command word or data from or to the 8251A.

C / D: (Control Word/Data): This input pin, together with RD and WR inputs, informs the 8251A that the word on the data bus is either a data or control word/status information. If this pin is 1, control / status is on the bus, otherwise data is on the bus.

RD: This active-low input to 8251A is used to inform it that the CPU is reading either data or status information from its internal registers. This active-low input to 8251A is used to inform it that the CPU is writing data or control word to 8251A.

WR: This is an active-low chip select input of 825lA. If it is high, no read or write operation can be carried out on 8251. The data bus is tri-stated if this pin is high.

CLK: This input is used to generate internal device timings and is normally connected to clock generator output. This input frequency should be at least 30 times greater than the receiver or transmitter data bit transfer rate.

RESET: A high on this input forces the 8251A into an idle state. The device will remain idle till this input signal again goes low and a new set of control word is written into it. The minimum required reset pulse width is 6 clock states, for the proper reset operation.

TXC (Transmitter Clock Input): This transmitter clock input controls the rate at which the character is to be transmitted. The serial data is shifted out on the successive negative edge of the TXC.

TXD (Transmitted Data Output): This output pin carries serial stream of the transmitted data bits along with other information like start bit, stop bits and parity bit, etc.

RXC **(Receiver Clock Input):** This receiver clock input pin controls the rate at which the character is to be received.

RXD (Receive Data Input): This input pin of 8251A receives a composite stream of the data to be received by 8251 A.

RXRDY (Receiver Ready Output): This output indicates that the 8251A contains a character to be read by the CPU.

TXRDY - Transmitter Ready: This output signal indicates to the CPU that the internal circuit of the transmitter is ready to accept a new character for transmission from the CPU.

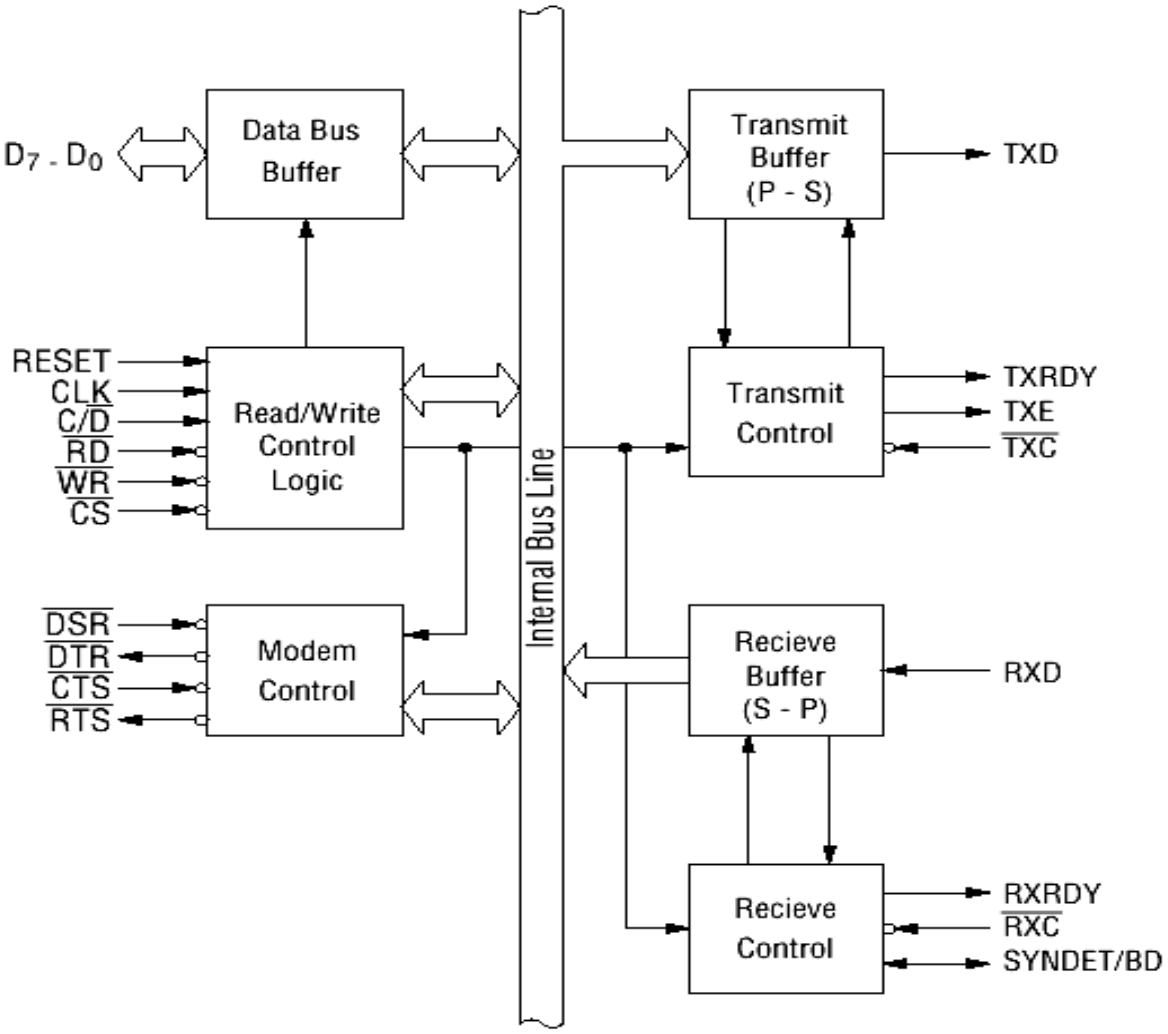
DSR **- Data Set Ready:** This is normally used to check if data set is ready when communicating with a modem.

DTR - **Data Terminal Ready:** This is used to indicate that the device is ready to accept data when the 8251 is communicating with a modem.

RTS - **Request to Send Data:** This signal is used to communicate with a modem.

TXE- Transmitter Empty: The TXE signal can be used to indicate the end of a transmission mode.

Internal Architecture of 8251A:



The data buffer interfaces the internal bus of the circuit with the system bus. The read / write control logic controls the operation of the peripheral depending upon the operations initiated by the CPU. C / decides whether the address on internal data bus is control address / data address. The modem control unit handles the modem handshake signals to coordinate the communication between modem and USART. The transmit control unit transmits the data byte received by the data buffer from the CPU for serial communication. The transmission rate is controlled by the input frequency. Transmit control unit also derives two transmitter status signals namely TXRDY and TXEMPTY which may be used by the CPU for handshaking. The transmit buffer is a parallel to serial converter that receives a parallel byte for conversion into a serial signal for further transmission.

The receive control unit decides the receiver frequency as controlled by the RXC input frequency. The receive control unit generates a receiver ready (RXRDY) signal that may be used by the CPU for handshaking. This unit also detects a break in the data string while the 8251 is in asynchronous mode. In synchronous mode, the 8251 detects SYNC characters using SYNDET/BD pin.

Operating Modes of 8251:

1. Asynchronous mode
2. Synchronous mode

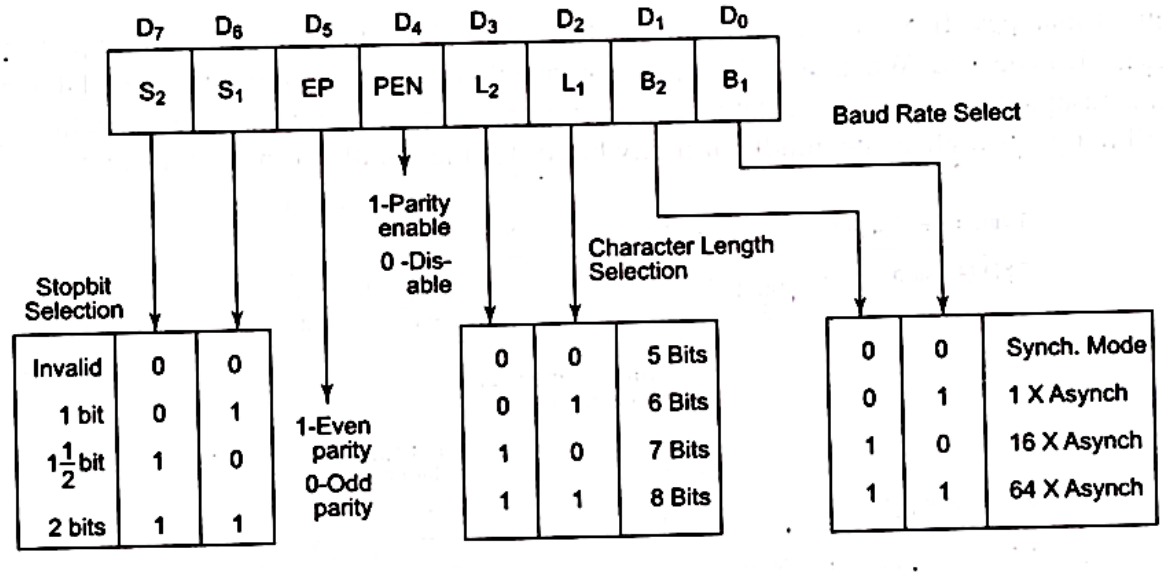
Asynchronous Mode (Transmission)

When a data character is sent to 8251A by the CPU, it adds start bits prior to the serial data bits, followed by optional parity bit and stop bits using the asynchronous mode instruction control word format. This sequence is then transmitted using TXD output pin on the falling edge of TXC.

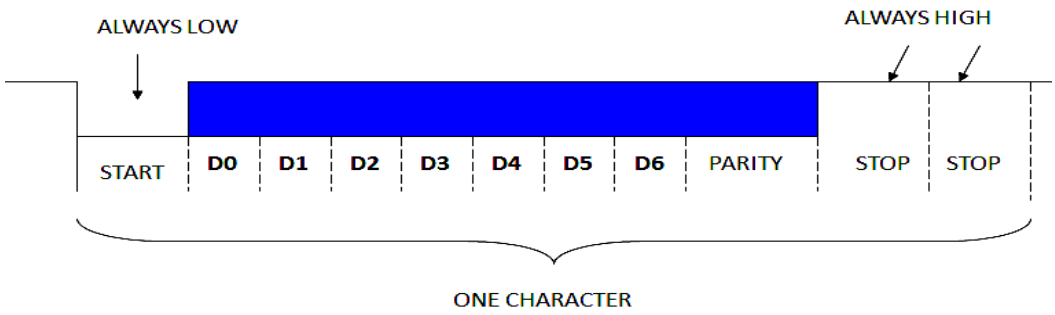
Asynchronous Mode (Receive)

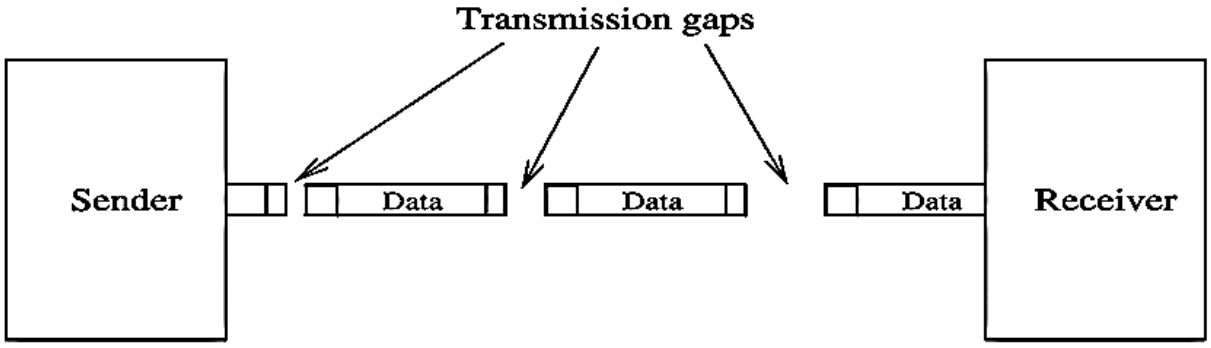
A falling edge on RXD input line marks a start bit. The receiver requires only one stop bit to mark end of the data bit string, regardless of the stop bit programmed at the transmitting end. The 8-bit character is then loaded into the into parallel I/O buffer of 8251. RXRDY pin is raised high to indicate to the CPU that a character is ready for it. If the previous character has not been read by the CPU, the new character replaces it, and the overrun flag is set indicating that the previous character is lost.

Mode instruction format for Asynchronous mode

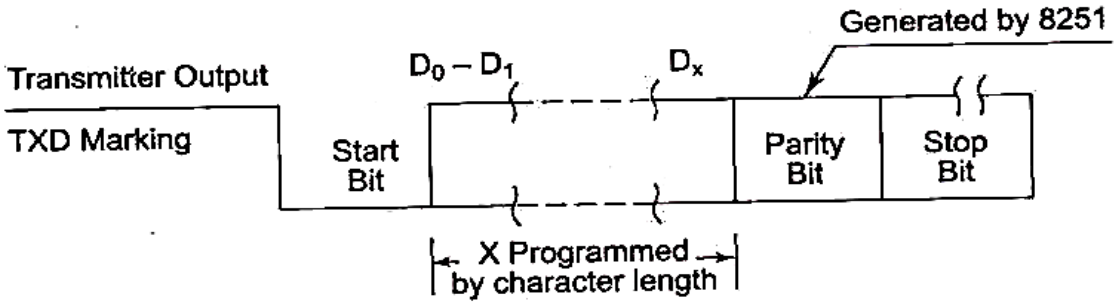


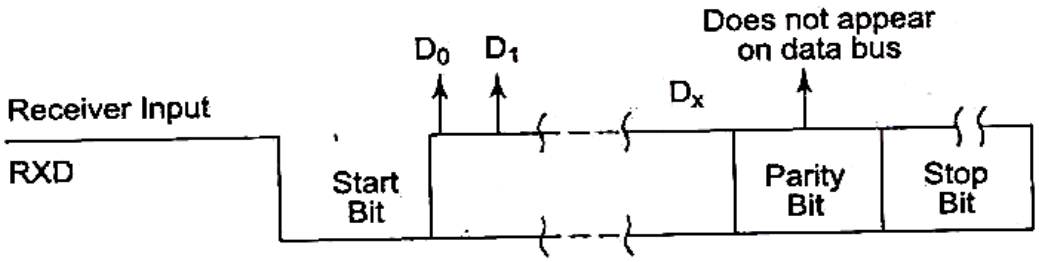
Asynchronous Mode Transmit and Receive Formats



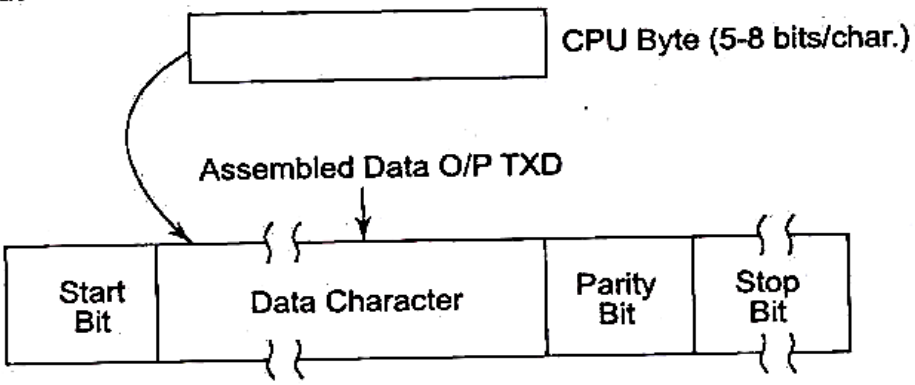


(a) Asynchronous transmission

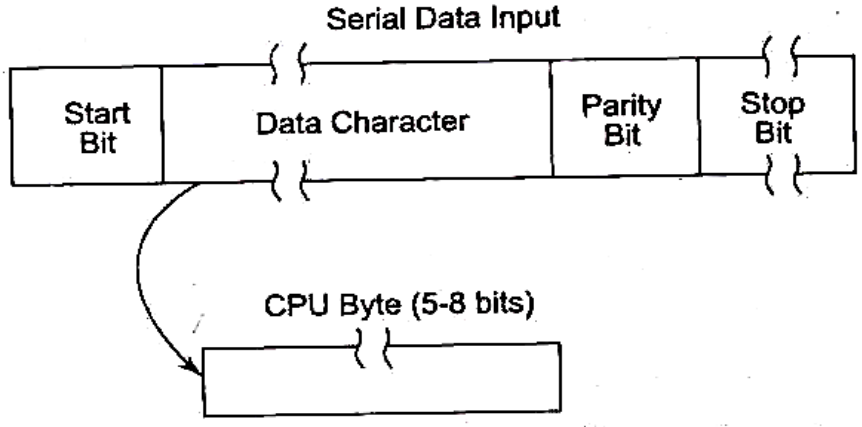




Transmission Format



Receive Format



Synchronous Mode (Transmission)

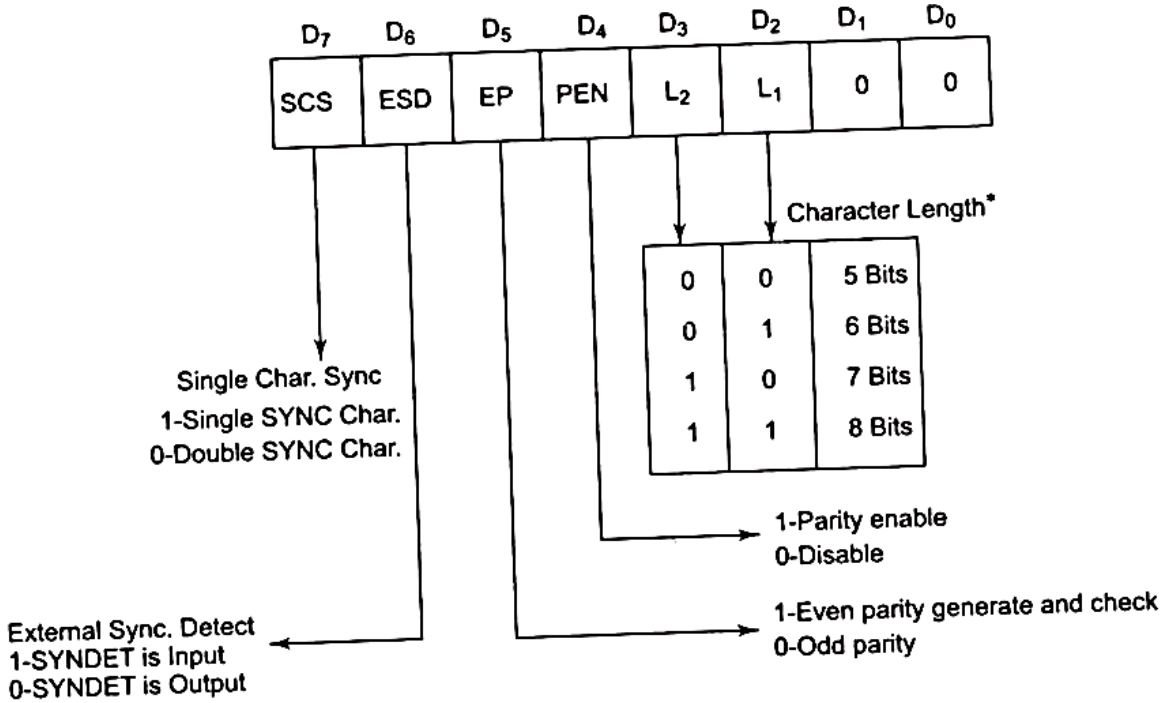
The TXD output is high until the CPU sends a character to 8251 which usually is a SYNC character. When CTS line goes low, the first character is serially transmitted out. Characters are shifted out on the falling edge of TXC. Data is shifted out at the same rate as TXC, over TXD output line. If the CPU buffer becomes empty, the SYNC character or characters are inserted in the data stream over TXD output.

Synchronous Mode (Receiver)

In this mode, the character synchronization can be achieved internally or externally. The data on RXD pin is sampled on rising edge of the RXC. The content of the receiver buffer is compared with the first SYNC character at every edge until it matches. If 8251 is programmed for two SYNC characters, the subsequent received character is also checked. When the characters match, the hunting stops.

The SYNDET pin set high and is reset automatically by a status read operation. In the external SYNC mode, the synchronization is achieved by applying a high level on the SYNDET input pin that forces 8251 out of HUNT mode. The high level can be removed after one RXC cycle. The parity and overrun error both are checked in the same way as in asynchronous mode.

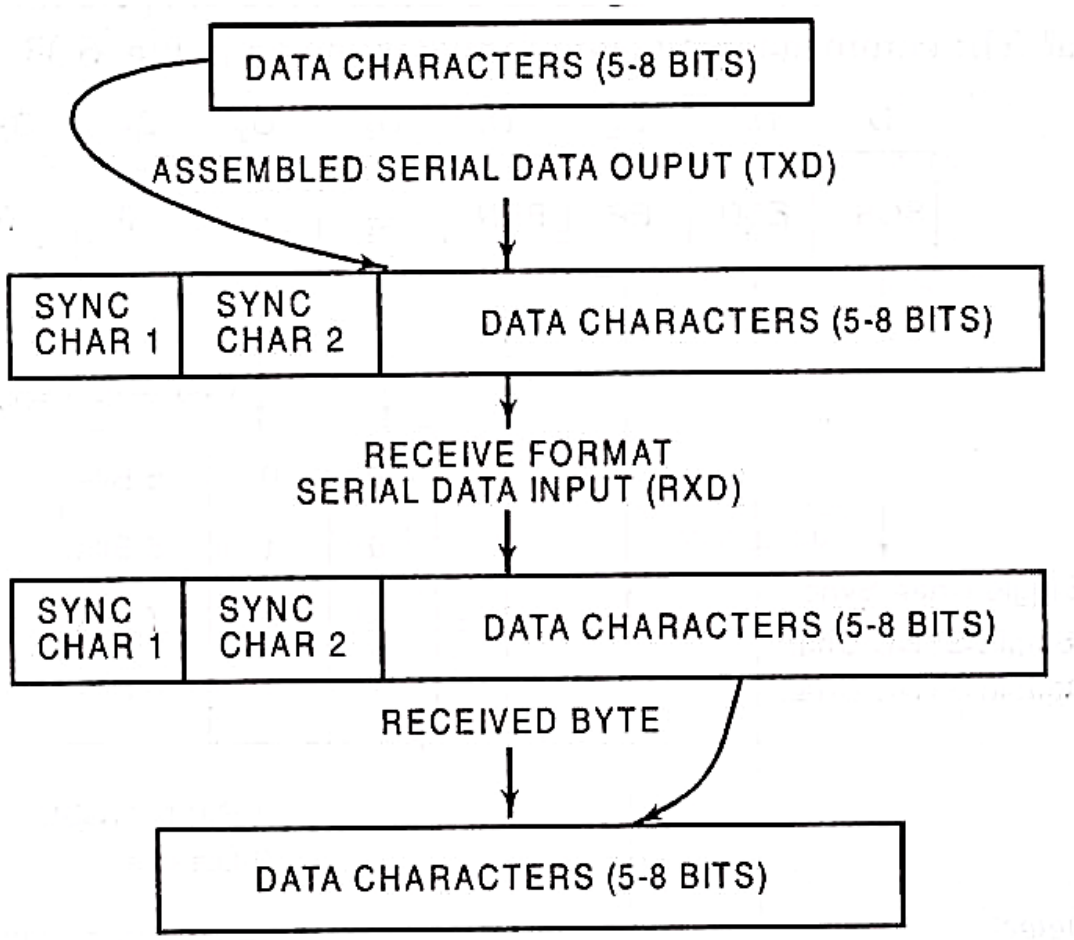
Synchronous Mode Instruction Format



Synchronous mode Transmit and Receive data format



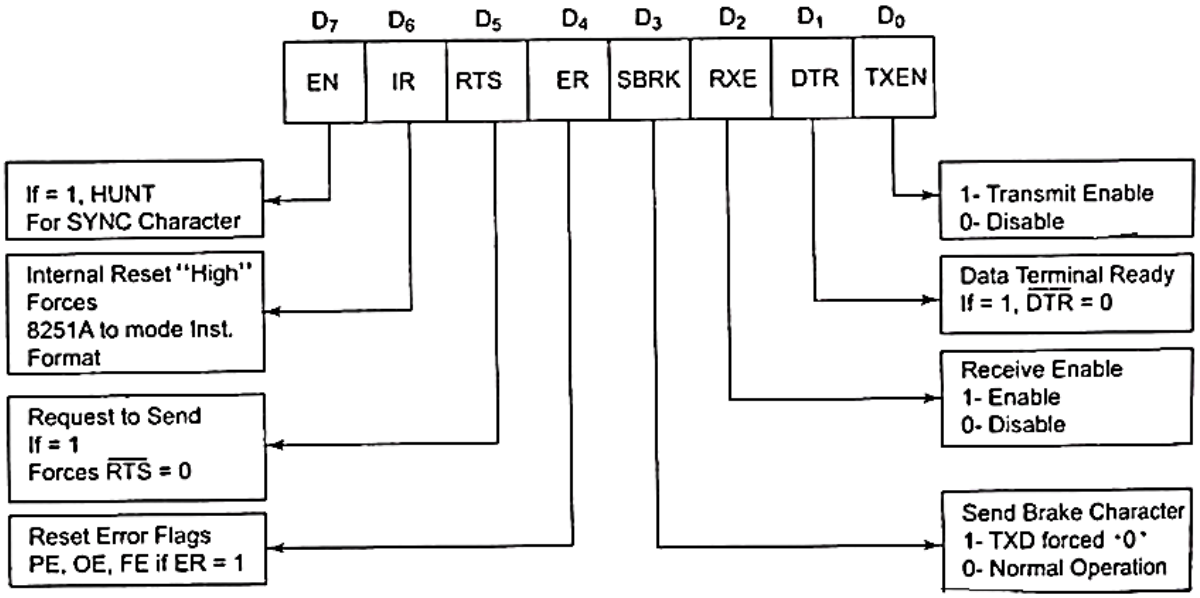
(b) Synchronous transmission



Command Instruction Definition

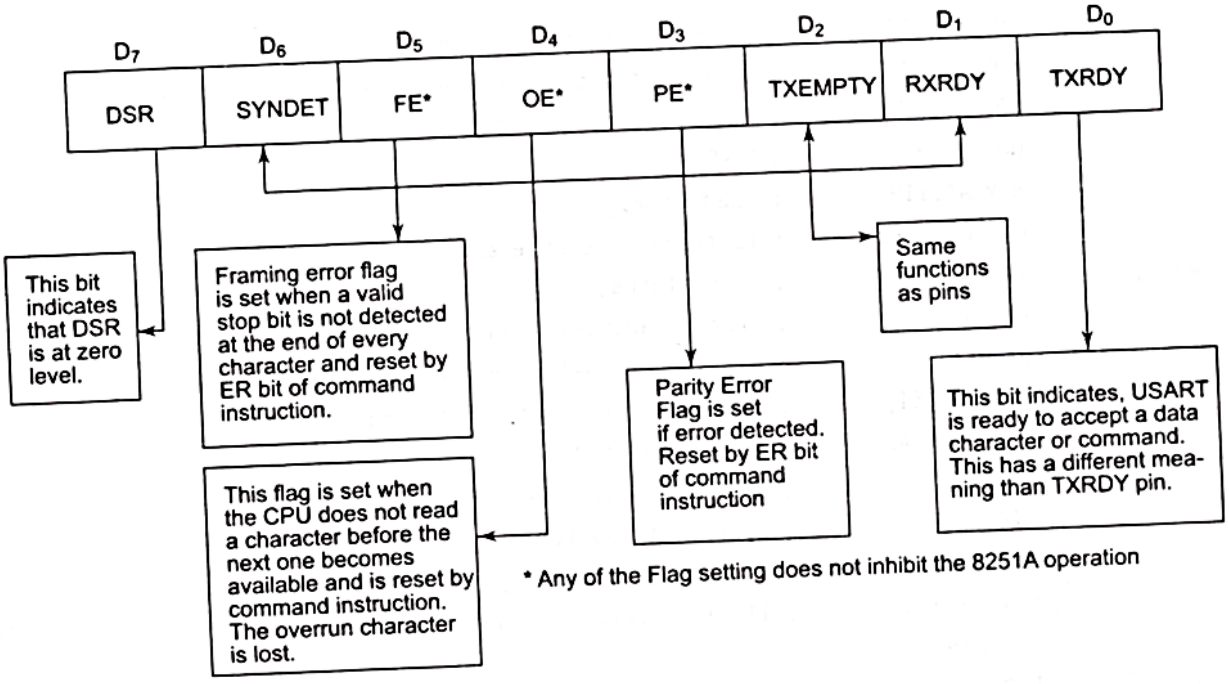
The command instruction controls the actual operations of the selected format like enable transmit/receive, error reset and modem control. A reset operation returns 8251 back to mode instruction format.

Command Instruction format



Status Read Definition

This definition is used by the CPU to read the status of the active 8251 to confirm if any error condition or other conditions like the requirement of processor service has been detected during the operation.



Interfacing 8251 with 8086:

Design the hardware interface circuit for interfacing 8251 with 8086. Set the 8251 in asynchronous mode as a transmitter and receiver with even parity enabled, 2 stop bits, 8-bit character length, frequency 160 kHz and baud rate 10 K.

(a) Write an ALP to transmit 100 bytes of data string starting at location 2000:5000H.

(b) Write an ALP to receive 100 bytes of data string and store it at 3000:4000H.

Solution:

Asynchronous mode control word for transmitting 100 bytes of data:

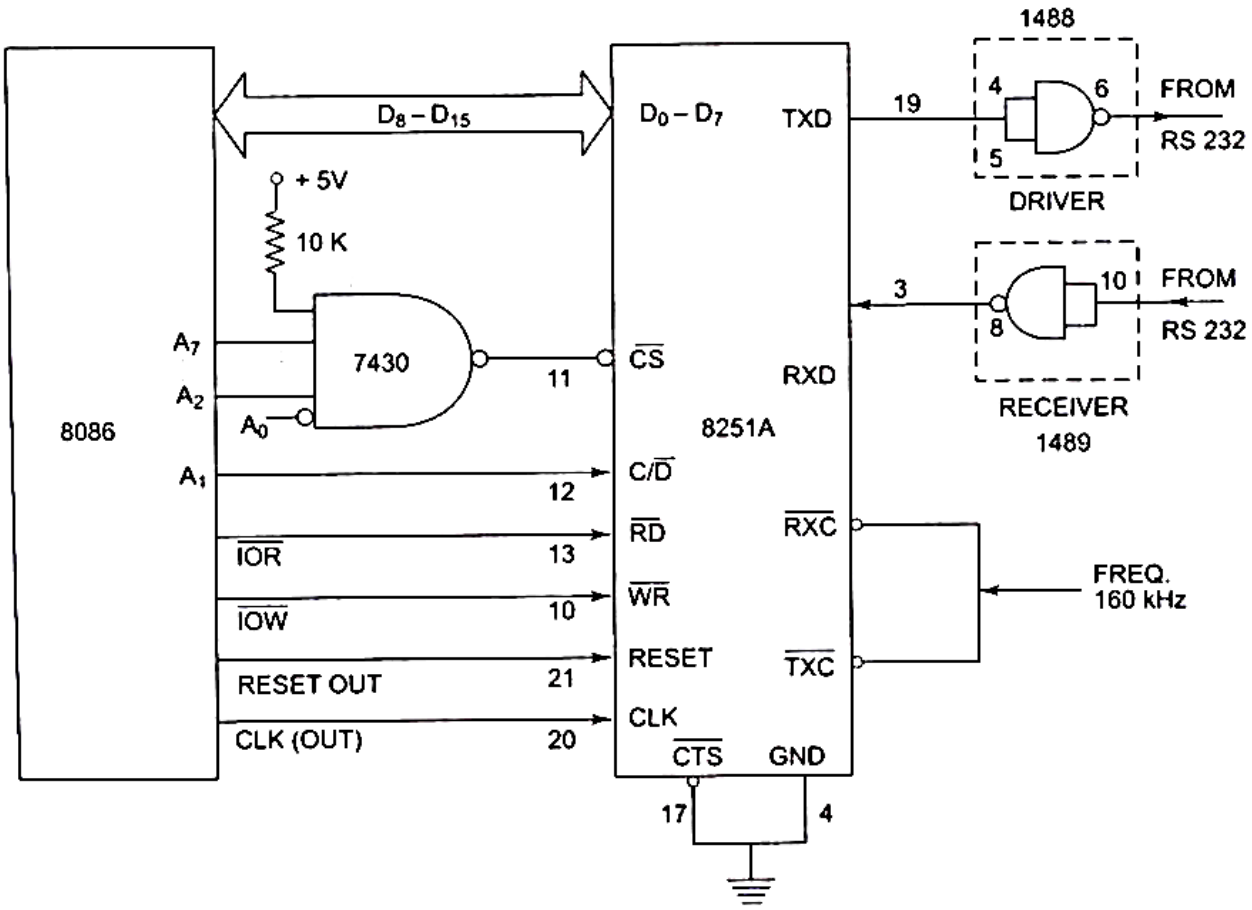
D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	0 = FEH
2 Stop bits		Even Parity Enabled		8-bit format		CLK scaled	

a) ALP to initialize 8251 and transmit 100 bytes of data

```
        ASSUME CS: CODE
        CODE SEGMENT
    START: MOV AX, 2000H
           MOV DS, AX      ; DS points to byte string segment
           MOV SI, 5000H   ; SI points to byte string
           MOV CL, 64H     ; Length of string in CL (hex)
           MOV AL, 0FEH    ; Mode control word to D0 – D7
           OUT 0FEH, AL
           MOV AX, 11H     ; Load command word
           OUT 0FE, AL     ; to transmit enables and error reset
     WAIT: IN AL, 0FEH     ; Read status
           AND AL, 01H     ; Check transmitter enable
           JZ WAIT         ; bit, if zero wait for the transmitter to be ready
           MOV AL, [SI]    ; If ready, first byte of string data is transmitted
           OUT 0FCH, AL
           INC SI          ; Point to next byte
           DEC CL          ; Decrement counter
           JNZ WAIT        ; If CL is not zero, go for next byte
           MOV AH, 4CH
           INT 21H
        CODE ENDS
            END START
```

b) An ALP to initialize 8251 and receive 100 bytes of data

```
ASSUME CS: CODE
        CODE SEGMENT
            START: MOV AX, 3000H
                   MOV DS, AX       ; Data segment set to 3000H
                   MOV SI, 4000H    ; Pointer to destination offset
                   MOV CL, 64H      ; Byte count in CL
                   MOV AL, 7EH      ; Only one stop bit for
                   OUT OFEH, AL     ; receiver is set
                   MOV AL, 14H      ; Load command word to enable
                   OUT 0FEH, AL     ; the receiver and disable transmitter
          NXTBT: IN AL, OFEH        ; Read status
                   AND AL, 38H      ; Check FE, OE and PE
                   JZ READY         ; If zero, jump to READY
                   MOV AL, 14H      ; If not zero, clear them
                   OUT OFEH, AL
          READY: IN AL, 0FEH        ; Check RXRDY, if receiver is not ready
                   AND AL, 02H
                   JZ READY         ; wait
                   IN AL, 0FCH      ; If it is ready,
                   MOV [SI], AL     ; receive the character
                   INC SI           ; Increment pointer to next byte
                   DEC CL           ; Decrement counter
                   JNZ NXTBT        ; Repeat, if CL is not zero
                   MOV AH, 4CH
                   INT 21H
        CODE ENDS
            END START
```



Interfacing 8251 with 8086

DMA Controller 8257

The Intel 8257 is a 4-channel **Direct Memory Access** (DMA) controller. It is specifically designed to simplify the transfer of data at high speeds for the Intel® microcomputer systems. Its primary function is to generate, upon a peripheral request, a sequential memory address which will allow the peripheral to read or write data directly to or from memory. Acquisition of the system bus in accomplished via the CPU's hold function.

The 8257 has priority logic that resolves the peripherals requests and issues a composite hold request to the CPU. It maintains the DMA cycle count for each channel and outputs a control signal Jo notify the peripheral that the programmed number of DMA cycles is complete. Other output control signals simplify sectored data transfers. The 8257 represents a significant savings in component count for DMA-based microcomputer systems and greatly simplifies the transfer of data at high speed between peripherals and memories.

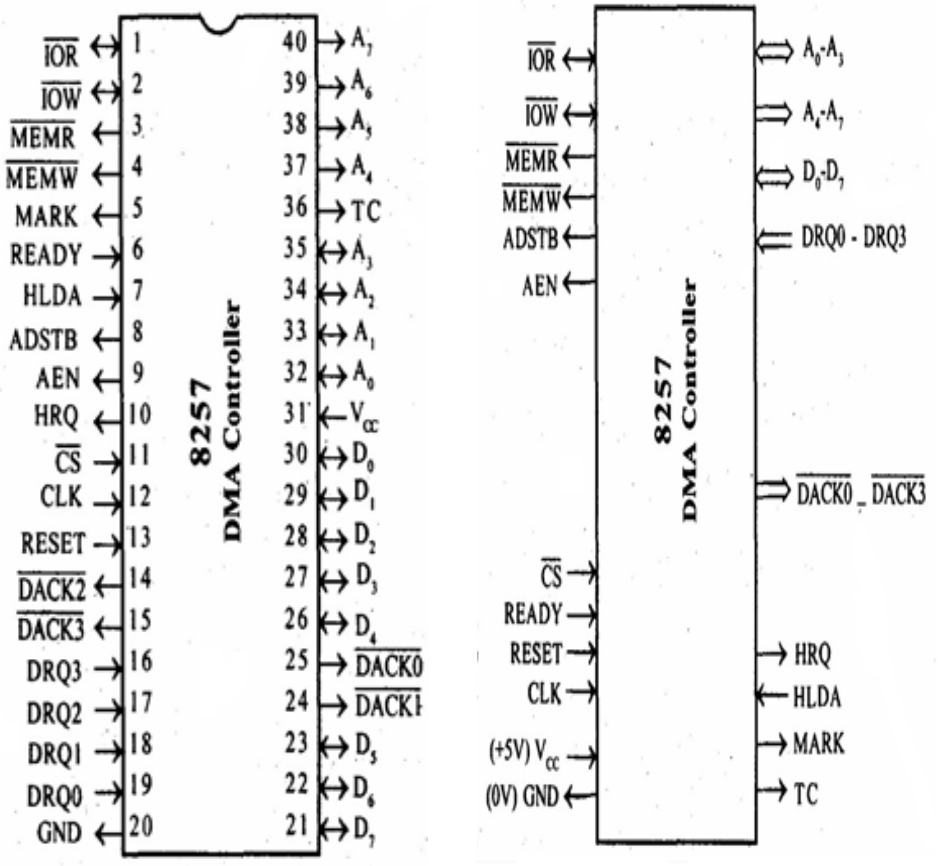
8257 features:

It is a device to transfer the data directly between IO device and memory without the CPU. So it performs a high-speed data transfer between memory and I/O device.

The features of 8257 are:

1. The 8257 has four channels and so it can be used to provide DMA to four I/O devices
2. Each channel can be independently programmable to transfer up to 64kb of data by DMA.
3. Each channel can be independently perform read transfer, write transfer and verify transfer.

Pin diagram 8257:



DRQo-DRQ3:
These are the four individual channel DMA request inputs, used by the peripheral devices for requesting the DMA services. The DRQo has the highest priority while DRQ**3** has the lowest one, if the fixed priority mode is selected.

DACKo-DACK3:
These are the active-low DMA acknowledge output lines which inform the requesting peripheral that the request has been honoured and the bus is relinquished by the CPU. These lines may act as strobe lines for the requesting devices.

Do-D7:
- These are bidirectional, data lines used to interface the system bus with the internal data bus of 8257.
- These lines carry command words to 8257 and status word from 8257, in slave mode, i.e. under the control of CPU. The data over these lines may be transferred in both the directions. When the 8257 is the bus master (master mode, i.e. not under CPU control), it uses Do-D7 lines to send higher byte of the generated address to the latch.
- This address is further latched using ADSTB signal. the address is transferred over Do-D7 during the first clock cycle of the DMA cycle. During the rest of the period, data is available on the data bus.

IOR:
This is an active-low bidirectional tristate input line that acts as an input in the slave mode. In slave mode, this input signal is used by the CPU to read internal registers of 8257.this line acts output in master mode. In master mode, this signal is used to read data from a peripheral during a memory write cycle.

IOW:
This is an active low bidirection tristate line that acts as input in slave mode to load the contents of the data bus to the 8-bit mode register or upper/lower byte of a 16-bit DMA address register or terminal count register. In the master mode, it is a control output that loads the data to a peripheral during DMA memory read cycle (write to peripheral).

CLK:
This is a clock frequency input required to derive basic system timings for the internal operation of 8257.

RESET:
This active-high asynchronous input disables all the DMA channels by clearing the mode register and tristates all the control lines.

Ao-A3:
These are the four least significant address lines. In slave mode, they act as input which select one of the registers to be read or written. In the master mode, they are the four least significant memory address output lines generated by 8257.

CS:
This is an active-low chip select line that enables the read/write operations from/to 8257, in slave mode. In the master mode, it is automatically disabled to prevent the chip from getting selected (by CPU) while performing the DMA operation.

A4-A7:
This is the higher nibble of the lower byte address generated by 8257 during the master mode of DMA operation.

READY:
This is an active-high asynchronous input used to stretch memory read and write cycles of 8257 by inserting wait states. This is used while interfacing slower peripherals..

HRQ:
- The hold request output requests the access of the system bus.
- In the non-cascaded 8257 systems, this is connected with HOLD pin of CPU.
- In the cascade mode, this pin of a slave is connected with a DRQ input line of the master 8257, while that of the master is connected with HOLD input of the CPU.

HLDA:
The CPU drives this input to the DMA controller high, while granting the bus to the device. This pin is connected to the HLDA output of the CPU. This input, if high, indicates to the DMA controller that the bus has been granted to the requesting peripheral by the CPU.

MEMR: This active –low memory read output is used to read data from the addressed memory locations during DMA read cycles.

MEMW: This active-low three state output is used to write data to the addressed memory location during DMA write operation.

ADST: This output from 8257 strobes the higher byte of the memory address generated by the DMA controller into the latches.

AEN: This output is used to disable the system data bus and the control the bus driven by the CPU, this may be used to disable the system address and data bus by using the enable input of the bus drivers to inhibit the non-DMA devices from responding during DMA operations. If the 8257 is I/O mapped, this should be used to disable the other I/O devices, when the DMA controller addresses is on the address bus.

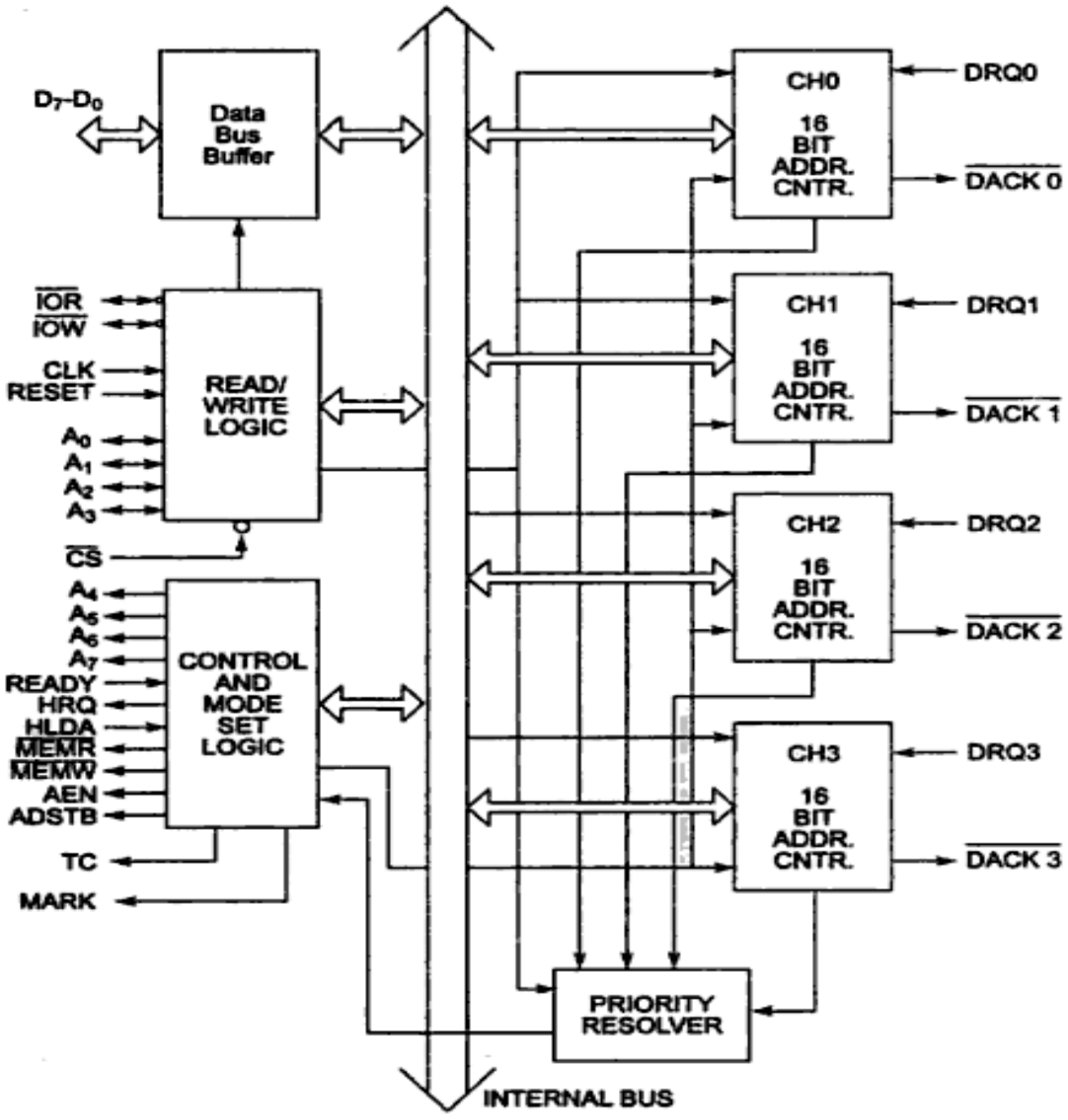
TC:
- Terminal count output indicates to the currently selected peripherals that the present DMA cycle is the last for the previously programmed data block.
- If the TC STOP bit in the mode set register is set, the selected channel will be disabled at the end of the DMA cycle.
- The TC pin is activated when the 14-bit content of the terminal count register of the selected channel becomes equal to zero.
- The lower order 14 bits of the terminal count register are to be programmed with a 14-bit equivalent of (n-1), if n is the desired number of DMA cycles.

MARK:
The modulo 128 mark output indicates to the selected peripheral that the current DMA cycle is the 128th cycle since the previous MARK output. The mark will be activated after each 128 cycles or integral multiples of it from the beginning if the data block (the first DMA cycle), if the total number of the required DMA cycles (n) is completely divisible by 128.

Vcc:
This is a +5v supply pin required for operation of the circuit.

GND:
This is a return line for the supply (ground pin of the IC).

Functional Block Diagram of 8257:



Internal Architecture of 8257

The functional blocks of 8257 are **data bus buffer**, **read/write logic**, **control logic**, **priority resolver** and **four numbers of DMA channels**.

Each channel has two programmable 16-bit registers named as **address register** and **count register**.

The 8257 is a programmable. Direct Memory Access (DMA) device which, when coupled with a single Intel® 8212 I/O port device, provides a complete four-channels DMA controller for use in Intel® microcomputer systems. After being initialized by software, the 8257 could transfer a block of data, containing up to 16.384 bytes, between memory and a peripheral device directly, without further intervention required of the CPU. Upon receiving a DMA transfer request from an enabled peripheral, the 8257:

1. **Acquires control of the system bus.**

2. **Acknowledges** that requesting peripheral which is connected to the highest priority channel.

3. **Outputs** the least significant eight bits of the memory address onto system address lines A0-A7. outputs the most significant eight bits of the memory address to the 8212 I/O port via.the data bus (the 8212 places these address bits on lines A8-A15), and

4. **Generates the appropriate memory and I/O read/ write control signals** that cause the peripheral to receive or deposit a data byte directly from or to the addressed location in memory.

8257 Modes:

The 8257 processor works on two modes:

1) Master mode

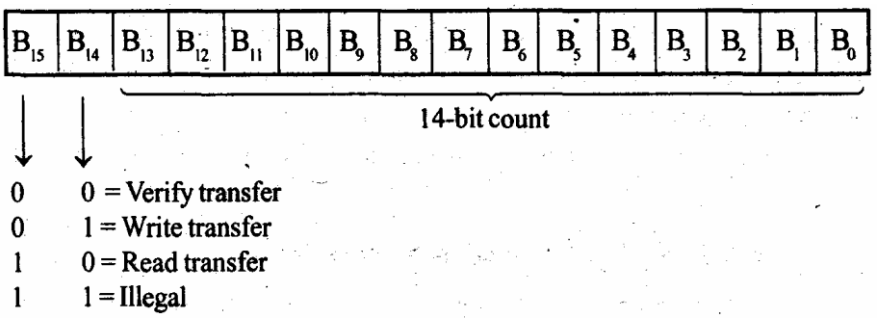
2) Slave mode

- An active-low input which enables the I/O Read or I/O Write input when the 8257 is being read or programmed in the "slave" mode.
- In the "master" mode. CS is automatically disabled to prevent the chip from selecting itself while performing the DMA function.

Control word:

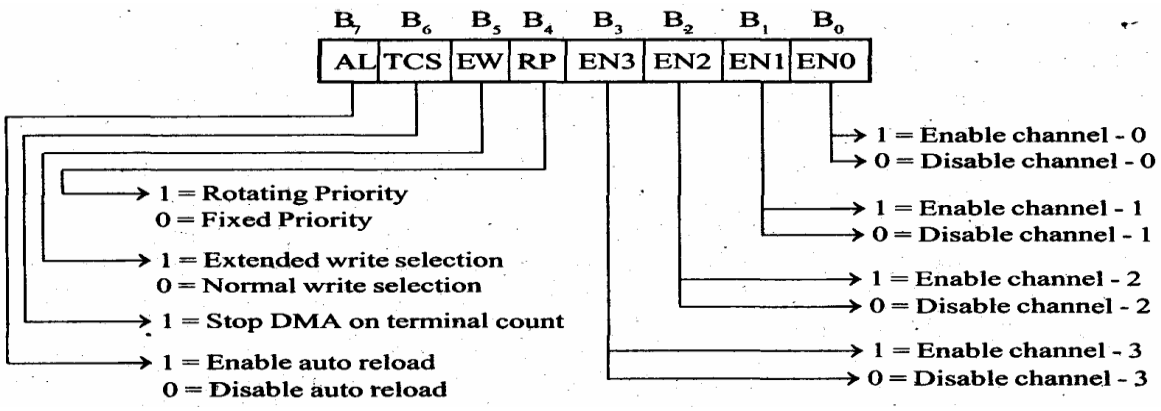
- Address register is used to store the starting address of memory location for DMA data transfer.
- The address in the address register is automatically incremented after every operation (read/write/verify transfer).
- The count register is used to count the number of byte or word transferred by DMA

The format of count register is



- 14-bits B0-B13 is used to count value and a 2-bits is used for indicate the type of DMA transfer (Read/Write/ transfer).
- In read transfer the data is transferred from memory to I/O device.
- In write transfer the data is transferred from I/O device to memory.
- Verification operations generate the DMA addresses without generating the DMA memory and I/O control signals.
- The 8257 has two eight bit registers called mode set register and status register.

The format of mode set register is



The use of mode set register is:

1. Enable/disable a channel.
2. Fixed/rotating priority
3. Stop DMA on terminal count.
4. Extended/normal write time.
5. Auto reloading of channel-2.

- The bits B0, B1, B2, and B3 of mode set register are used to enable/disable channel -0, 1, 2 and 3 respectively. A one in these bit position will enable a particular channel and a zero will disable it

- If the bit B4 is set to one, then the channels will have rotating priority and if it zero then the channels wilt have fixed priority.
    - In rotating priority after servicing a channel its priority is made as lowest.
    - In fixed priority the channel-0 has highest priority and channel-2 has lowest priority.

- If the bit B5 is set to one, then the timing of low write signals (MEMW and IOW) will be extended.

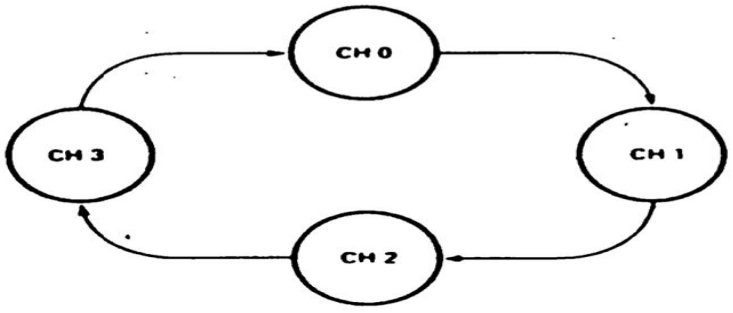
- If the bit B6 is set to one then the DMA operation is stopped at the terminal count.

- The bit B7 is used to select the auto load feature for DMA channel-2.

- When bit B7 is set to one, then the content of channel-3 count and address registers are loaded in channel-2 count and address registers respectively whenever the channel-2 reaches terminal count. When this mode is activated the number of channels available for DMA reduces from four to three.

Rotating Priority Bit 4

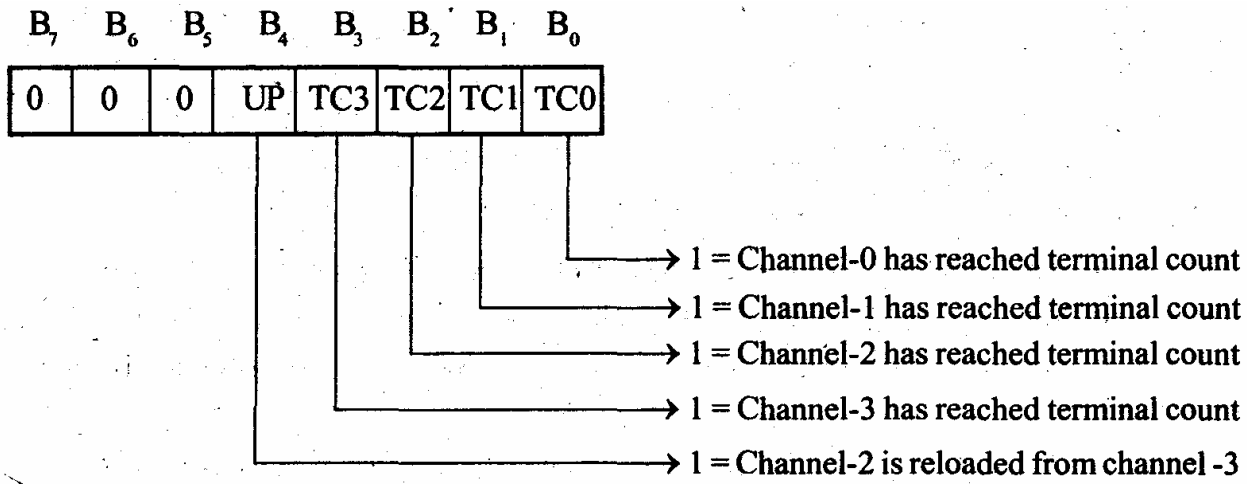
In the Rotating Priority Mode, the priority of the channels has a circular sequence. After each DMA cycle, the priority of each channel changes. The channel which had just been serviced will have the lowest priority.



If the ROTATING PRIORITY bit is not set (set to a zero), each DMA channel has a fixed priority. In the fixed priority mode, Channel 0 has the highest priority and Channel 3 has the lowest priority. If the ROTATING PRIORITY bit is set to a one, the priority of each channel changes after each DMA cycle (not each DMA request). Each channel moves up to the next highest priority assignment, while the channel which has just been serviced moves to the lowest priority assignment:

	CHANNEL → JUST SERVICED	CH-0	CH-1	CH-2	CH-3
Priority → Assignments	Highest	CH-1	CH-2	CH-3	CH-0
		CH-2	CH-3	CH-0	CH-1
		CH-3	CH-0	CH-1	CH-2
	Lowest	CH-0	CH-1	CH-2	CH-3

The format of **status register** of 8257 is shown in fig. below:



- The bit **B0, B1, B2, and B3** of **status register** indicates the **terminal count status** of channel-0, 1,2 and 3 respectively. A one in these bit positions indicates that the particular channel has reached terminal count.
- These status bits are cleared after a read operation by microprocessor.
- The **bit B4** of **status register** is called **update flag** and a **one in this bit position indicates that the channel-2 register has been reloaded from channel-3 registers in the auto load mode of operation.**

The internal addresses of the registers of 8257 are listed in table.

8257 Register Selection

Register	Binary Address								Hexa Address
	Decoder input and enable				Input to address pins of 8257				
	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
Channel-0 DMA address register	0	1	1	0	0	0	0	0	60
Channel-0 count register	0	1	1	0	0	0	0	1	61
Channel-1 DMA address register	0	1	1	0	0	0	1	0	62
Channel-1 count register	0	1	1	0	0	0	1	1	63
Channel-2 DMA address register	0	1	1	0	0	1	0	0	64
Channel-2 count register	0	1	1	0	0	1	0	1	65
Channel-3 DMA address register	0	1	1	0	0	1	1	0	66
Channel-3 count register	0	1	1	0	0	1	1	1	67
Mode set register (Write only)	0	1	1	0	1	0	0	0	68
Status register (Read only)	0	1	1	0	1	0	0	0	68

DMA operation state diagram:

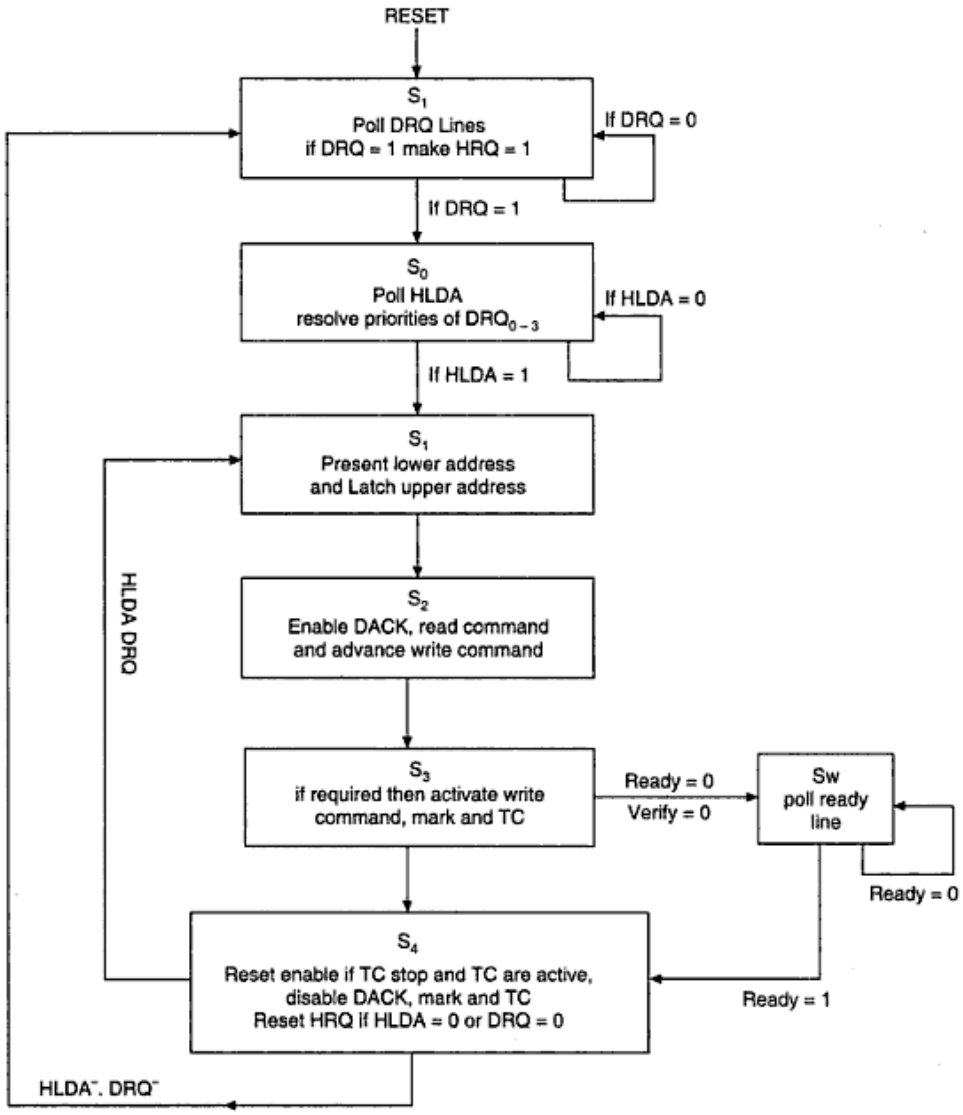


Figure 14.14 State diagram of 8257.

Single Byte Transfers

- A single byte transfer is initiated by the I/O device raising the DRQ line of one channel of the 8257. If the channel is enabled, the 8257 will output a HRQ to the CPU.
- The 8257 now waits until a HLDA is received insuring that the system bus is free for its use. Once HLDA is received the DACK line for the requesting channel is activated (LOW). The DACK line acts as a chip select for the requesting I/O device.
- The 8257 then generates the read and write commands and byte transfer occurs between the selected I/O device and memory. After the transfer is complete, the DACK line is set HIGH and the HRQ line is set LOW to indicate to the CPU that the bus is now free for use.
- DRQ must remain HIGH until DACK is issued to be recognized and must go LOW before S4 of the transfer sequence to prevent another transfer from occurring. (See timing diagram.)

Consecutive Transfers

- If more than one channel requests service simultaneously, the transfer will occur in the same way a burst does. No overhead is incurred by switching from one channel to another.
- In each S4 the DRQ lines are sampled and the highest priority request is recognized during the next transfer.
- A **burst mode** transfer in a lower priority channel will be overridden by a higher priority request. Once the high priority transfer has completed control will return to the lower priority channel if its DRQ is still active.
- No extra cycles are needed to execute this sequence and the HRQ tine remains active until all DRQ lines go LOW.

Control Override

The continuous DMA transfer mode described above can be interrupted by an external device by lowering the HLDA line. After each DMA transfer the 8257 samples the HLDA line to insure that it is still active. If it is not active, the 8257 completes the current transfer, releases the HRQ line (LOW) and returns to the idle state. If DRQ lines are still active the 8257 will raise the HRQ line in the third cycle and proceed normally. (See timing diagram.)

Ready

The 8257 has a Ready input similar to the 8080A and the 8085A. The Ready line is sampled in State 3. If Ready is LOW the 8257 enters a wait state. Ready is sampled during every wait state. When Ready returns HIGH the 8257 proceeds to State 4 to complete the transfer. Ready is used to interface memory or I/O devices that cannot meet the bus set up times required by the 8257.

Speed: The 8257 uses four clock cycles to transfer a byte of data. No cycles are lost in the master to master transfer maximizing **bus** efficiency. A 2MHz clock input will allow the 8257 to transfer at a rate of 500K bytes/second.

Memory Mapped I/O Configurations

The 8257 can be connected to the system bus as a memory device instead of as an I/O device for memory mapped I/O configurations by connecting the system memory control lines to the 8257s I/O control lines and the system I/O control lines to the 8257s memory control lines.

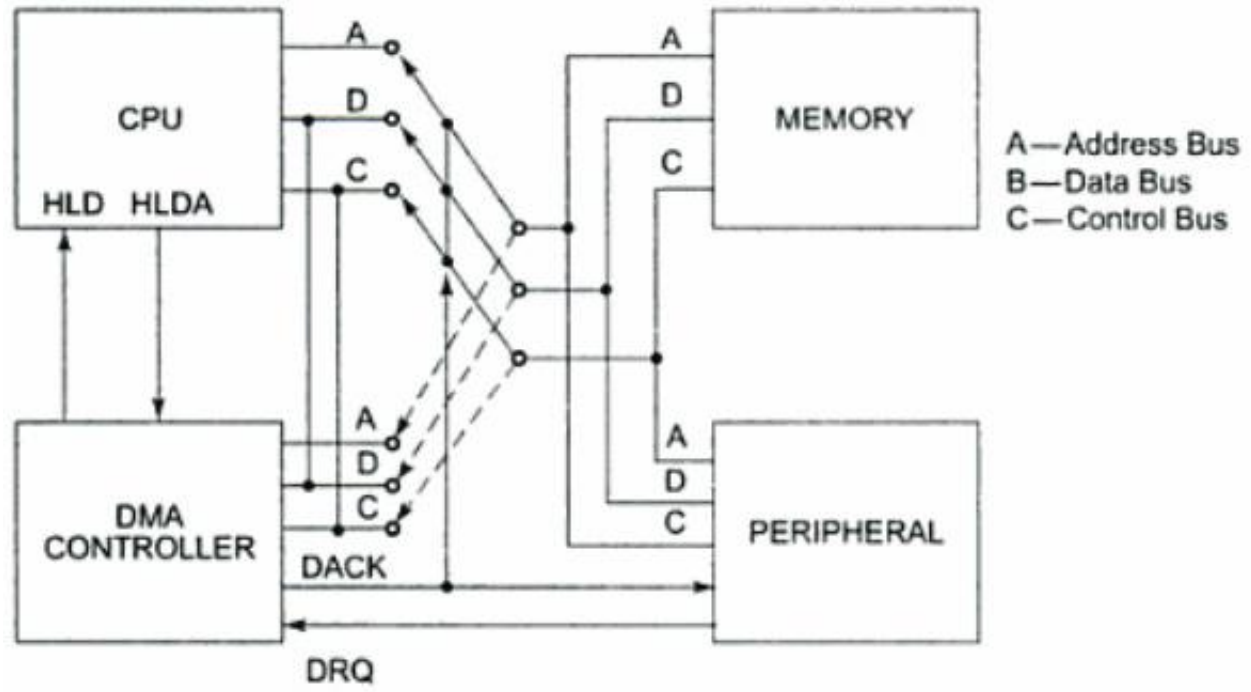
This configuration permits use of the 8080's considerably larger repertoire of memory instructions when reading or loading the 8257s registers. Note that with this connection, the programming of the Read (bit 15) and Write (bit 14) bits in the terminal count register will have a different meaning.

Interfacing 8257 with 8086

- Once a DMA controller is initialized by a CPU property, it is ready to take control of the system bus on a DMA request, either from a peripheral or itself (in case of memory-to-memory transfer).

- The DMA controller sends a HOLD request to the CPU and waits for the CPU to assert the HLDA signal. The CPU relinquishes the control of the bus before asserting the HLDA signal.

A conceptual implementation of the system is shown in Figure



- Once the HLDA signal goes high, the DMA controller activates the DACK signal to the requesting peripheral and gains the control of the system bus.

- The DMA controller is the sole master of the bus, till the DMA operation is over. The CPU remains in the HOLD status (all of its signals are tri-state except HOLD and HLDA), till the DMA controller is the master of the bus.

- In other words, the DMA controller interfacing circuit implements a switching arrangement for the address, data and control busses of the memory and peripheral subsystem from/to the CPU to/from the DMA controller.