UNIT-5

System and interfacing and data acquisition – Data Acquisition Systems, Analog to Digital and Digital to Analog conversions; Digital Signal Processing – data flow in DSPs, block diagrams, typical layouts, Interfacing motor drives.

Data Acquisition System:

A typical Data Acquisition System consists of individual sensors with the necessary signal conditioning, data conversion, data processing, multiplexing, data handling and associated transmission, storage and display systems.

In order to optimise the characteristics of the system in terms of performance, handling capacity and cost, the relevant sub systems can be combined together. Analog Data Acquisition System is generally acquired and converted into digital form for the purpose of processing, transmission, display and storage.

Processing may consist of a large variety of operations, ranging from simple comparison to complicated mathematical manipulations. It can be for such purposes as collecting information (averages, statistics), converting the data into a useful form (e.g., calculations of efficiency of motor speed, torque and power input developed), using data for controlling a process, performing repeated calculations to separate signals buried in the noise, generating information for display, and various other purposes.

Data may be transmitted over long distances (from one point to another) or short distances (from test centre to a nearby PC).

The data may be displayed on a digital panel or on a CRT. The same be stored temporarily (for immediate use) or permanently for ready reference later.

Data acquisition generally relates to the process of collecting the input data in digital form as rapidly, accurately, and economically as necessary. The basic instrumentation used may be a DPM with digital outputs, a shaft digitiser, or a sophisticated high speed resolution device.

To match the input requirements with the output of the sensor, some form of scaling and offsetting is necessary, and this is achieved by the use of amplifier/ attenuators.

For converting analog information from more than one source, either additional transducers or multiplexers are employed. To increase the speed with which information is accurately converted, sample-hold circuits are used. (In some cases, for analog signals with extra-wide range, logarithmic conversion is used.)

Data Acquisition System Block Diagram:

A schematic block diagram of a General Data Acquisition System (DAS) is shown in

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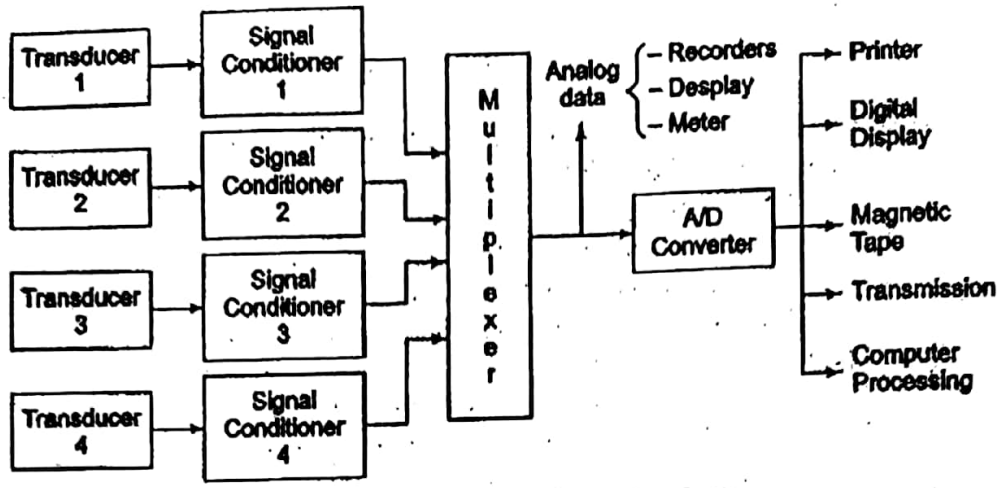


Fig. 17.1 Generalised Data Acquisition System

The characteristics of the data acquisition system, depend on both the properties of the analog data and on the processing carried out.

Based on the environment, a broad Classifications of data acquisition system into two categories.

1. **Those suitable for favourable environments (Those intended for hostile environments**

The former category may include, among other, laboratory instrument applications, test systems for collecting long term drift information on zeners, high calibration test instruments, and routine measurements in research, as mass spectrometers and lock-in amplifiers. In these, the systems are designed to perform tasks oriented more towards making sensitive measurements than to problems of protecting the integrity of analog data.

The Classifications of data acquisition system specifically includes measure, protecting the integrity of the analog data under hostile conditions. Such measurement conditions arise in aircraft control systems, turbovisous in electrical power systems, and in industrial process control systems.

Most of these hostile measurement conditions require devices capable of a wide range of temperature operations, excellent shielding, redundant paths for critical measurements and considerable processing of the digital data acquisition system.

On the other hand, laboratory measurements are performed over a narrow temperature range with much less electrical noise, employing high sensitivity and precision devices for higher accuracies and resolution.

The important Factors to Consider When Setting Up a Data Acquisition System are as follows.

1. Accuracy and resolution
2. Number of channels to be monitored
3. Analog or digital signal
4. Single channel or multichannel
5. Sampling rate per channel
6. Signal conditioning requirements of each channel
7. Cost

The various general Configuration of Data Acquisition System are

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1. **Single channel possibilities**
- Direct conversion
- Pre-amplification and direct conversion
- Sample and hold, and conversion
- Pre-amplification, signal conditioning and any of the above
2. **Multi channel possibilities**
- Multiplexing the outputs of single channel converters
- Multiplexing the output of sample-hold circuits
- Multiplexing the inputs of sample-hold circuits
- Multiplexing low level data

Objectives of Data Acquisition System:

- It must acquire the necessary data, at correct speed and at the correct
- Use of all data efficiently to inform the operator about the state of the
- It must monitor the complete plant operation to maintain on-line optimum and safe operations.
- It must provide an effective human communication system and be able to identify problem areas, thereby minimising unit availability and maximising unit through point at minimum cost.
- It must be able to collect, summarise and store data for diagnosis of operation and record purpose.
- It must be able to compute unit performance indices using on-line, real-time data.
- It must be flexible and capable of being expanded for future require
- It must be reliable, and not have a down time greater than 0.1%.

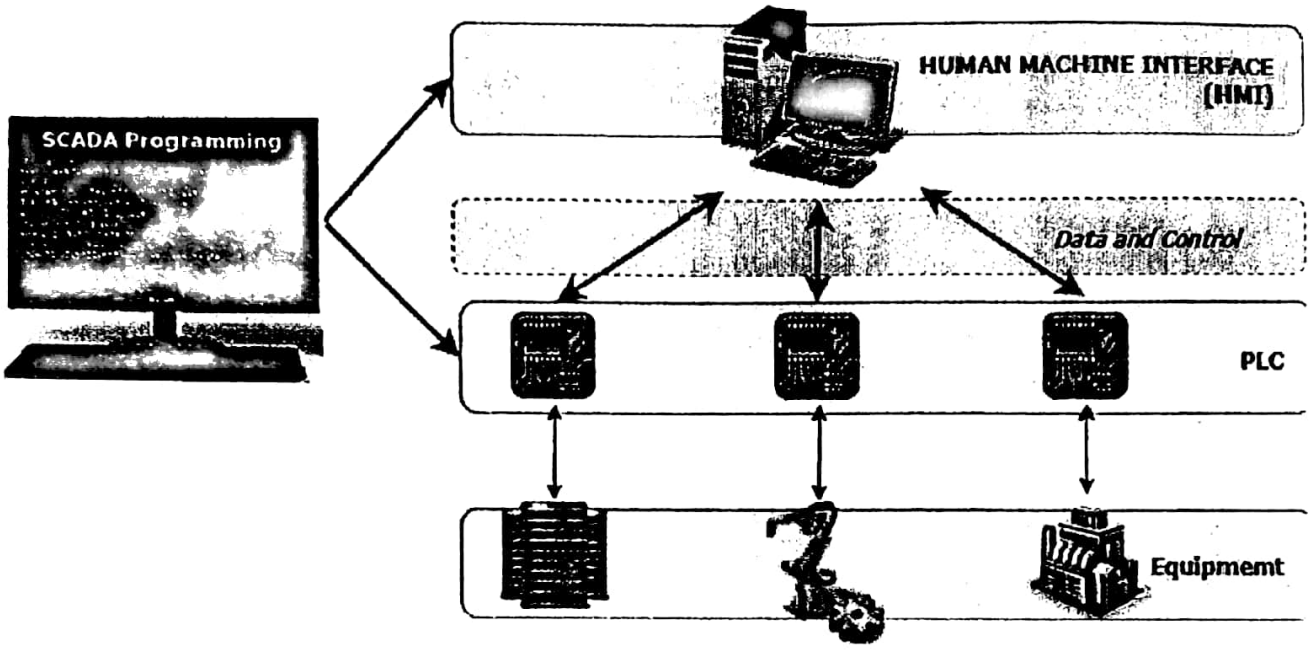
SCADA

Supervisory Control and Data Acquisition (SCADA) is a system that aims to monitor and control field devices at your remote sites. SCADA systems are critical as it helps maintain efficiency by collecting and processing real-time data.

The main goal of this supervisory system is to monitor and control equipment in the industrial processes for companies in the public and private sectors. As a matter of fact, in today's world, there are SCADA systems almost everywhere. This includes industrial plants, manufacturing, transportation, oil and gas, power distribution, water control and etc.

Let's dive deeper into SCADA functions and the components that make SCADA operations possible.

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SCADA systems perform several functions that allow for proper management of remote facilities. The following are the core functions of a SCADA system.

1.Data Acquisition

The collection of SCADA data frequently involves some kind of analog to digital conversion. Temperature is converted to degrees Celsius. Transmit signal strength is converted to dBm. Chann quality is measured in errored seconds.

2. Networked Data Communication

The collected data is transmitted either spontaneously or in response to a request for data to some kind of upstream consolidator or master. The communication channel can be analog (T202, POTS or digital (RS485, TCP/IP). SCADA network topology typically also includes some kind of transport validation independent of any content validation.

3.Data Presentation

The collected data is processed, organized and presented for system operators to make appropriate response and control decisions. The presentation can vary from tabular presentation of logged events to graphical presentation against mapping or image backgrounds.

4. Control

If control decisions are warranted and the system supports output, appropriate commands can be dispatched to affect specific operational or configuration changes. Most control actions are performed by RTUs and PLCs.

The Four Main Components Of SCADA

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If you plan to deploy a SCADA system, then you need to know and understand the four important system components that present in every SCADA network. Yours might be tailored to your specifi requirements, but it will need the following basic components

1.Inputs

Inputs (either digital or analog) and output relays or electrical signals that directly interface with managed elements in the remote sites. That's where the SCADA functions start.

These sensors and control relays perform the data acquisition but can't interpret communication protocols on their own. But your SCADA system still needs a way to collect this data and report it to you in a meaningful way. That's where RTUs come into play.

2. Remote Telemetry Units (RTUs)

Just like Programmable Logic Controllers (PLC), RTUs are small computerized units deployed in the field at specific sites and locations. Remote telemetry unit, also known as a remote terminal un (RTU), serves as local collection points for gathering reports from sensors and delivering commands to control relays.

3. Human Machine Interface (HMI) SCADA

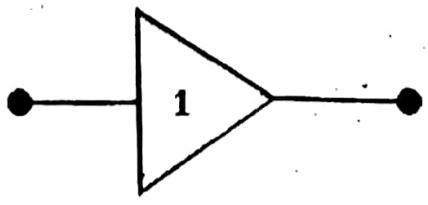
HMI software is a computer master station system that processes data and allows a human operato to manage and control the system. HMIs provide the human operator with information gathered from multiple RTUs. This information is displayed in the master unit's user interface that should b understandable and actionable since quick response actions to alarms are usually required. The bes HMI SCADA software will present the data as an intuitive graphical representation based on maps

4. Communications Network

The communications network is what connects telemetry and SCADA at your remote sites. Today one of the most common communications technology is Ethernet.

Buffers

Sometimes in digital electronic circuits we need to isolate logic gates from each other or have them drive or switch higher than normal loads, such as relays, solenoids and lamps without the need for inversion. One type of single input logic gate that allows us to do just that is called the **Digital Buffer.**



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A **digital buffer** (or a **voltage buffer**) is an electronic circuit element that is used to isolate the input from the output, providing either no voltage or a voltage that is same as the input voltage. It draws very little current and will not disturb the original circuit. It is also called a unity gain buffer because it provides a gain of 1, which means it provides at most the same voltage as the input voltage, serving no amplification function.

A voltage buffer has a very high input impedance (the opposition to current flow viewed from the load). The high input impedance is the reason a voltage buffer is used. A circuit with a voltage buffer will always draw a little amount of current because of the high input impedance of the buffer. As a result, the power source will not be affected.

The digital buffer is important because it can control the on and off of data transmission, which is used widely in the world of registers (sophisticated data storage device) and buses (data transferring device). A typical digital buffer that is used to control multiple data inputs written onto a bus is a Tri-State Digital Buffer, which controls the data flow by "tri-state" pins.

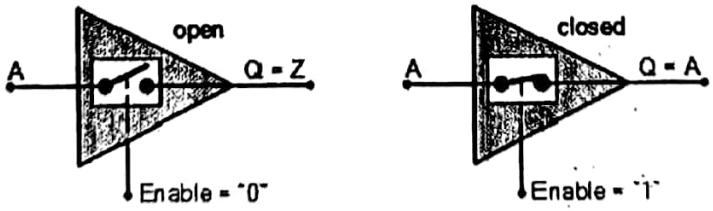
The "Tri-state Buffer"

As well as the standard Digital Buffer seen above, there is another type of digital buffer circuit whose output can be "electronically" disconnected from its output circuitry when required. This type of Buffer is known as a 3-State Buffer or more commonly a Tri-state Buffer.

A Tri-state Buffer can be thought of as an input controlled switch with an output that can be electronically turned "ON" or "OFF" by means of an external "Control" or "Enable" (EN) signal input. This control signal can be either a logic "0" or a logic "1" type signal resulting in the Tri-state Buffer being in one state allowing its output to operate normally producing the required output or in another state were its output is blocked or disconnected.

Then a tri-state buffer requires two inputs. One being the data input and the other being the enable or control input as shown.

Tri-state Buffer Switch Equivalent



When activated into its third state it disables or turns "OFF" its output producing an open circuit condition that is neither at a logic "HIGH" or "LOW", but instead gives an output state of very high impedance, **High-Z**, or more commonly Hi-Z. Then this type of device has two logic state inputs, "0" or a "1" but can produce three different output states, "0", "1" or " Hi-Z " which is why it is called a "Tri" or "3-state" device.

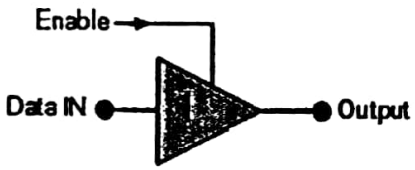
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Note that this third state is NOT equal to a logic level "0" or "1", but is an high impedance state in which the buffers output is electrically disconnected from the rest of the circuit. As a result, no current is drawn from the supply.

There are four different types of Tri-state Buffer, one set whose output is enabled or disabled by an "**Active-HIGH**" control signal producing an inverted or non-inverted output, and another set whose buffer output is controlled by an "**Active-LOW**" control signal producing an inverted or non-inverted output as shown below.

Active "HIGH" Tri-state Buffer

Symbol



Tri-state Buffer

Truth Table

Enable	IN	OUT
0	0	Hi-Z
0	1	Hi-Z
1	0	0
1	1	1

Read as Output = Input if Enable is equal to "1"

An **Active-high** Tri-state Buffer such as the 74LS241 octal buffer, is activated when a logic level "1" is applied to its "enable" control line and the data passes through from its input to its output. When the enable control line is at logic level "0", the buffer output is disabled and a high impedance condition, Hi-Z is present on the output.

An active-high tri-state buffer can also have an inverting output as well as its high impedance state creating an active-high tri-state inverting buffer as shown.

Handshaking

When two devices have to send and receive data at different rates, handshaking is necessary. Slower device controls the rate at which data are transferred. For parallel data transfer strobe and acknowledge is the method used. "Readiness to receive data" is indicated by the receiving device and then data is sent by the sending device, and while data is being received the receiving device indicates "not ready for data". When data reception is complete it indicates "ready for data" so that data can be sent again.

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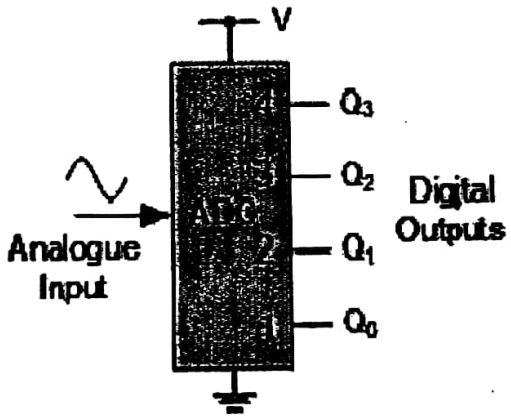
Analogue-to-Digital Converters, (ADCs)

Digital Signal: A digital signal is a signal that represents data as a sequence of discrete values; at any given time it can only take on one of a finite number of values.
Analog Signal: An analog signal is any continuous signal for which the time varying feature of the signal is a representation of some other time varying quantity i.e., analogous to another time varying signal.
The following techniques can be used for Analog to Digital Conversion:

a. PULSE CODE MODULATION:

The most common technique to change an analog signal to digital data is called pulse code modulation (PCM). A PCM encoder has the following three processes:

1. Sampling
2. Quantization
3. Encoding

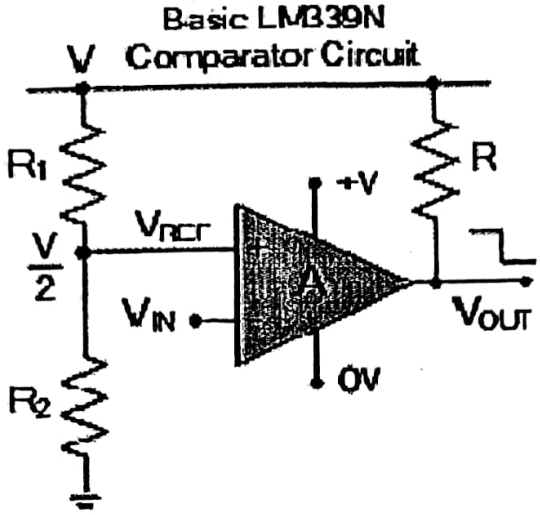


The process of taking an analogue voltage signal and converting it into an equivalent digital signal can be done in many different ways, and while there are many analogue-to-digital converter chips such as the ADC08xx series available from various manufacturers, it is possible to build a simple ADC using discrete components. One simple and easy way is by using parallel encoding, also known as *flash*, *simultaneous*, or *multiple comparator* converters in which comparators are used to detect different voltage levels and output their switching state to an encoder.

Parallel of "Flash" A/D converters use a series of interconnected but equally spaced comparators and voltage references generated by a series network of precision resistors for generating an equivalent output code for a particular n-bit resolution. The advantage of parallel or flash converters is that they are simple to construct and do not require any timing clocks as the instant an analogue voltage is applied to the comparator inputs, it is compared against a reference voltage. Consider the comparator circuit below.

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Comparator Circuit



An analogue comparator such as the LM339N which has two analogue inputs, one positive and one negative, and which can be used to compare the magnitudes of two different voltage levels. A voltage input, (V_{IN}) signal is applied to one input of the comparator, while a reference voltage, (V_{REF}) to the other. A comparison of the two voltage levels at the comparator's input is made to determine the comparators digital logic output state, either a "1" or a "0".

The reference voltage, V_{REF} is compared against the input voltage, V_{IN} applied to the other input. For an LM339 comparator, if the input voltage is less than the reference voltage, ($V_{IN} < V_{REF}$) the output is "OFF", and if it is greater than the reference voltage, ($V_{IN} > V_{REF}$) the output will be "ON". Thus a comparator compares two voltage levels and determines which one of the two is higher.

In our simple example above, V_{REF} is obtained from the voltage divider network setup by R_1 and R_2. If the two resisors are of equal values, that is $R_1 = R_2$, then clearly the reference voltage level will be equal to half the supply voltage, or V/2. So for a comparator with an open-collector output, if V_{IN} is less than V/2, the output is HIGH, and if V_{IN} is greater than V/2, the output is LOW acting as a 1-bit ADC.

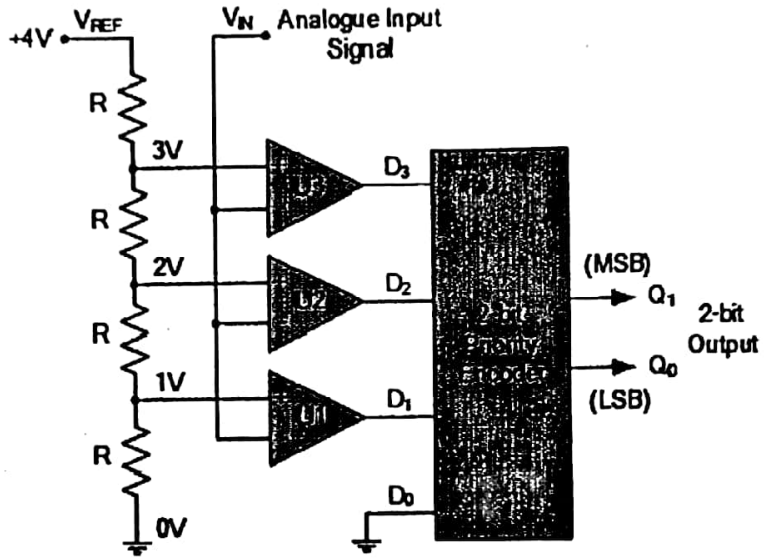
But by adding more resistors to the voltage divider network we can effectively "divide" the supply voltage by an amount determined by the resistances of the resistors. However, the more resistors we use in the voltage divider network the more comparators will be required.

In general, $2^n - 1$ comparators would be required for conversion of an "n"-bit binary output, where "n" is typically in the range from 8 to 16. In our example above, the single bit ADC used $2^1 - 1$, which equals "1" comparator to determine if V_{IN} was greater or smaller than the V/2 reference voltage.

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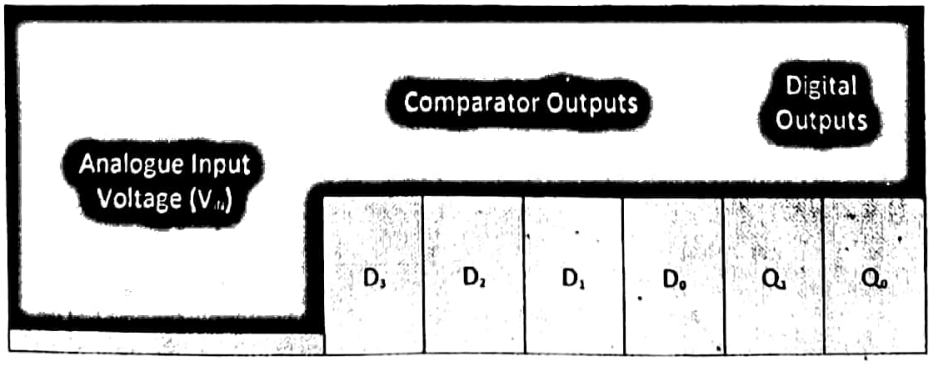
If we now create a 2-bit ADC, then we will need $2^2 - 1$ which is "3" comparators as we need four different voltage levels corresponding to the 4 digital values required for a 4-to-2 bit encoder circuit as shown.

2-bit Analogue to Digital Converter Circuit



This will give us a 2-bit output code for all four possible values of analogue input of:

2-bit A/D converter Output



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0 to 1 V	0	0	0	0	0	0
1 to 2 V	0	0	1	X	0	1
2 to 3 V	0	1	X	X	1	0
3 to 4 V	1	X	X	X	1	1

Where: "X" is a "don't care", that is either a logic "0" or a logic "1" condition.

So how does this *analogue-to-digital converter* work. For an A/D converters to be useful it has to produce a meaningful digital representation of the analogue input signal. Here in this simple 2-bit ADC example we have assumed for simplicity that the input voltage V_{IN} is between 0 and 4 volts, so have set V_{REF} and the resistive voltage-divider network to drop 1 volt across each resistor.

When V_{IN} is between 0 and 1 volt, (<1V) the input on all three comparators will be less than the reference voltage, so their outputs will be LOW and the encoder will output a binary zero (00) condition on pins Q_0 and Q_1. When V_{IN} increases and exceeds 1 volt but is less than 2 volts, ($1V<V_{IN}<2V$) comparator U1 which has a reference voltage input set at 1 volt, will detect this voltage difference and produce a HIGH output. The priority encoder which is used as the 4-to-2 bit encoding detects the change of input at D_1 and produces a binary output of "1" (01).

Note that a **Priority Encoder** such as the TTL 74LS148 allocates a priority level to each individual input. The priority encoders output corresponds to the currently active input which has the highest priority. So when an input with a higher priority (D_1 compared to D_0) is present, all other inputs with a lower priority will be ignored. So if there are two or more inputs at logic level "1" at the same time, the actual output code on D_0 and D_1 would only correspond to the input with the highest designated priority.

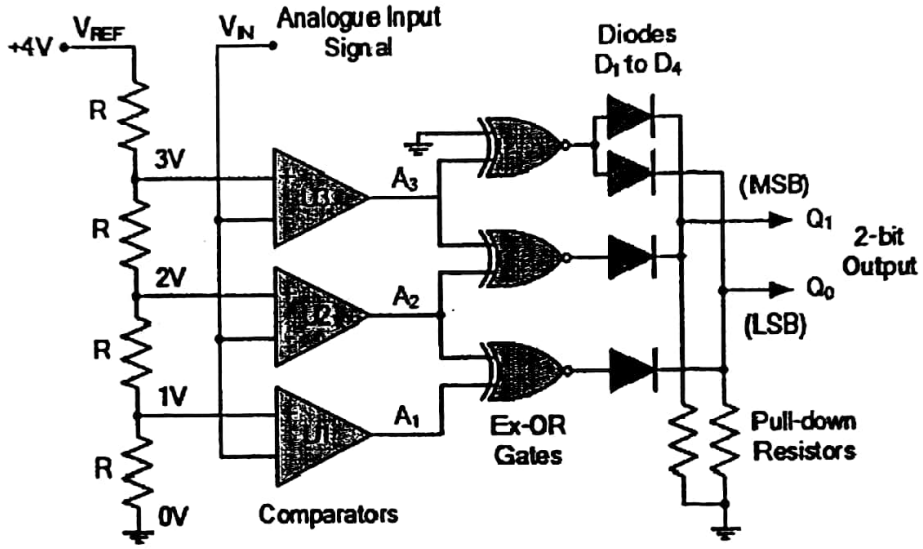
So now as V_{IN} increases above 2 volts, the next reference voltage level, comparator U2 detects the change and produces a HIGH output. But because input D_2 has a higher priority than inputs D_0 or D_1, the priority encoder outputs a binary "2" (10) code, and so on when V_{IN} exceeds 3 volts producing a binary code output of "3" (11). Clearly as V_{IN} reduces or changes between each reference voltage level, each comparator will output either a HIGH

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or a LOW condition to the encoder which inturn produces a 2-bit binary code between 00 and 11 relative to V_{IN}.

This is all well and good, but priority encoders are not available as 4-to-2 bit devices, and if we use a commercially available one such as the TTL 74LS148 or its CMOS 4532 equivalent which are both 8-bit devices, then six of the binary bits would not be used. But a simple encoder circuit can be made using digital Ex-OR gates and a matrix of signal diodes as shown.

2-bit ADC Using Diodes



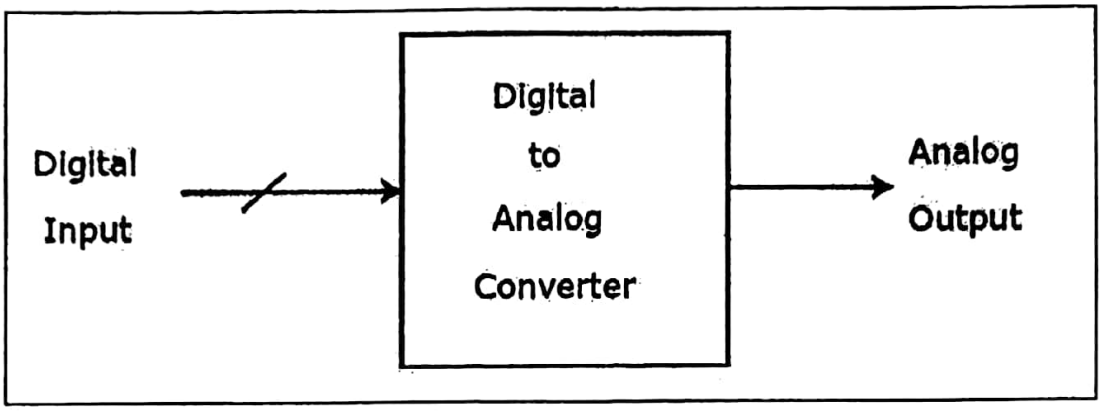
Here the outputs of the comparators are encoded using Exclusive-OR gates before being fed to the diodes. Two external pull-down resistor are used at their outputs and ground (0V) to ensure a LOW condition and stop the outputs from floating when the diodes are reverse biased. So as with the previous circuit, depending upon the value of V_{IN} determines which comparator produces an output signal HIGH (or LOW) to the exclusive-OR gates producing a HIGH output if one input or the other input is HIGH, but not both, (Boolean expression is Q = A.B + A.B). These Ex-OR gates could also be constructed using the combinational logic AND–OR–NAND gates.

The problem here with both designs of 4-to-2 converters is that the *resolution* of this simple 2-bit A/D converter is 1 volt because as we have seen, the analogue input voltage at V_{IN} must change by one full volt in order for the encoder to change its output code. One way to improve the resolution of the output is to increase it to a 3-bit A/D converter using more comparators.

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A **Digital to Analog Converter (DAC)** converts a digital input signal into an analog output signal. The digital signal is represented with a binary code, which is a combination of bits 0 and 1. This chapter deals with Digital to Analog Converters in detail.

The **block diagram** of DAC is shown in the following figure –



A Digital to Analog Converter (DAC) consists of a number of binary inputs and a single output. In general, the **number of binary inputs** of a DAC will be a power of two.

Types of DACs

There are **two types** of DACs

- Weighted Resistor DAC
- R-2R Ladder DAC

This section discusses about these two types of DACs in detail –

Weighted Resistor DAC

A **weighted resistor DAC** produces an analog output, which is almost equal to the digital (binary) input by using **binary weighted resistors** in the inverting adder circuit. In short, a binary weighted resistor DAC is called as **weighted resistor DAC.**

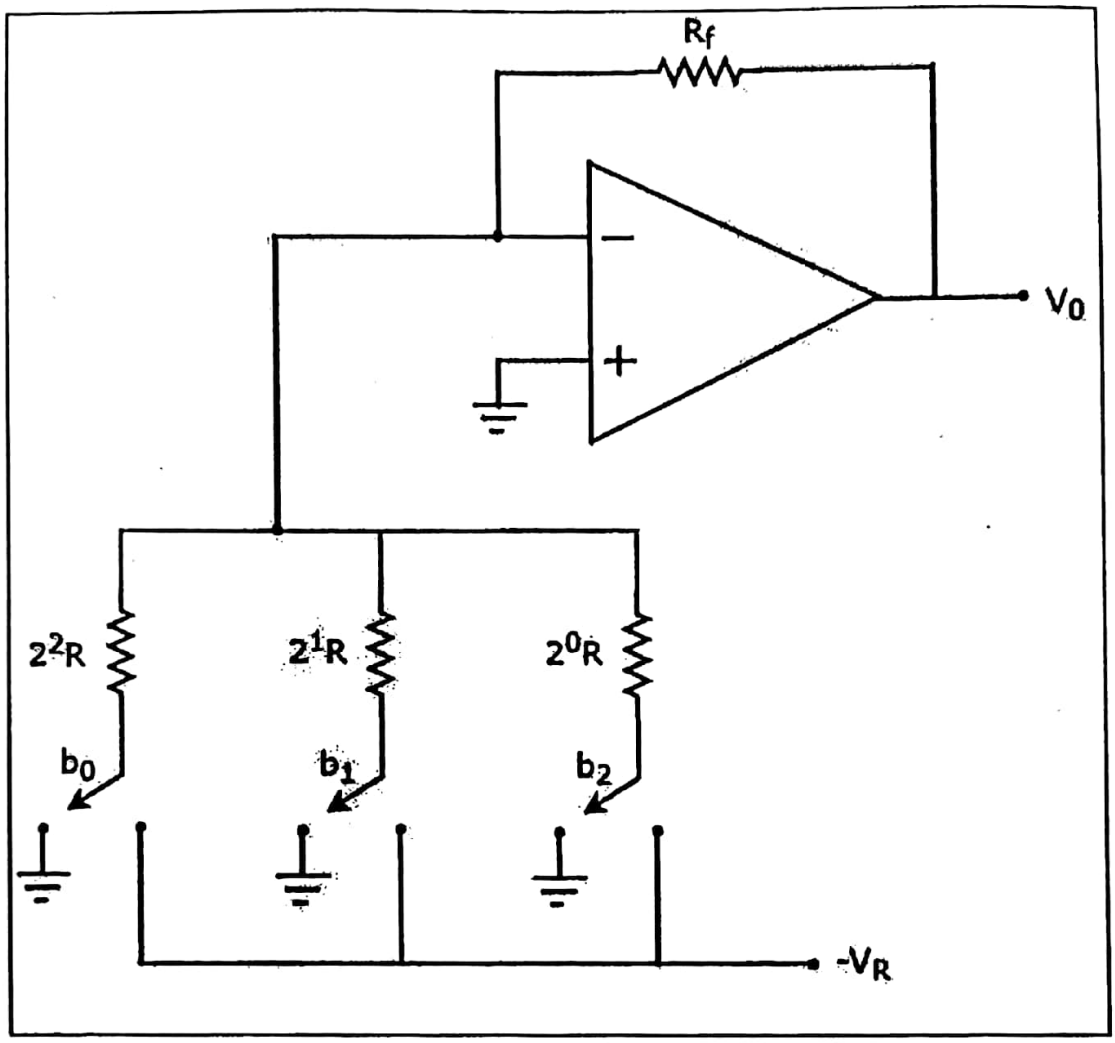
The **circuit diagram** of a 3-bit binary weighted resistor DAC is shown in the following figure –

Recall that the bits of a binary number can have only one of the two values. i.e., either 0 or 1. Let the **3-bit binary input** is $b_2b_1b_0$ $b_2b_1b_0$. Here, the bits b_2 b_2 and b_0 b_0 denote the **Most Significant Bit (MSB) and Least Significant Bit (LSB)** respectively.
The **digital switches** shown in the above figure will be connected to ground, when the corresponding input bits are equal to '0'. Similarly, the digital switches shown in the above figure will be connected to the negative reference voltage, $-V_R$ $-VR$ when the corresponding input bits are equal to '1'.

In the above circuit, the non-inverting input terminal of an op-amp is connected to ground.

That means zero volts is applied at the non-inverting input terminal of op-amp.

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According to the virtual short concept, the voltage at the inverting input terminal of opamp is same as that of the voltage present at its non-inverting input terminal. So, the voltage at the inverting input terminal's node will be zero volts.

The disadvantages of a binary weighted resistor DAC are as follows –

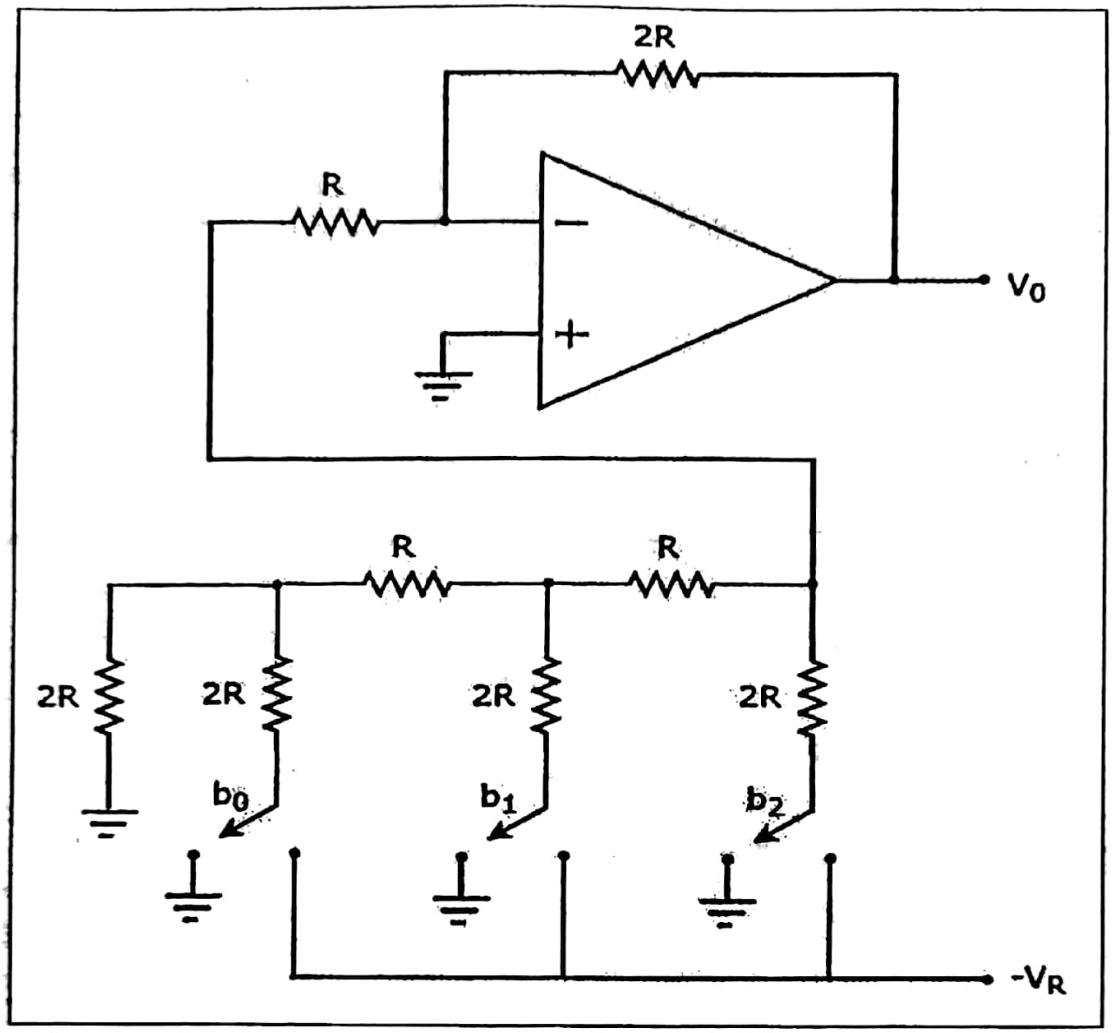
- **The difference between the resistance values corresponding to LSB & MSB will increase as the number of bits present in the digital input increases.**
- **It is difficult to design more accurate resistors as the number of bits present in the digital input increases.**

R-2R Ladder DAC

The R-2R Ladder DAC overcomes the disadvantages of a binary weighted resistor DAC. As the name suggests, R-2R Ladder DAC produces an analog output, which is almost equal to the digital (binary) input by using a **R-2R ladder network** in the inverting adder circuit.

The**circuit diagram**of a 3-bit R-2R Ladder DAC is shown in the following figure –

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Recall that the bits of a binary number can have only one of the two values. i.e., either 0 or 1. Let the 3-bit binary input is $b_2b_1b_0$ or $b_2b_1b_0$. Here, the bits b_2 and b_0 denote the Most Significant Bit (MSB) and Least Significant Bit (LSB) respectively.

The digital switches shown in the above figure will be connected to ground, when the corresponding input bits are equal to '0'. Similarly, the digital switches shown in above figure will be connected to the negative reference voltage, $-V_R$ when the corresponding input bits are equal to '1'.

It is difficult to get the generalized output voltage equation of a R-2R Ladder DAC. But, we can find the analog output voltage values of R-2R Ladder DAC for individual binary input combinations easily.

The advantages of a R-2R Ladder DAC are as follows –

- R-2R Ladder DAC contains only two values of resistor: R and 2R. So, it is easy to select and design more accurate resistors.
- If more number of bits are present in the digital input, then we have to include required number of R-2R sections additionally.

Due to the above advantages, R-2R Ladder DAC is preferable over binary weighted resistor DAC.

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9.5 Data Flow in DSPs, Block Diagrams and Typical Layouts

Figure 9.22 indicates a block diagram indicating the data flow representation in a DSP. Signal processing systems can be expressed as a network of transfer functions, data sources, data sinks and control functions. Such networks can, in turn, be represented clearly by diagrams, with icons or "blocks" (representing the functions) linked by lines (which depict communication between the functions). Each block represents a function, such as addition, subtraction, FFT, etc. The blocks are connected with lines or arrows, called directed arcs, which indicate how data moves between the blocks. Such diagrams are called data flow graphs, or more commonly, block diagrams, and they provide a convenient method of describing, documenting and analyzing a signal processing system. Figure 9.23 indicates a block diagram indicating the functional blocks of a typical DSP.

Figure 9.24 indicates the use of DSPs in a typical layout. DSP56001 has many I/O functions which simplifies the implementations. Motroloa 56001 has 13.5 MIPS processing power with 24-bit word length. The implementation shown below has the following interfaces:

1. Host interface to the host computer.
2. Line level analog inputs and outputs.
3. Microphone preamplifier inputs and headphone output.
4. Special monitor loud speaker output.
5. Eight general-purpose high current outputs and four general-purpose inputs.
6. TTL level time multiplexer to interface more A/D and D/A converters.

Types of DSPs

Because different applications have varying ranges of frequencies, different DSPs are required. DSPs are classified by their dynamic range, the spread of numbers that must be processed in the course of an application. This number is a function of the processor's data width (the number of bits it manipulates) and the type of arithmetic it performs (fixed or floating point). For example, a 32-bit processor has a wider dynamic range than a 24-bit processor, which in turn has a wider range than 16-bit processor. Floating-point chips have wider ranges than fixed-point devices.

Each type of processor is suited for a particular range of applications. 16-bit fixed-point DSPs are used for voice-grade systems such as phones, because they work with a relatively narrow range of sound frequencies. Hi-fidelity stereo sound has a wider range, calling for a 16-bit ADC and a 24-bit fixed-point DSP. Image processing, 3D graphics and scientific simulations have a much wider dynamic range and require a 32-bit floating-point processor.

How Fast are DSPs?

The primary reason for using a DSP instead of a traditional microprocessor is *speed*, the ability to move samples into the device, carry out the needed mathematical operations and output the processed data. This

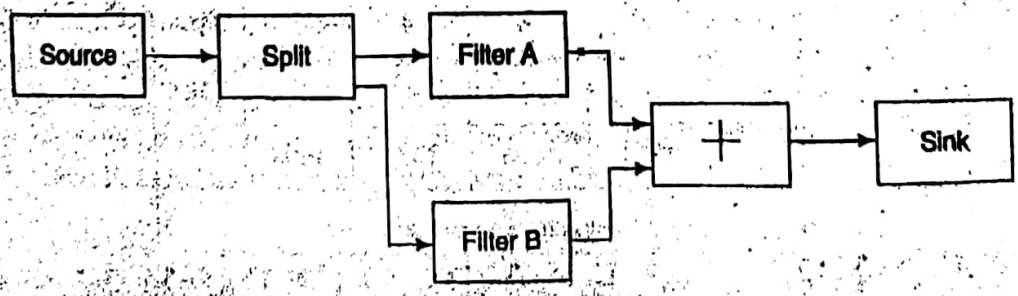


Figure 9.22 | Block diagram for data flow in DSP.

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Figure 9.23 | Block diagram of internal funotional blocks of DSP

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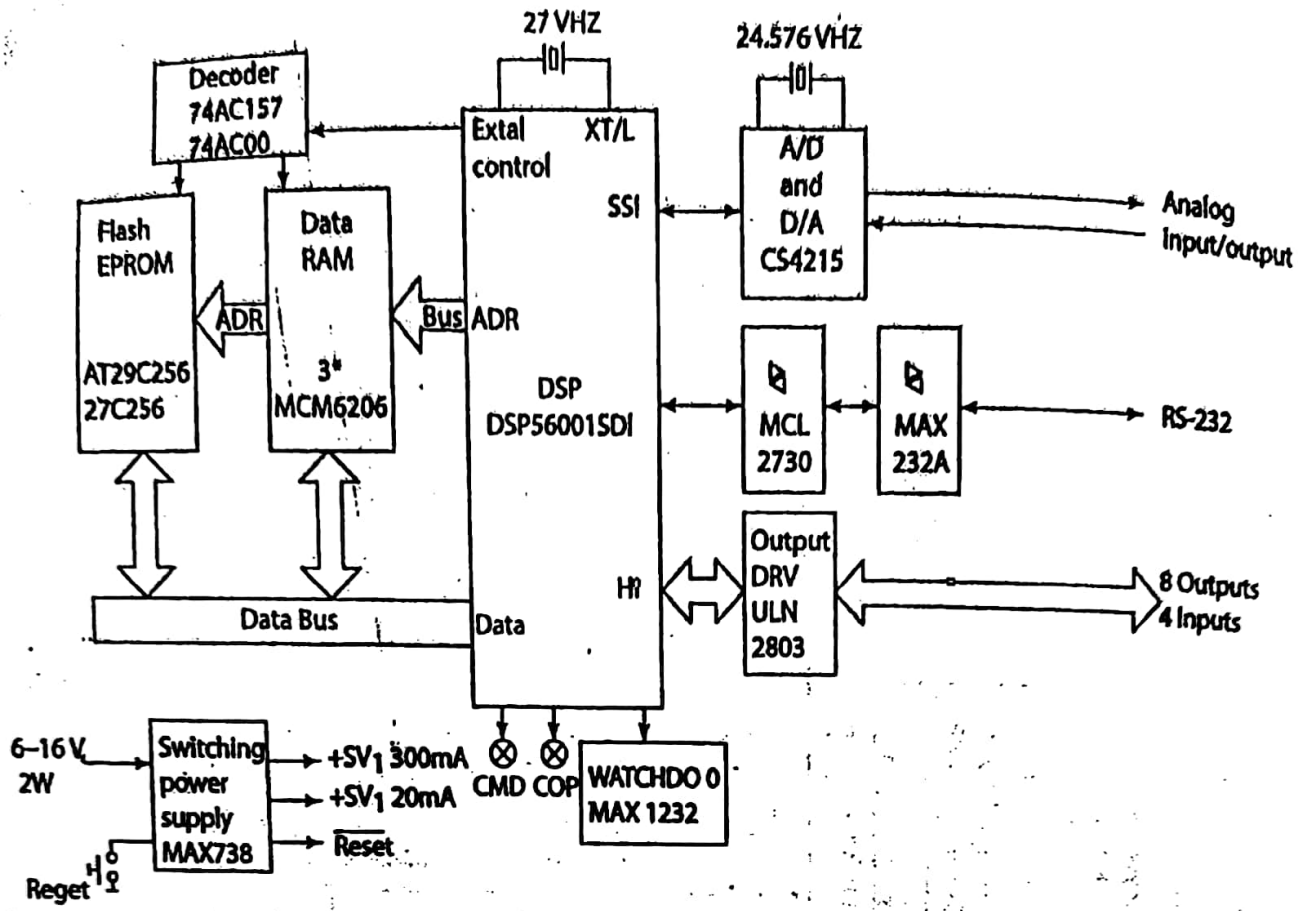


Figure 9.24 | The use of DSP 56001 in a typical layout.

brings up the question: How fast are DSPs? The usual way of answering this question is *benchmarks*, methods for expressing the speed of a microprocessor as a number. For instance, fixed-point systems are often quoted in million integer operations per second (MIPS). Likewise, floating-point devices can be specified in million floating-point operations per second (MFLOPS).

About 150 years ago, British Prime Minister Benjamin Disraeli declared that there are three types of lies: *lies, damn lies* and *statistics*. If Disraeli were alive today and working with microprocessors, he would add *benchmarks* as a fourth category. The idea behind benchmarks is to provide a head-to-head comparison to show which is the best device. Unfortunately, this often fails in practicality, because different microprocessors excel in different areas.

There is an old saying in electronics: "*A specification writer can get twice as much performance from a device as an engineer*". These people are not being untruthful; they are just paid to have good imaginations. Benchmarks should be viewed as a *tool* for a complicated task. If you are inexperienced in using this tool, you may come to the wrong conclusion. A better approach is to look for specific information on the execution speed of the algorithms you plan to carry out. For instance, if your application calls for an FIR filter, look for the exact number of clock cycles it takes for the device to execute this particular task.

When it comes to understanding the execution time, we may mention here that many DSPs can carry out a multiply accumulate operation in a single clock cycle. Since most FIR filters use 25–400 coefficients, 25–400 clock cycles are required, respectively, for each sample being processed. As previously described, there is a small amount of overhead needed to achieve this loop efficiency (priming the first loop and completing the last loop), but it is negligible when the number of loops is large. To obtain the throughput of the filter we can divide the clock rate (say 40 MHz) by the number of clock cycles required per sample. This gives us a

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maximum FIR data rate of about 100 k to 1.6 M samples/s. The calculations cannot get much simpler than this. The calculations are just as easy for recursive filters. Typical FIR filters use about 5–17 coefficients. Since these loops are relatively short, we will add a small amount of overhead, say 3 cycles/sample. This results in 8–20 clock cycles being required per sample of processed data. For the 40 MHz clock rate, this provides a maximum IIR throughput of 1.8–3.1 M samples/s.

Next we come to the frequency domain techniques. FFT subroutines are almost always provided by the manufacturer of the DSP. These are highly optimized routines written in assembly. The specification sheet of a DSP may indicate that a 1024 sample complex FFT requires 18 221 clock cycles, or about 0.46 ms at 40 MHz. To calculate the throughput, it is easier to view this as 17.8 clock cycles per sample. This "per-sample" value only changes slightly with longer or shorter FFTs. For instance, a 256 sample FFT requires about 14.2 clock cycles per sample and a 4096 sample FFT requires 21.4 clock cycles per sample. Real FFTs can be calculated about 40% faster than these complex FFT values. This makes the overall range of all FFT routines about 10–22 clock cycles per sample, corresponding to a throughput of about 1.8–3.3 M samples/s.

FFT convolution is a fast way to carry out FIR filters. In a typical case, a 512 sample segment is taken from the input, padded with an additional 512 zeros and converted into its frequency spectrum by using a 1024-point FFT. After multiplying this spectrum by the desired frequency response, a 1024-point inverse FFT is used to move back into the time domain. The resulting 1024 points are combined with the adjacent processed segments using the overlap-add method. This produces 512 points of the output signal.

How many clock cycles do this take? Each 512 sample segment requires two 1024-point FFTs, plus a small amount of overhead. In round terms, this is about a factor of 5 greater than that for a single FFT of 512 points. Since the real FFT requires about 12 clock cycles per sample, FFT convolution can be carried out in about 60 clock cycles per sample. For a 2106x SHARC DSP at 40 MHz, this corresponds to a data throughput of approximately 660 k samples/s.

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9.7 Interfacing Motor Drives

Interface Boards for Motor Drives

I/O Card or Data Acquisition Card is a hardware module with associated driver software. This can be connected to the computer Bus. A typical I/O card can provide analog input to as many as eight motors. DAC capability is inbuilt into the card (16-bit DAC including a sign bit and +10 V range). 8-channels ADC is also inbuilt into the card. Figure 9.29 indicates a schematic of a motor speed control system using an interface board. I/O board does the task of interfacing the motor side with the computer side.

Drive Units: DC Drives

These are of two types of drive units for DC motor drives: linear amplifiers and pulse-width modulated (PWM) amplifiers.

Motor Drivers

Drivers are required to generate necessary currents to energize the windings of the motors. Angular position and speed of the motor can be controlled by getting a feedback from a speed sensor. Drive units primarily contain a drive amplifier and a DC power supply. Drive is controlled by a control input from a computer. The computer receives feedback signals of the motor motion and generates control signals. Driver parameters such as amplifier gains are software programmable. Sophisticated control schemes can be implemented in addition to typical servo control schemes such as PID. Figure 9.30 is the schematic representation of PWM driver system.

Linear amplifiers have the basic disadvantage of power loss as the output voltages are proportioned in a dissipative way using resistive circuits. Power consumption remains same irrespective of the power consumed by the motor. Efficiency can be made close to unity by using PWM amplifiers. There are two feedbacks. One of speed and another of current. When the load on the motor increases then immediate reaction is an increase in current drawn and a fall in the voltage. Both have to be attended by the PWM amplifier. Here the speed control is much finer than having only one feedback. There are applications where torque is itself the primary output as in the case of metal forming operation, machining, grasping, etc. In digital control more sophisticated combinations of torque and speed can be achieved.

Basic PWM amplifier has inputs from the current sensing and speed sensing devices. Output is the pulse width modulated power supply to run the motor.

Typically, PWM driver consists of speed reference, speed feedback, a differential amplifier and a second stage amplification based on the current feedback from the motor to fine tune the torque performance of

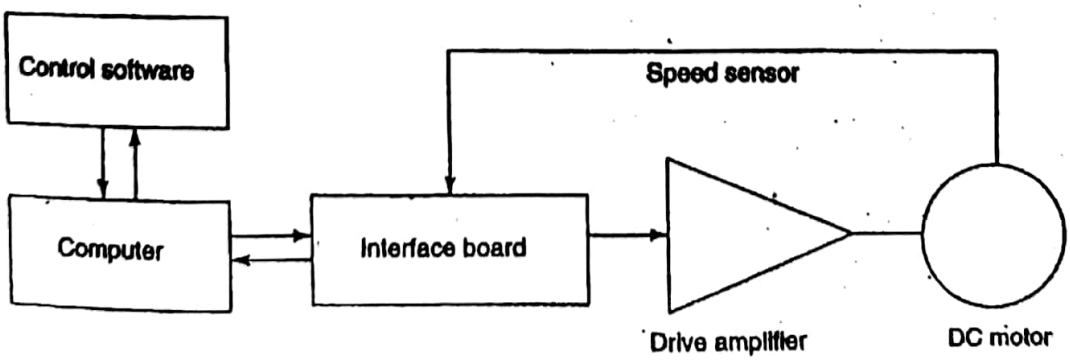


Figure 9.29 | Schematic for motor speed control using I/O Board.

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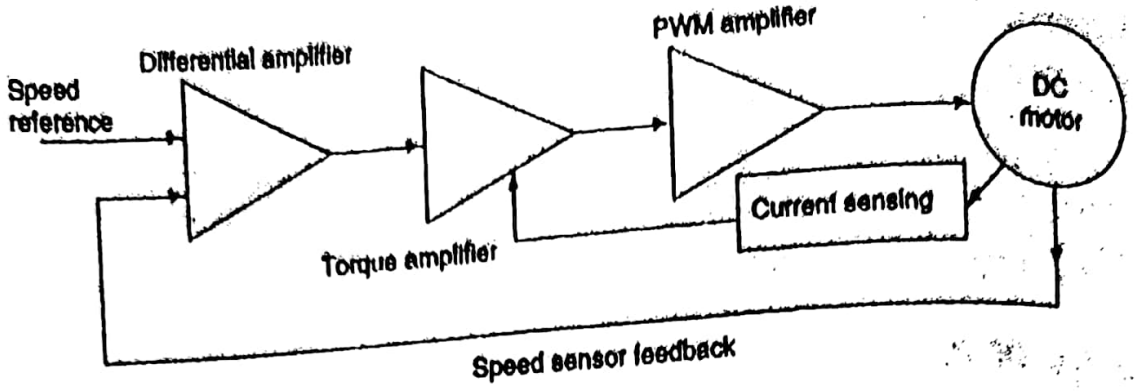


Figure 9.30 | PWM driver system.

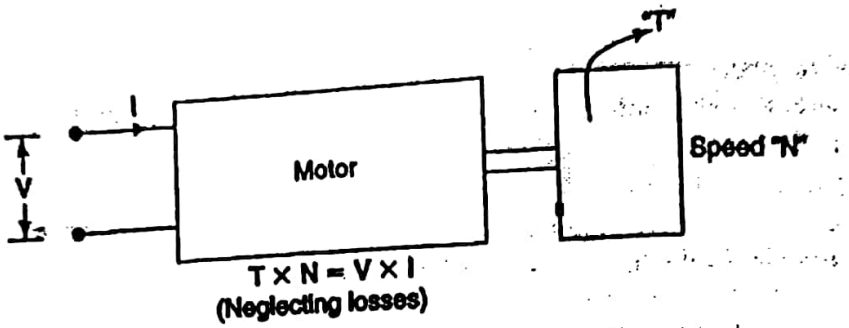


Figure 9.31 | Speed torque relation in a motor (AC or DC).

the motor. PWM driver output is fed to the windings of the motor. PWM is accomplished by varying the duty cycle of the generated pulse signal through switching control as explained next. Final control of the DC motor is achieved either by varying the supply voltage or the field current. Controlling the speed by armature current gives a wider range, whereas field weakening can only change the speed from the nominal operating speed in a small band.

In a typical situation, when the voltage remains constant ; and the torque on the motor increases, the speed decreases and current increases. Figure 9.31 indicates this relation.

These reduction in speed and increase in current together see that power output (mechanical) given by the product of torque and speed is balanced with the power input which is the product of voltage and current (in DC or AC with constant power factor). But the current has to be brought down by increasing the supply voltage as the scope for changing the current is limited by the I^2R losses in the motor. In fact the I^2R losses and the iron losses that can be dissipated safely decide the power rating of the motor. At any point of time the power input to the motor is equal to the product of T and N.

When T increases N falls and I increases. How much N falls and how much I increases depend upon the motor characteristic.

Figure 9.32 shows a typical DC drive. We may observe that digital firing circuit is controlled by current and speed feedbacks.

Variable Frequency Drive (VFD)

VFDs brought the use of AC motors into prominence and reduced the predominance of DC motors in variable speed applications. VFD is the electronic controller designed to change the frequency of supply to the motor. As the frequency supplied to the motor is increased the motor speed increases. In the early

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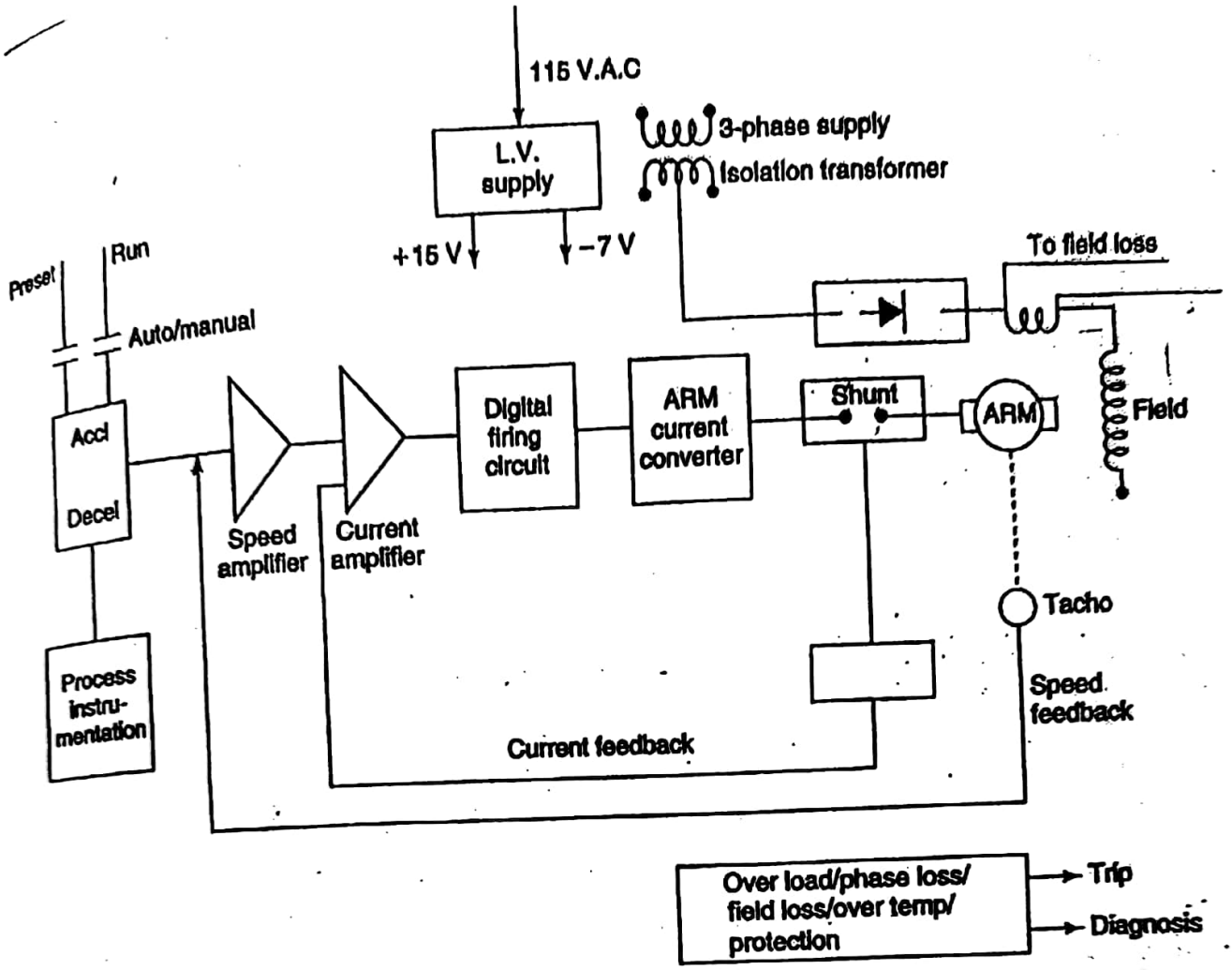


Figure 9.32 | Block diagram of a DC drive.

1960s the VFD was used to control small motors, but in 1980s the drive was extended to cover very large motors as larger transistors became available. Advent of microprocessor control has enabled the VFD to have, in addition to speed control, protection against over-current during ramp up and ramp down conditions.

In large motors the reduction in starting current and associated demand reduction itself reduces the utility bills substantially. Also in applications where the motor has to operate at part loads, for long periods, the savings in energy is very high. One example is primary air fans in utility boilers.

These drivers are available in smaller sizes and are lot effective, efficient and occupy less space. Schematic of a VFD is shown in Figure 9.33. The VFDs has following three main sections:

1. AC–DC converter (rectifier);
2. DC–intermediate section (filter);
3. DC–AC inverter (switching).

Components used are regular transistors, darlington pair transistors, or IGBTs (insulated gate bipolar transistors).

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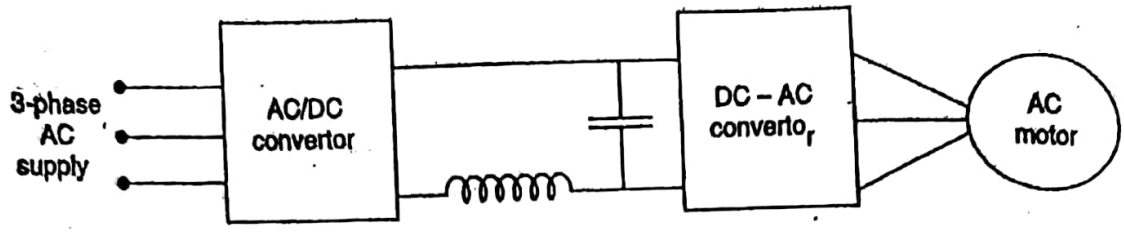


Figure 9.33 | Schematic of a VFD.

Typical VFD

Figure 9.34 shows a typical VFD schematic. In the block diagram, R, S, T terminals are three-phase inputs and UVW are the VFD output to the three-phase motor. These voltages can be 240–400 at low voltage levels and can be 1.1–3.3 kV in power station applications.

Next section would be the filtering of rectified AC before supplying to the inverter.

The inverter stage consists of three pairs of IGBTs which are turned ON and OFF for approximately 12 times in each half cycle by a PWM control circuit. The amplitude will be adjusted so that overall shape of the output wave looks like a sine wave. The frequency can be adjusted between 0 and 120 Hz typically and in some cases between 0 and 400 Hz. The voltage and current of the output would be adjusted to generate the required torque to the motor. The drive maintains a volt to frequency (V/F) ratio so that motor has sufficient power to provide the torque requirements. This ratio can be adjusted slightly to take care of typical load requirements of larger loads at lower speeds.

Terminals indicated are self-explanatory. Stop and start pushbutton switches start the start frequency. Start sequence will provide a slowly increasing ramp of voltage and frequency to start the motor slowly.

Drive enable contacts can be controlled by an external control relay. A jog pushbutton will run the motor at a jog speed written into the program. External switches SW1, SW2 and SW3 provide fixed speeds as entered into the program. A specific application may require the motor to operate at three fixed speeds for three specific operations. These can be selected by the operator. An external potentiometer 0–10 kΩ can be used along with 0–10 V input or 4–20 mA input to generate any speed from 0% to 100%.

The serial ports for communication and for operator interface are provided. Serial communication can be used for reloading the parameters from a portable computer.

One advantage of VFD is its ability to run in the reverse direction without using expensive reversing motor starters. This is accomplished by changing the input phase sequence obtained by changing the timing logic. Provision is also provided for braking the motor. VFD is basically an open loop controller, with motor supplied at different frequency levels for larger speed variations and torque and speed ranges dictated in a small band by the induction motor characteristic.

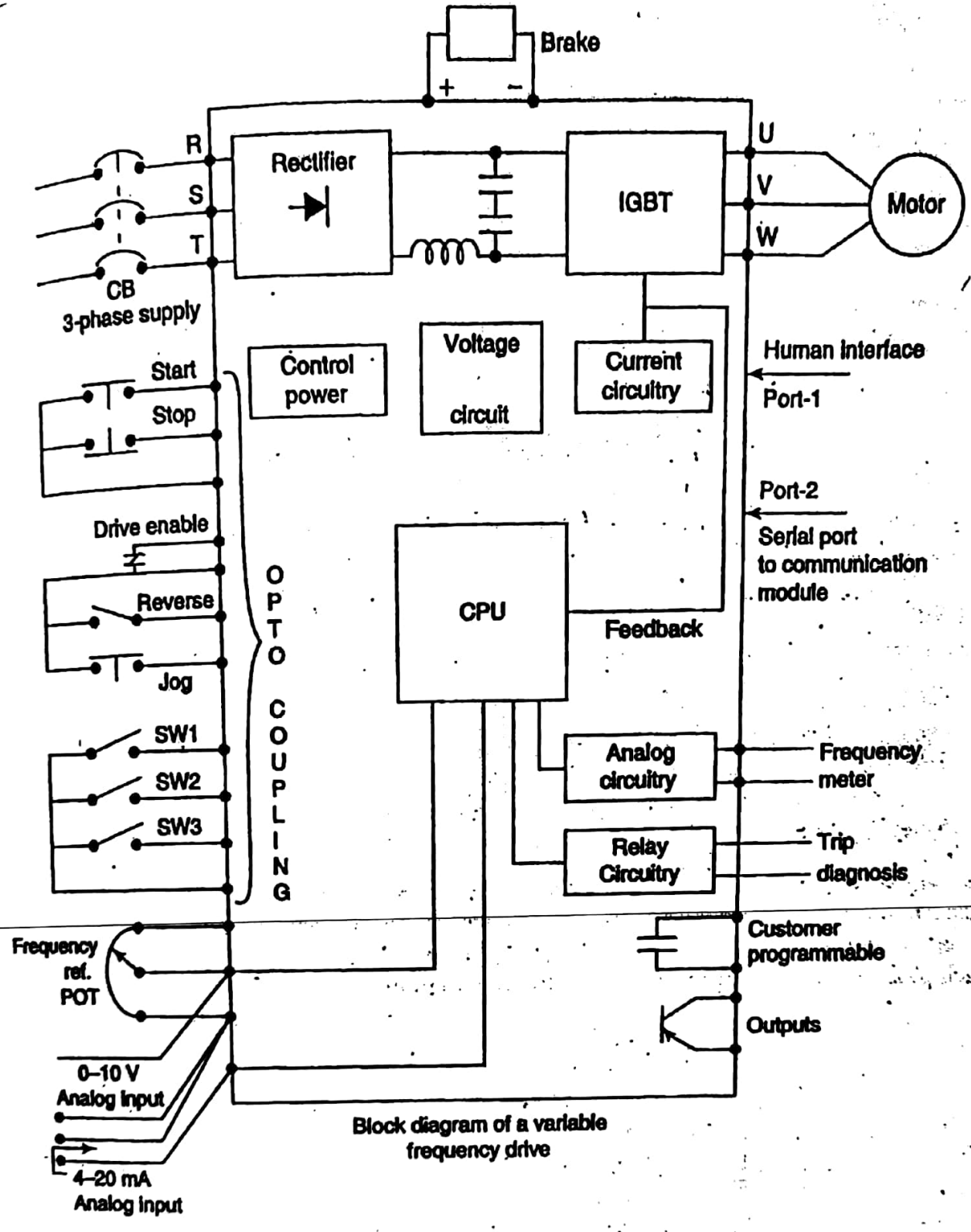
Scalar and Vector Drives

Some manufacturers provide additional circuits inside the drive to bring in the closed loop feedback signals from encoders or resolvers. These circuits decode the signals from the sensors and scale them to the required level, This makes the drive operate like a package. This helps the designer to immediately put a system together where the components match. Such drives are called vector drives by "Allen Bradley". Scalar drives of "Allen Bradley" can be operated either on open loop or on closed loop.

Stepper Motor Driver and Controller

A stepper motor is basically an open loop actuator. Stepwise rotation of the motor is synchronized with the command pulse train. Because of this, this is also called digital synchronous motor. Basic schematic is as shown in Figure 9.35.

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Block diagram of a variable frequency drive

Figure 9.34 | Block diagram of a VFD.

The basic components are identified in the diagram. Main basic component is a translator to interpret the command pulses and switch the analog circuits to generate the high currents required by the windings of the stepper motor.

The command pulses are generated either by a control computer, microprocessor or a variable frequency oscillator (hardware approach). For bidirectional motion two pulse trains are required; the position pulse train and direction pulse train. For steady-state operation, the stepping rate can be set manually, adjusting the potentiometer connected to the translator to get simple motions (e.g. starting from rest and stopping after

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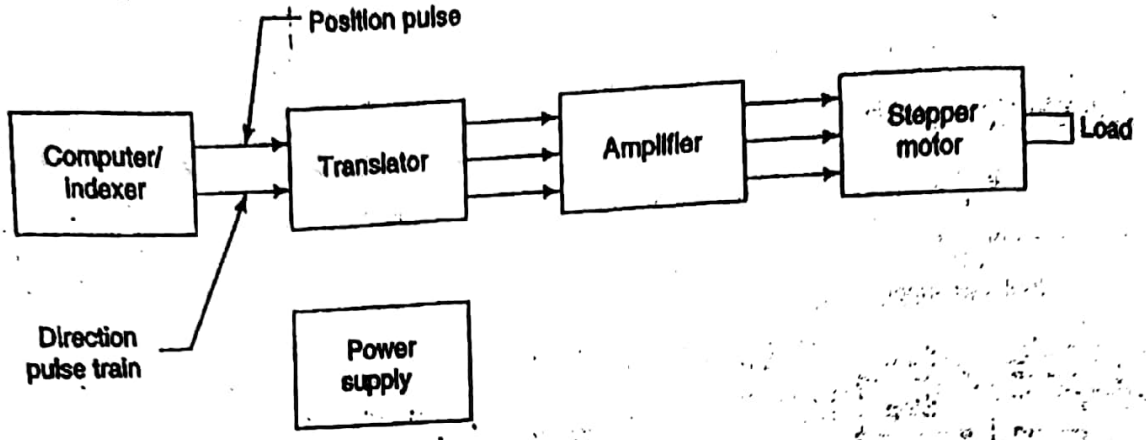


Figure 9.35 | Basic components of a stepper motor driver.

a predetermined angular position). Under more complex projections, computer based generation of pulse commands would be required.

Drive Unit

The driver hardware consists of the following components:

1. The drivers for stepper motors contain the digital hardware to interpret the information carried by the stepping pulse signal and the direction pulse signal, and provide appropriate signals to the switches that actuate the phase windings of the motor.
2. Drive circuits for phase windings with switching transistors to actuate the phases.
3. Power supply to the phase winding.

These components are commercially available as single packages to operate corresponding class of stepper motors. An integrated heat sink is also provided to dissipate the heat generated in the hardware. Figure 9.36 indicates a unipolar drive (no current reversal in a phase winding). So the windings have two coil segments for each phase. Consequently, the motor has five input points. The translator generates the proper logic to

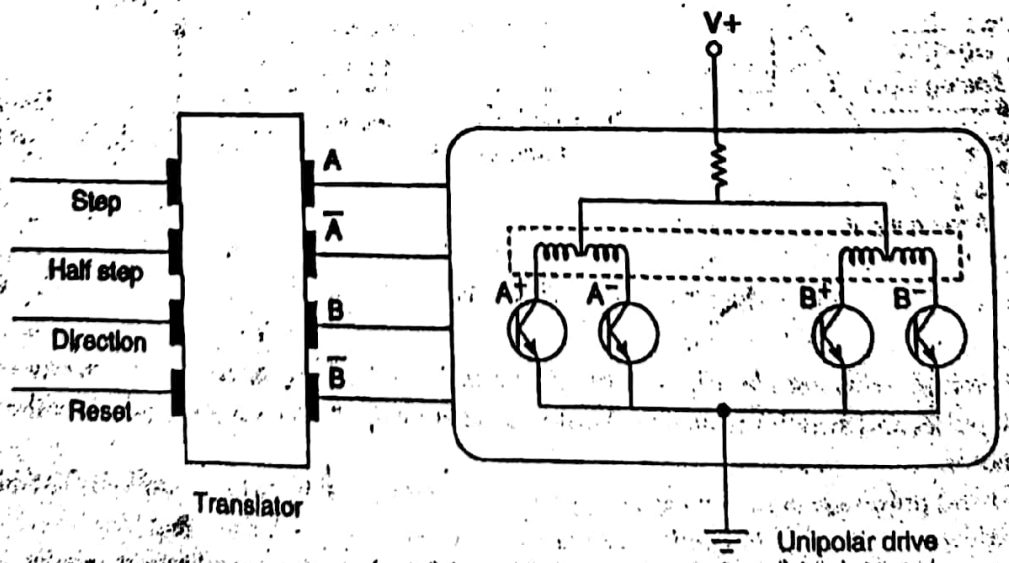


Figure 9.36 | Drive hardware for bifilar wound stepper motor.

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