3.a Switching characteristics of Devices

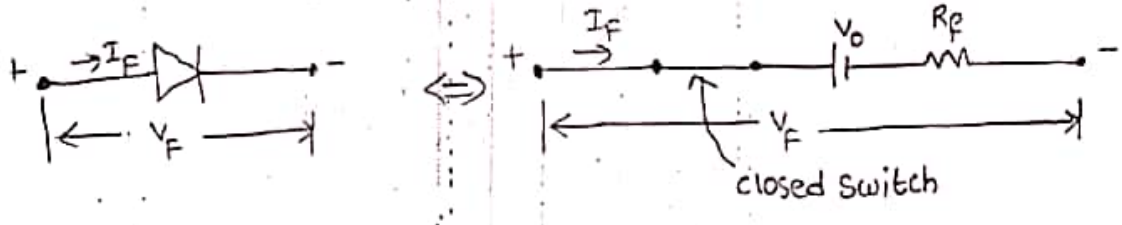
G. Venkata Hanuman
Asst. Prof

Diode as a switch :-

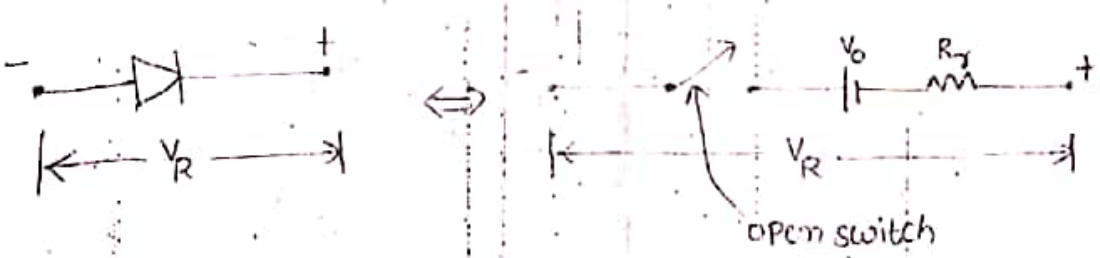
The diode conducts when it is in forward biased and blocks conduction when it is in reverse biased, it can function as an electronic switch.

Let V_0 = barrier potential, R_f = forward resistance of a practical diode

If a forward bias voltage $V_F > V_0$ is applied, as shown, the diode readily conducts, and a forward current I_F results.



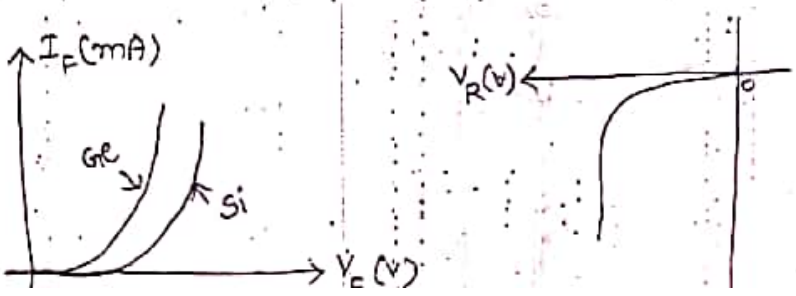
A reverse biased Junction diode as shown in fig. below



V_R is reverse voltage, diode is in reverse biased, so it does not conducts the reverse saturation current (μA) flows through the circuit.

V-I characteristics

The forward and reverse V-I characteristics of a P-n Junction diode as shown in fig. below



cut-in voltage for Ge → 0

Si → 0.7V

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Diode current equation

$$I_D = I_0 \left[e^{(KV_D / T_K)} - 1 \right]$$

where $I_0 \rightarrow$ Reverse saturation current.

$V_D \rightarrow$ External bias voltage

$T_K \rightarrow$ Temperature in ^oK

$K \rightarrow \frac{11600}{\eta}$ $\left.\begin{matrix} \therefore \eta = 1 \rightarrow Ge \\ \eta = 2 \rightarrow Si \end{matrix}\right\}$ For low levels of diode current

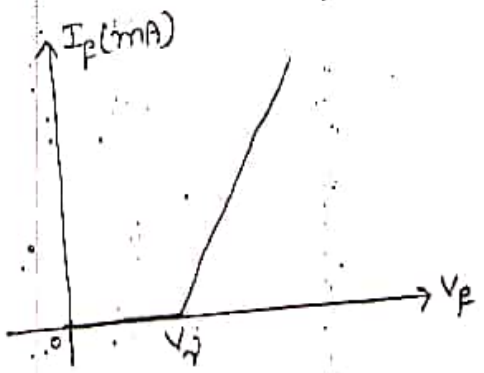
and $\eta = 1 \rightarrow$ For high levels of diode current

For +ve values of $V_D \rightarrow$ diode in forward bias condition, $I_D \rightarrow$ +ve and it Increases exponentially.

For -ve values of $V_D \rightarrow$ diode in reverse bias condition, $I_D \rightarrow$ equals to $-I_S$, the reverse current which remains constant in magnitude until breakdown occurs.

Piece wise linear diode characteristics

The piece wise linear approximation for a semiconductor diode characteristics as shown in fig. below



The break down is at V_γ, which is called the threshold voltage.

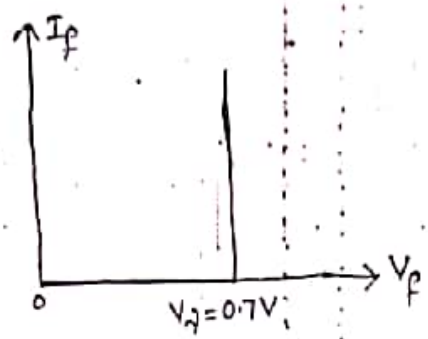
→ If $V_f < V_\gamma$, the cut-in voltage, $I_f = 0$ hence no conduction for $V_f < 0.7V$.

→ If $V_f > 0.7V$, I_f Increases linearly w.r.to V_f.

forward resistance is given as $R_f = \frac{\Delta V_f}{\Delta I_f}$

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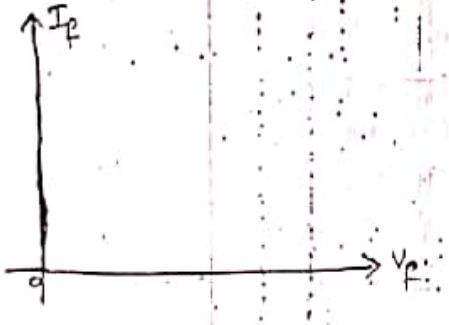
If $R_f << R_s$, the circuit resistance can be Ignored, the piece wise linear characteristics can be modified as



From graph,

$R_f = 0$, $I_f = 0$ for $V_f < 0.7V$

For an Ideal diode, cut in voltage $V_\gamma = 0$, $R_f = 0$. The piece wise linear characteristics as shown in fig.

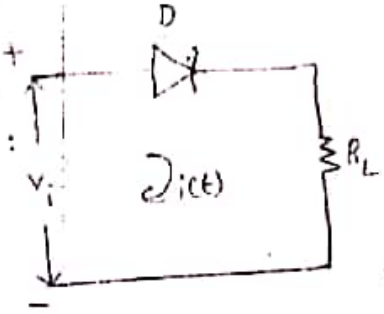


From graph,

$V_\gamma = 0$, $R_f = 0$

Diode Switching times :-

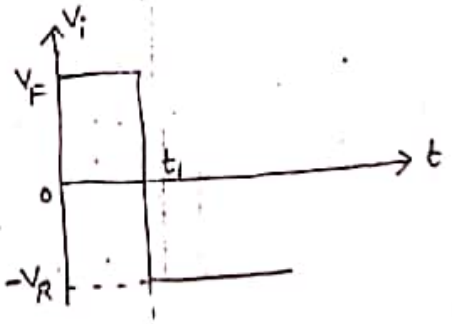
Consider a p-n Junction which is in the conducting mode. Let the current through the device be I_F.



$I_F = \frac{V_F}{R_L}$

$I_R = \frac{V_R}{R_L}$

The output waveforms as shown in fig. below



where,

$I_F \rightarrow$ diode forward current

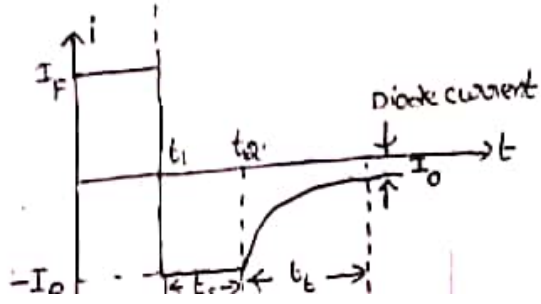
$-I_R \rightarrow$ Diode reverse current

$I_0 \rightarrow$ Reverse Saturation current

$t_s \rightarrow$ storage time

$t_t \rightarrow$ transition time

$t_{rr} \rightarrow$ Reverse recovery time



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operation :-

when a forward bias is applied, holes from the P-region diffuse in n-region, electrons from the n-region to P-region, current I_F flows. In these new regions, they constitutes minority charge carriers.

A Reverse voltage is applied at $t = t_1$, it act as forward voltage for the large no of minority carriers progressing through the junction, it results current simply reverses making $I_R = I_F$.

certain time is needed for these minority charge carriers to move into the other region of P-n junction and becomes majority charge carrier This time Interval, denoted as t_s is termed as "storage time."

During this Period of transition, the reverse current stays at the same level I_R, after this transition has passed off, at $t = t_2$, the reverse current decreases exponentially for a time t_t, at the end of which it is equal to I_0, the reverse saturation current. The time Interval t_t is termed as transition time.

The reverse recovery time is the sum of storage time and transition time

$$t_{rr} = t_s + t_t$$

Transistor as a switch :-

A Transistor can be used as a switch. It has 3 regions of operation:

1. cut-off region
2. Active region
3. saturation region

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cut-off region :- The emitter-base Junction and collector-base Junctions are reverse biased, the transistor operates in cut-off region and it act as open switch.

2. Active region :- The emitter-base Junction is forward bias and collector-base Junction is reverse biased, the transistor operates in Active region and it act as Amplifier.

3. Saturation region :- when both emitter-base Junction and collector-bas Junctions are forward biased, and it act as closed switch.

when the transistor is switched from cut-off to saturation and from saturation to cut-off with negligible active region, the transistor is operated as a switch.

when the transistor is in saturation region, voltages are zero and currents are maximum. when the transistor is in cut-off region, voltages are maximum and currents are zero.

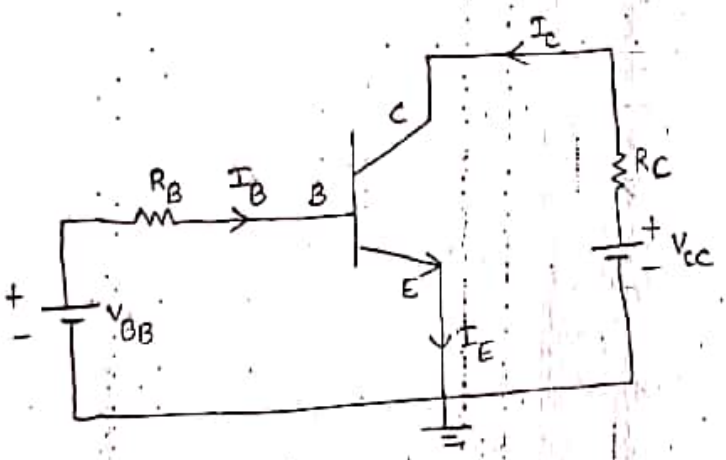


Fig :- Transistor used as a switch

The transistor is operating in common emitter mode, I_B is Input current, I_C is output current, V_{BE} is Input voltage, V_{CE} is

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Apply KVL, to the output circuit,

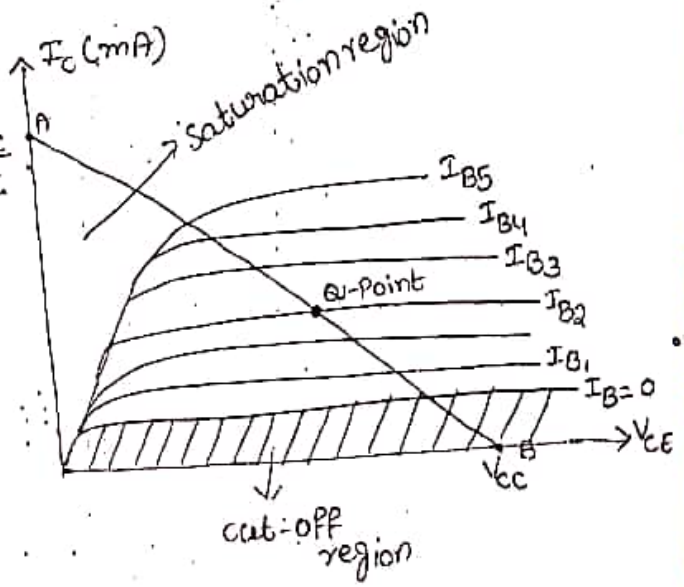
$$V_{cc} = I_c R_c + V_{CE} \quad \text{(or)} \quad V_{CE} = V_{cc} - I_c R_c$$

—①

To plot the output characteristics, Input current I_B is kept consta

A graph is drawn between, output current I_c and out put voltage V_{CE} at constant I_B.

The out put characteristics, as shown in fig. below



The d.c load line, is obtained as

i) when $I_c = 0$,

$\Rightarrow V_{cc} = 0 + V_{CE}$

$\Rightarrow V_{cc} = V_{CE}$

Therefore, V_{cc} is placed on x-axis.

ii) when $V_{CE} = 0$, $V_{cc} = I_c R_c$

$\Rightarrow I_c = \frac{V_{cc}}{R_c}$

Therefore, the coordinates of 'A' are $I_c = \frac{V_{cc}}{R_c}$ is placed on y-axis.

from fig, 'Q' is ~~the~~ located at the mid point of the d.c load line AB between saturation and cut-off regions i.e Q is exactly between A and B.

The line is drawn between A and B points it is called as d.c load line. Point 'A' denotes saturation and Point 'B' denotes cut-off region.

The point of Intersection of the load line with an output characteristic is called operating point (or) Quiescent Point (or) Q-Poin

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Transistor Switching times :-

consider the transistor as it makes transition from one state to other, consider the transistor as a switch circuit.

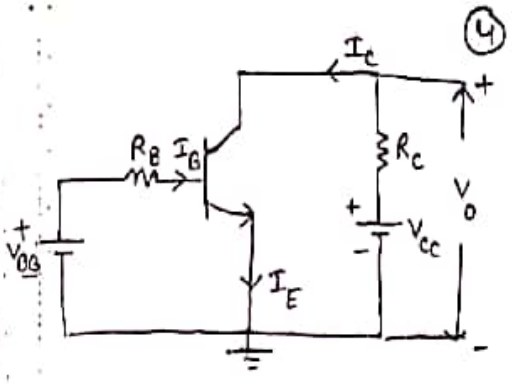
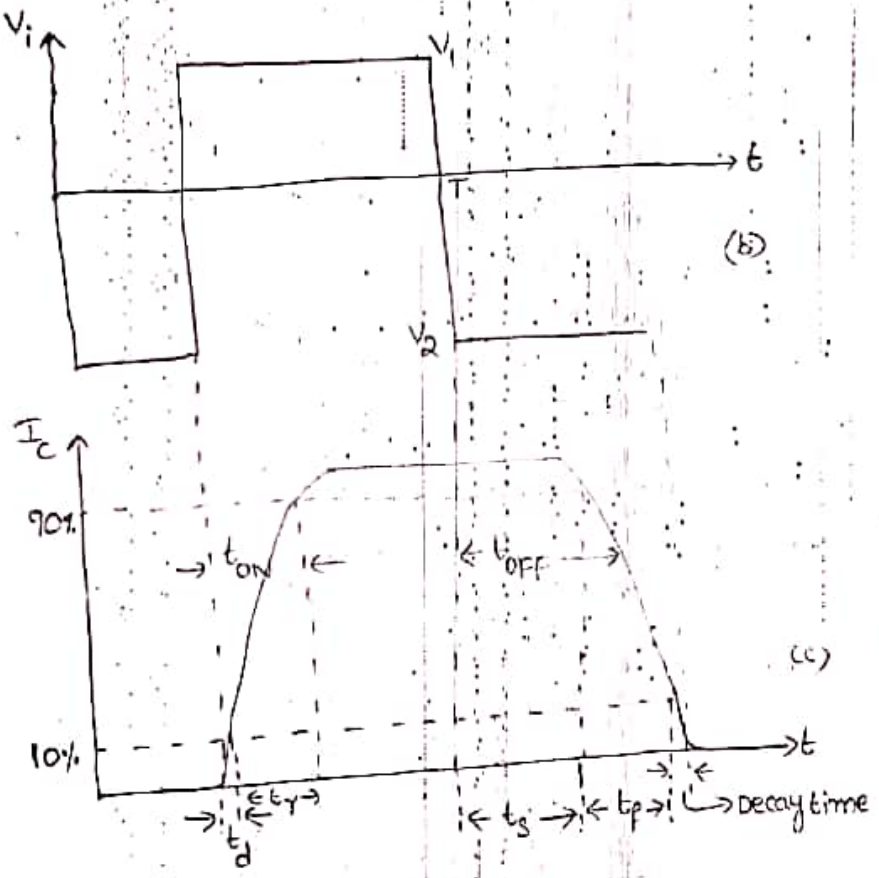


Fig:- Transistor as a switc

Let the Input current I_B be a pulse as shown. The variation of the output current I_c with time as shown in fig. below



t_r → Rise time
t_f → fall time
t_d → delay time
t_s → storage time
t_{ON} → Turn-on time
t_{OFF} → Turn-off

Fig:-b) Input waveform and c) response of collector current

From figure (b), the pulse waveform makes transitions between the voltage levels V_1, V_2. At V_1 the transistor is in saturation region, At V_2 the transistor is in cut-off region.

The Input waveform is applied between the base and emitte through R_B. The collector current does not respond Immediately to the

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Input signal is applied, it takes some time.

Delay time (t_d):- The time required for the collector current to change from zero to 10% of maximum current is called delay time.

Rise time (t_r):-

The time required for the collector current to rise from 10% to 90% of its maximum current is called Rise time.

TURN-ON time (t_{ON}):-

The sum of delay time and rise time is called turn-ON time

$$t_{ON} = t_d + t_r$$

Storage time (t_s):-

The time interval during which the collector current drops from maximum to 90% of the saturation current is called storage time.

Fall time (t_f):-

The time required for the collector current to drop from 90% to 10% of the saturation current is called fall time.

Turn-OFF time (t_{OFF}):-

The sum of storage time and fall time is called transistor turn-off time

$$t_{OFF} = t_s + t_f$$

Decay time:- The time for which the collector current I_c falls from 10% of its maximum value to the level of I_{CBO} is considered while evaluating t_{OFF}. This interval is called decay time, it is very small,

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Breakdown voltage consideration of a transistor :-

When the transistor is in saturation, the voltage at collector i.e $V_{CE} = 0$, and when it is cut-off, $V_{CE} = V_{CC}$. Thus collector voltage V_{CE} changes between the limits 0V & V_{CC}.

A Reverse-bias voltage is applied across the collector-base junction of a transistor, keeping the emitter lead open-circuited. A small reverse current flows and this remains practically unchanged in magnitude, even if the reverse voltage is Increased. However there is a certain maximum reverse-bias voltage at which the junction breaks down. This termed as "Breakdown voltage", denoted as BCV_{BO}

The Breakdown voltage is a transistor, not depending on other factors. It is mainly due to phenomenon of "Avalanche breakdo

The current I_{CO} which crosses the junction normally in the absence of breakdown gets multiplied by a factor 'M' which may be quite large.

At the breakdown voltage Bc BV_{CBO}, current through the collector-base junction is MI_{CO}

The avalanche multiplication factor M, depends on voltage V_{CB} is given by

$$M = \frac{1}{1-\left(\frac{V_{CB}}{BV_{CBO}}\right)^n} \quad -(1)$$

n → parameter, range from 2 to 10

For large values of n, M is very nearly unity until V_{CB} approac

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when $V_{CB} = BV_{CBO}$, m becomes infinite.

In common base mode of operation, the collector current

$I_C = \alpha I_E$ where $\alpha \rightarrow$ current gain.

If avalanche multiplication is taken into consideration, then $I_C = m\alpha I_E$

$$\Rightarrow I_C = \alpha' I_E \quad [\because \alpha' = m\alpha] \quad -(2)$$

For common-emitter mode operation,

$$\beta \text{ (or) } h_{fe} = \frac{\alpha}{1-\alpha}, \text{ in presence of Avalanche multiplication}$$

$$h'_{fe} = \frac{\alpha'}{1-\alpha'} = \frac{m\alpha}{1-m\alpha} \quad -(3) \quad [\because \alpha' = m\alpha]$$

If $m\alpha = 1$, current gain h'_{fe} becomes Infinite.

The Base current is kept constant, breakdown occurs at the voltage V_{CB} which satisfies the equation,

$$m = \frac{1}{1-\left(\frac{V_{CB}}{BV_{CBO}}\right)^n} = \frac{1}{\alpha} \quad -(4)$$

$$\boxed{V_{CB} = BV_{CBO}\sqrt[n]{1-\alpha}} \quad -(5)$$

w.k.T $V_{CE} = V_{CB} + V_{BE}$

V_{BE} is quite small, $V_{CE} = V_{CB}$

$$\Rightarrow \boxed{V_{CE} = BV_{CBO}\sqrt[n]{1-\alpha}} \quad -(6)$$

w.k.T $h_{fe} = \frac{\alpha}{1-\alpha} \Rightarrow 1-\alpha = \frac{\alpha}{h_{fe}} = \frac{1}{h_{fe}} \quad -(7)$

substitute eq (7) in (6)

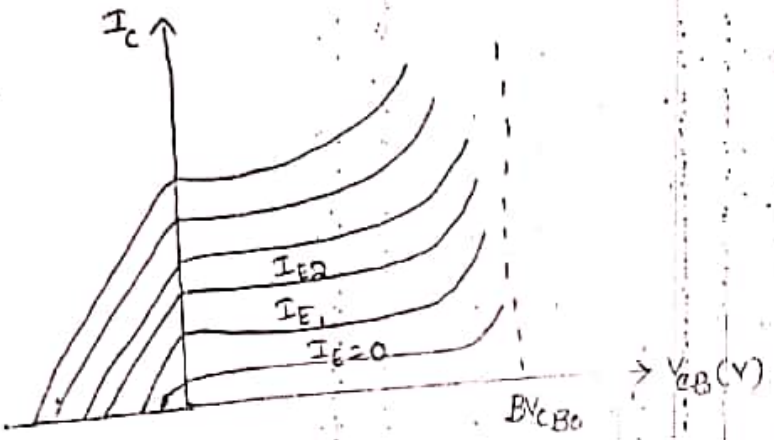
$$V_{CE} = BV_{CBO}\sqrt[n]{\frac{1}{h_{fe}}} \quad -(8)$$

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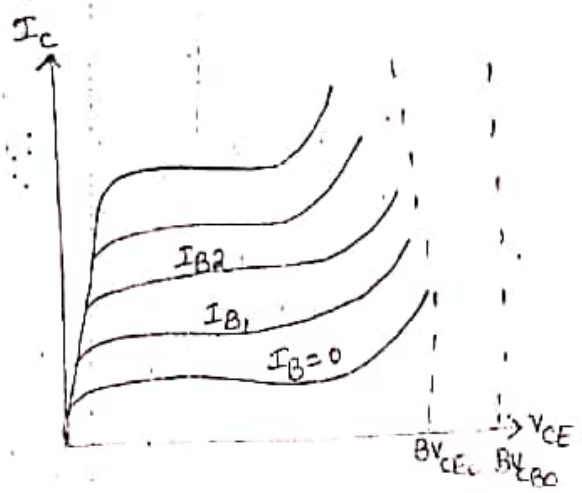
The collector-to-emitter break down voltage, with open circuited base, BV_{CEO} is

$$BV_{CEO} = BV_{CBO} \sqrt{\frac{1}{h_{fe}}} \quad \text{—(9)}$$

The CB characteristics have been extended into breakdown region. The curve for $I_E = 0$ is a plot as a function of V_{CB} and CE characteristics have been extended into breakdown region. The curve for $I_B = 0$ is shown in fig. below.



a) CB characteristics



b) CE characteristics

Saturation parameters of transistor:-

When a transistor is in saturation, the current is given a $\frac{V_{cc}}{R_L}$. As R_L is kept small in order to minimise the time of chargin of the capacitor. The collector supply voltage V_{cc} is small, if the transistor current is to be with in the permissible limits, as specified by the manufacturer.

The total voltage swing at the transistor switch is given as $[V_{cc} - V_{CE(sat)}]$.

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$V_{CE(sat)}$ is the collector-to- [illegible] in saturation.

Generally, V_{cc} is fixed. Hence, in order to have max. output voltage swi it is essential that $V_{CE(sat)}$ is small as practicable.

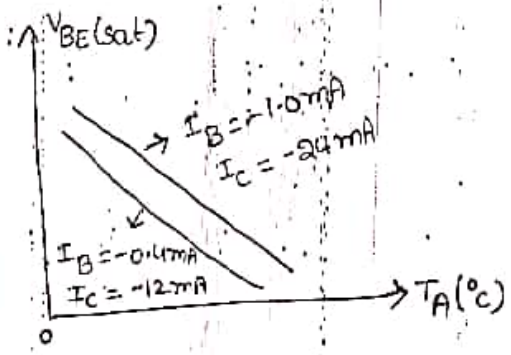
Saturation resistance (R_{CS}) (or) $R_{CE(sat)}$

When a transistor is in saturation, a quantity, usually referred to as common-emitter saturation resistance, is defined as the ratio $[V_{CE(sat)}/I_C]$.

Its value depends not only on the operating point, but also semiconductor material & type of construction of the transistor.

Temperature variation of saturation parameters :-

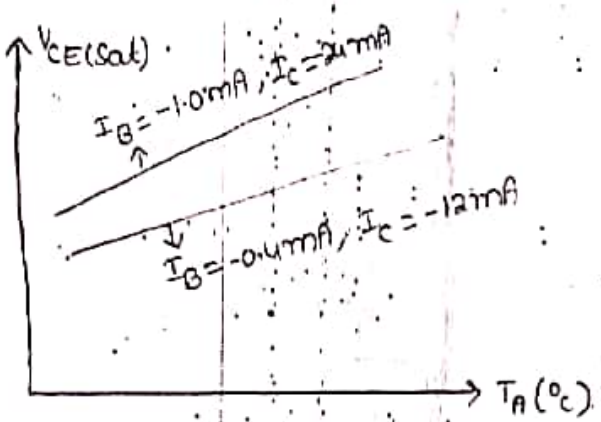
→ At constant base and collector currents, the forward base-to-emitter voltage V_{BE} has a typical temperature sensitivity in the range -1.5 to -2 mV/°c. This applies both silicon and Ge transistors A plot of Ge of V_{BE} versus ambient temperature as shown in fig. below



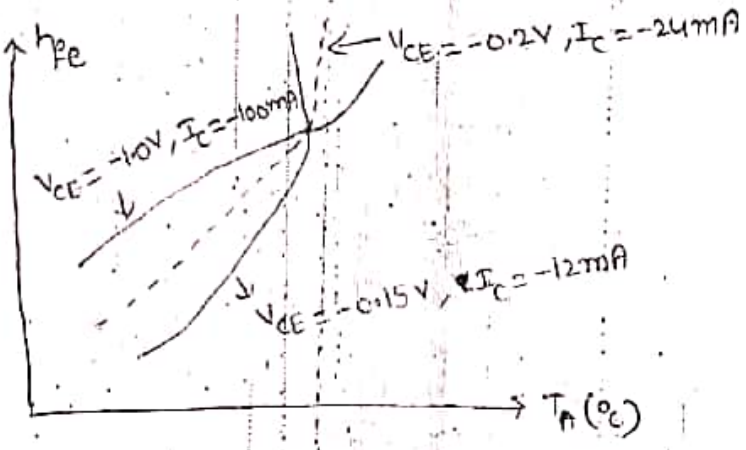
→ When a transistor is in saturation, both emitter-base and collector-base junctions forward biased. The transistor can be visualised at two forward biased diodes, joined back-to-back in series opposition. Hence, there is a change of temperature,

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the changes of voltage in two junctions practically cancel out, with the result $V_{CE(sat)}$ practically remains unaltered.

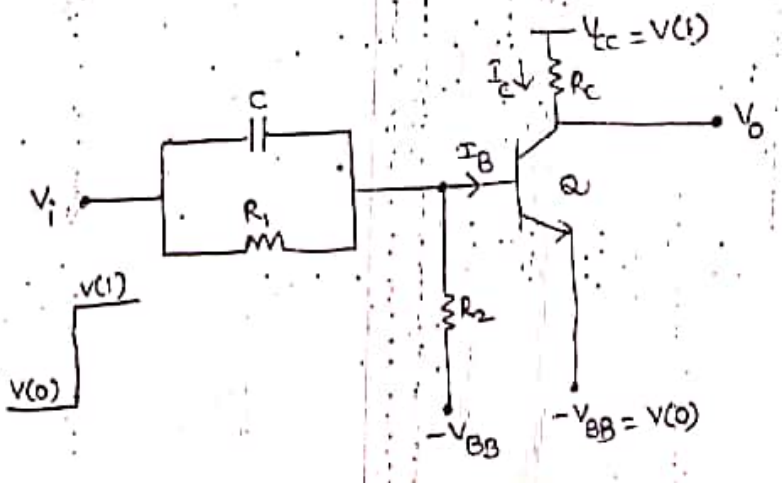


→ At small and moderate currents, h_{fe} increases substantially with increase of temperature. at high currents, h_{fe} becomes more (or) less insensitive to changes of temperature.



Design of transistor switch :-

A transistor has a inversion property. It can be used as a Inverter.



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Transistor is operated as an inverter, so when input voltage is low (logic 0) the output is high (logic 1), when Input is high the output is low.

The Input is a step voltage, i.e V_i either Low [V(0)] (or) high [V(1)]

For low Input, $V_i = V(0)$, the transistor is at cut-off, so the output is V_{CC} i.e V(1).

For High Input, $V_i = V(1)$, the transistor is at saturation, So the output is $V_{CE(sat)}$ i.e V(0)

when V_i is at V(0), the base voltage is (open circuit)

$$V_B = -V_{BB}\frac{R_1}{R_1+R_2} + V(0)\frac{R_2}{R_1+R_2}$$

If V(0) = 0V,

$$V_B = -V_{BB}\frac{R_1}{R_1+R_2}$$

[∵ Apply KVL at output

$V_{CC} = I_C R_C + V_{CE}$

$\Rightarrow I_C = \frac{V_{CC} + V_{CE}}{R_C}$]

when $V_i = V(1)$, transistor is in saturation,

$$I_C = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

we know that from hybrid-π model,

$$I_C = I_{B(min)} \cdot h_{fe(min)}$$

$$I_{B(min)} = \frac{I_C}{h_{fe(min)}}$$

$$= \frac{V_{CC} - V_{CE(sat)}}{R_C \cdot h_{fe(min)}}$$

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The current through Resistor R_1 is

$$I_1 = \frac{V(1) - V_{BE(sat)}}{R_1}$$

The current through resistor R_2, is

$$I_2 = \frac{V_{BE(sat)} - (-V_{BB})}{R_2}$$

∴ Base current I_B = current through I_1 – current through I_2

$$\frac{V_{cc} - V_{CE(sat)}}{R_c h_{fe(min)}} = \frac{V(1) - V_{BE(sat)}}{R_1} - \frac{V_{BE(sat)} - (-V_{BB})}{R_2}$$

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3.5 Bistable multivibrator

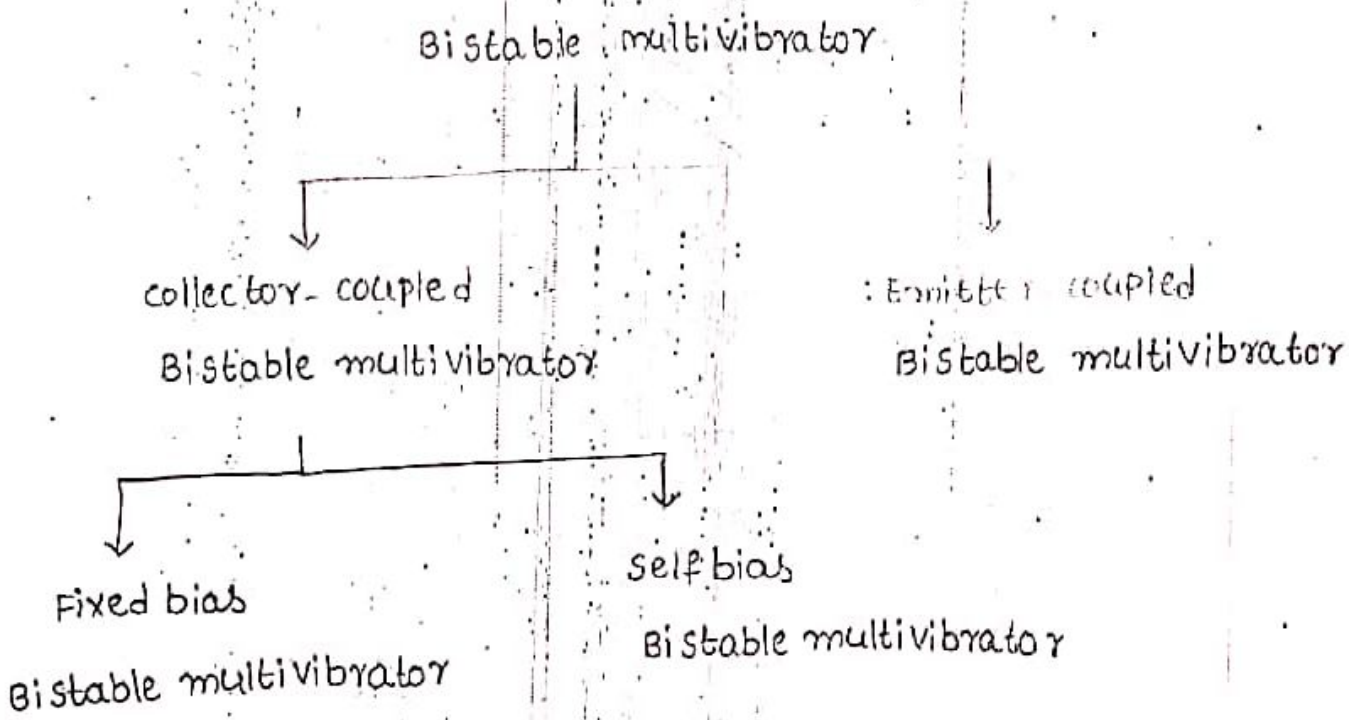
multivibrator means A circuit which can oscillate at a no of frequencies is called multivibrator.

→ Bistable multivibrator consists of two stable states.

→ In Bistable multivibrator coupling elements are resistors.

→ It contains basic memory element. It used to perform many digital operations such as counting and storing of binary data.

→ mainly used in pulse circuits. They are mainly used in gating (or) delay circuits.



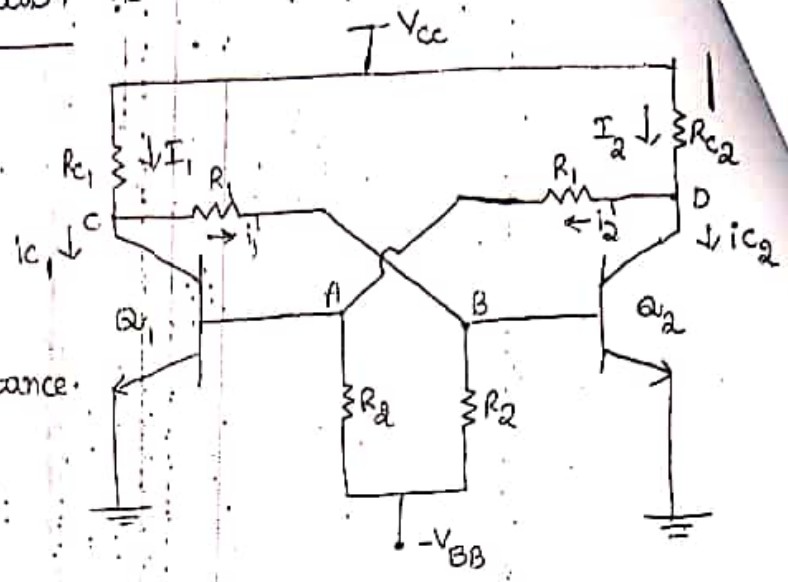
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Fixed bias Bistable multivibrator :-

Q_1, Q_2 are Identical transistors (npn).

R_1, R_2 are resistors

R_{C1}, R_{C2} are collector load resistance.



The output of First amplifier is coupled to the Input of second Amplifier and the output of second amplifier is coupled to the Input of first amplifier.

In one stable state Q_1 is ON and Q_2 is OFF and other stable state Q_1 is OFF and Q_2 is ON. Both the transistors conducting simultaneously and carrying current I_1, I_2.

operation:-

Let us consider transistor Q_2 starts conducting as the current I_1 Increases Q_2 gradually goes into saturation region simultaneously Q_1 goes into cut-off region. Then the total multivibrator goes into one stable state i.e Q_1 OFF and Q_2 ON. And to change the multivibrator from one stable state to another stable state, we applying external triggering either at base (or) at collector terminal of transistor.

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If the transistor is ON then output voltage, $V_0 = V_{CE(sat)}$.

If the transistor is OFF then the output voltage is $V_0 = V_{cc}$.

If a transistor is in OFF state, its collector current is zero and collector voltage is V_{cc}. If a transistor is in ON state, its collector current is maximum and collector voltage is zero.

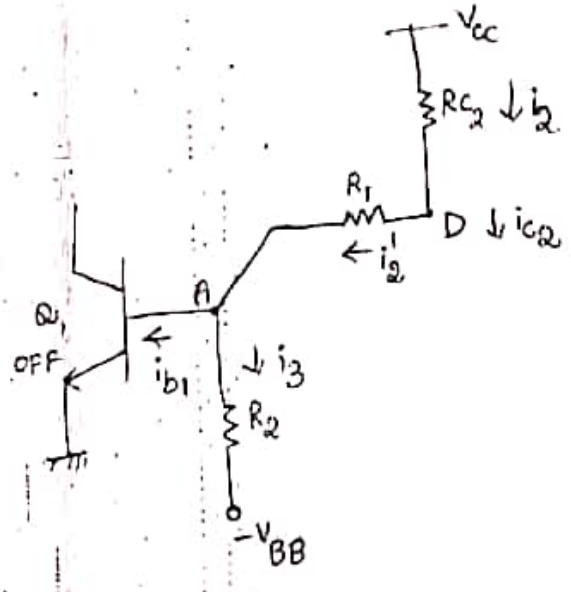
During a switching transient, transistor Q_2 is ON and Q_1 is OFF.

Q_2 ON, V_{c2} (or) $V_D = V_{CE(sat)} = 0V$

V_{B2} (or) $V_B = V_{BE(sat)} = 0V$

To find i_2, i_2', i_{c2}:-

$$i_2 = \frac{V_{cc} - V_D}{R_{c2}}$$



Since Q_1 OFF, $i_{B1} = 0$

Apply KCL at node A,

$$i_2' = i_3 + i_{b1}$$

$$i_3 = i_2'$$

But $i_2' = \frac{V_0 - (-V_{BB})}{R_1 + R_2} = \frac{V_0 + V_{BB}}{R_1 + R_2}$

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Apply KCL at node D,

$$i_2 = i_2' + i_{C2}$$

$$i_{C2} = i_2 - i_2'$$

$$\boxed{i_{C2} = \frac{V_{CC} - V_D}{R_{C2}} - \frac{V_D + V_{BB}}{R_1 + R_2}}$$

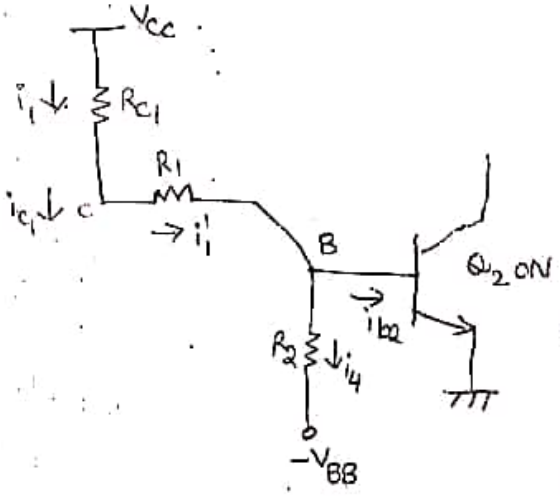
from the circuit,

$$i_3 = \frac{V_A - (-V_{BB})}{R_2} = \frac{V_A + V_{BB}}{R_2}$$

$$\Rightarrow \boxed{V_A = V_{B1} = -V_{BB} + i_3 R_2}$$

Find i_{b2}

Q_1 is OFF, $i_{C1} = 0$



Apply KCL at node 'C',

$$i_1 = i_{C1} + i_1'$$

$$\Rightarrow \boxed{i_1 = i_1'}$$

Apply KCL at node 'B',

$$i_1' = i_{b2} + i_4$$

$$i_{b2} = i_1' - i_4$$

$$i_{b2} = i_1 - i_4 \quad [\because i_1 = i_1']$$

$$i_1 = i_1' = \frac{V_{CC} - V_B}{R_{C1} + R_1}$$

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$$i_4 = \frac{V_B - (-V_{BB})}{R_2} = \frac{V_B + V_{BB}}{R_2}$$

$$i_{b2} = i_1 - i_4$$

$$\boxed{i_{b_2} = \frac{V_{cc} - V_B}{R_{c_1} + R_1} - \frac{V_B + V_{BB}}{R_2}}$$

From the circuit,

$$i_1 = \frac{V_{cc} - V_c}{R_{c_1}}$$

$$\boxed{V_c = V_{c_1} = V_{cc} - i_1 R_{c_1}}$$

The stable state voltages and stable currents are V_{B1}, V_{C1}, i_{b2}, i_{c2} respectively.

we know that $i_{b2(min)} = \frac{i_{c2}}{h_{fe(min)}}$: compare i_{b2} with $i_{b2(m}$

If $i_{b2} > i_{b2(min)}$ then only the transistor Q_2 is in ON state.

From circuit,

$$i_2' = \frac{V_D - V_A}{R_1} \Rightarrow V_A = V_D - i_2' R_1 = V_{B1}$$

If $V_A < 0$ i.e $V_{BE(Q_1)}$ is also zero i.e Q_1 is in OFF state.

Stable Voltage (V_c) :-

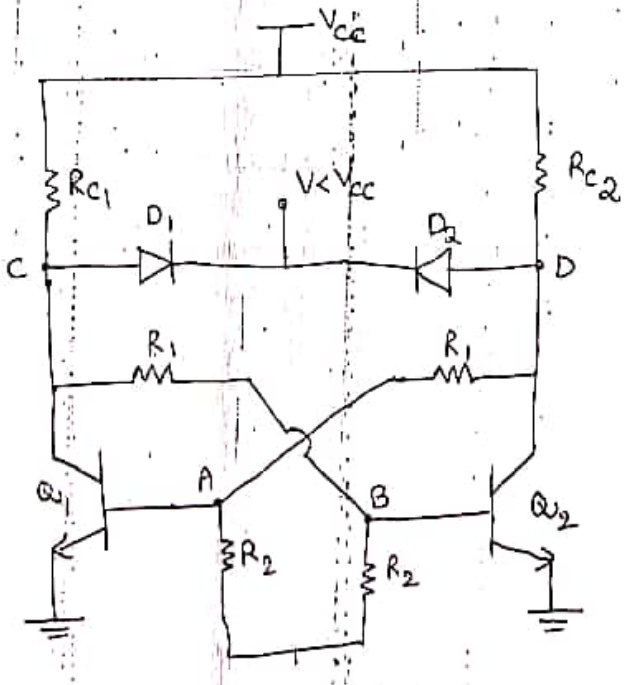
w.k.T $V_c = V_{cc} - I_{c_1} R_{c_1}$

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collector catching diodes :-

The collector voltage of a bistable multivibrator is used to drive other circuits and hence at one (or) both the collectors are shunting loads which reduces the magnitude of the collector voltage V_{c1} of the OFF transistor Q_1. The Input of Q_2 also reduces, it decreases the current I_{b2} and Q_2 driven into saturation.

Practically the circuit must be designed in such a way that under heaviest loading condition, stable state of the multivibrator is ensured. i.e, one transistor is OFF and other is in saturation. This can be obtained by using two diodes as shown in fig. The two diodes are called collector-catching diodes and auxilary supply voltage 'V' used as less than V_{cc} ($V < V_{cc}$)



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when Q_1 is in cut-off region, its collector voltage V_{c1} tries to rise to V_{cc}. when it becomes equal to V which is less than V_{cc}, the diode D_1 conducts, assuming it to be an Ideal diode. This act as short circuit and $V_{c1} = V$. Thus the diode D_1 clamps the collector voltage V_{c1} at V. By selecting proper value of V, it can be ensured that the circuit does not get loaded and I_{b2} is maintained at such a level that the transistor Q_2 is driven into saturation.

Self-bias bistable multivibrator:-

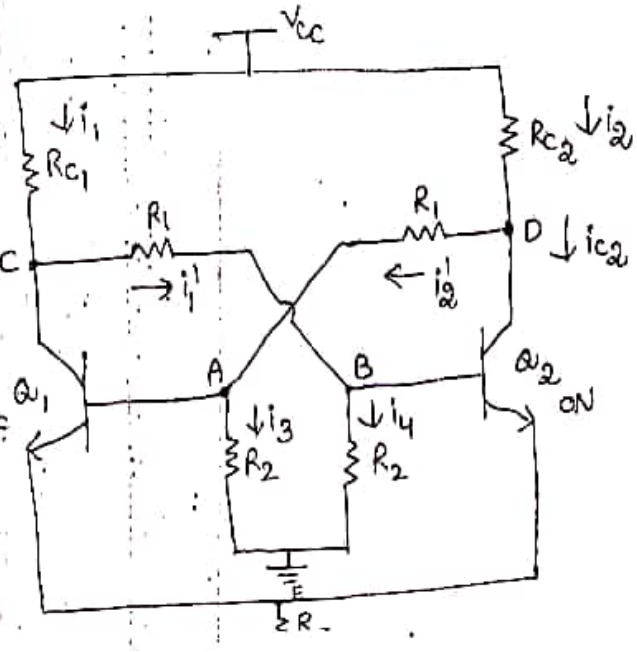
In a fixed bias ~~bina~~ bistable multivibrator requires two power supplies one is V_{cc} and other is $-V_{BB}$.

The need of $-V_{BB}$ is eliminated by using common emitter resistor R_E. This resistor provides self bias so it called as self biased binary.

Assume Q_1 is OFF (cut-off) and Q_2 is ON (saturation)

$$V_D = V_{CE(sat)} + V_E$$

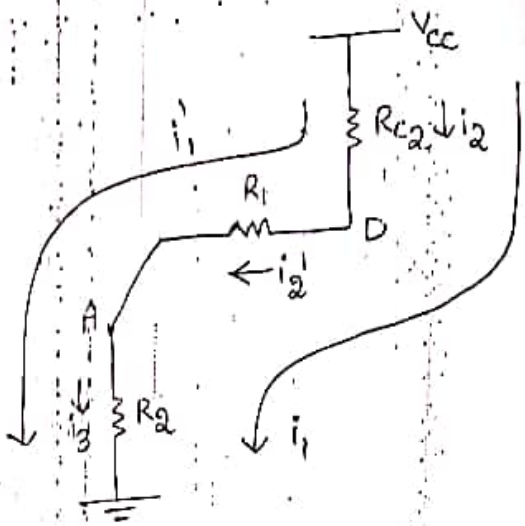
$$V_B = V_{BE(sat)} + V_E$$



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At node 'D':-

$$i_1 = \frac{V_{cc}}{R_1+R_2+R_{c2}}$$



But, current at node 'D' is i_1'

$$i_1' = \frac{V_D}{R_1+R_2}$$

$$V_D = i_1'(R_1+R_2) \quad [\because i_1 = i_1']$$

$$V_D = \frac{V_{cc}(R_1+R_2)}{R_1+R_2+R_{c2}} = V_{TH}(D)$$

Thevenin's voltage and resistance at node 'D' is

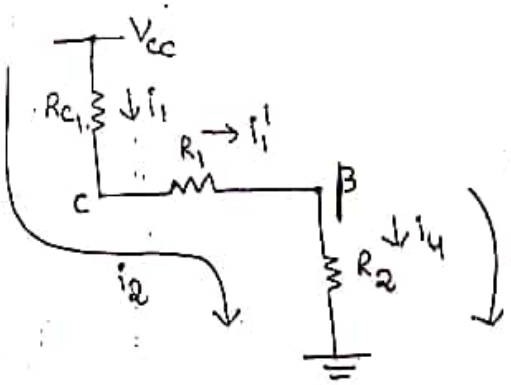
$$V_{TH}(D) = \frac{V_{cc}(R_1+R_2)}{R_1+R_2+R_{c2}}$$

$$R_{TH}(D) = R_{c2} \,||\, (R_1+R_2) = \frac{R_{c2}(R_1+R_2)}{R_1+R_2+R_{c2}}$$

At node 'B':-

$$i_2 = \frac{V_{cc}}{R_1+R_2+R_{c1}}$$

current $i_2' = \frac{V_B}{R_2} \Rightarrow V_B = i_2' R_2$



$$V_B = \frac{V_{cc} R_2}{R_1+R_2+R_{c1}} = V_{TH}(B)$$

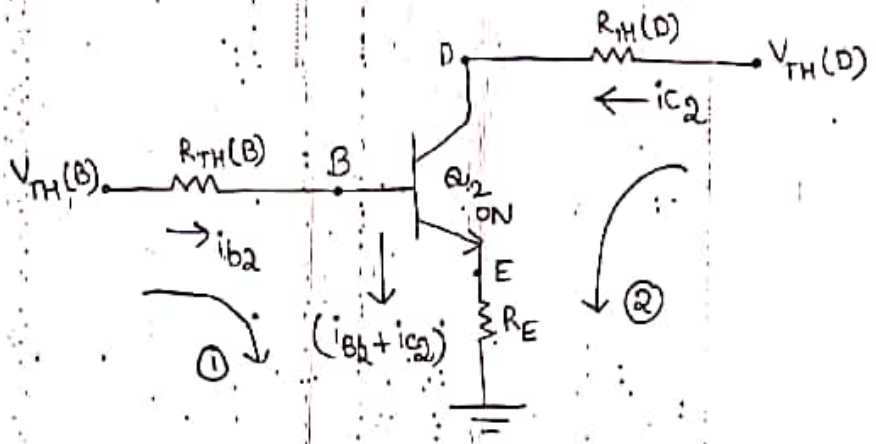
Thevenin's voltage and resistance at node 'B' is

$$V_{TH}(B) = \frac{V_{cc} R_2}{R_1+R_2+R_{c1}}$$

$$R_{TH}(B) = (R_1+R_{c1}) \,||\, R_2 = \frac{(R_1+R_{c1}) R_2}{R_1+R_2+R_{c1}}$$

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The equivalent circuit of transistor Q_2 is



The loop equations are,

$$V_{TH}(B) = i_{b2} R_{TH}(B) + V_{BE}(sat) + R_E (i_{b2} + i_{C2}) \quad \text{—①}$$

$$V_{TH}(D) = i_{C2} R_{TH}(D) + V_{CE}(sat) + R_E (i_{b2} + i_{C2}) \quad \text{—②}$$

Solving eq ① & ② to get i_{b2}, i_{C2} values.

From circuit, $i_{b2} = \dfrac{V_{TH}(B) - V_B}{R_{TH}(B)}$

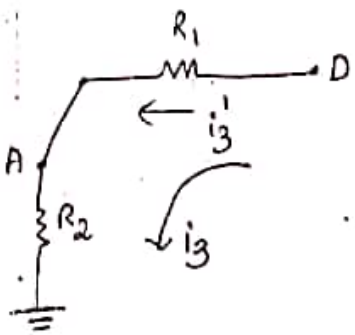
$$V_B = V_{TH}(B) - i_{b2} R_{TH}(B)$$

$$i_{C2} = \frac{V_{TH}(D) - V_D}{R_{TH}(D)}$$

$$V_D = V_{TH}(D) + i_{C2} R_{TH}(D)$$

Find V_A :-

current at node 'D' $\quad i_3 = \dfrac{V_D}{R_1 + R_2}$



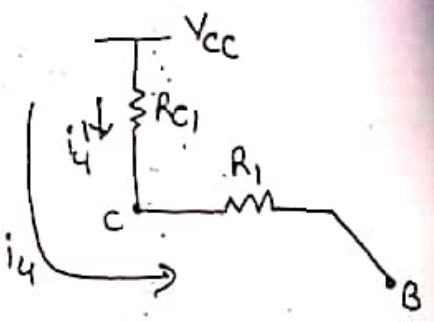
current at node 'A' is i_3',

$$i_3' = V_D - V_A$$

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$$V_A = V_D - i_3 R_1$$

$$V_A = V_D - \frac{V_D R_1}{R_1 + R_2} \qquad (\because i_3 = i_3')$$



At V_C :-

current at node 'B' is

$$i_4 = \frac{V_{CC} - V_B}{R_1 + R_{C_1}}$$

current at node 'c' is $i_4' = \frac{V_{CC} - V_C}{R_{C_1}}$

$$V_C = V_{CC} - i_4 R_{C_1}$$

$$V_{CC} = V_{CC} - \left[\frac{V_{CC} - V_B}{R_1 + R_{C_1}}\right] R_{C_1} \qquad (\because i_4 = i_4')$$

To Find V_E by using

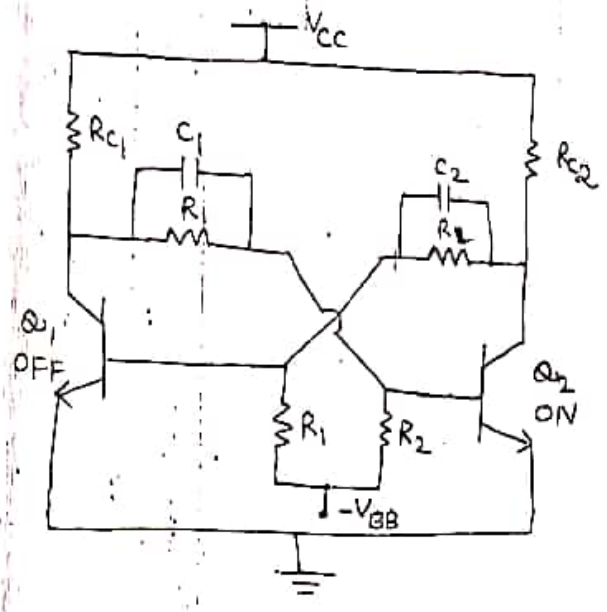
$$V_E = V_D - V_{CE(sat)} \quad (or) \quad V_E = V_B - V_{BE(sat)}$$

commutating capacitors :-

In order to Increase the switching speed of multivibrator the normal practice is to shunt the coupling resistors R_1, R_2 by suitable capacitors C_1, C_2. These capacitors are also termed as speed-up capacitors (or) transpose capacitors.

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Let Q_2 be ON, Q_1 be OFF



In order to change the state of the binary, a negative spike voltage is applied to collector of transistor Q_1. This appears at base of transistor Q_2.

The base of Q_2 goes negative, the potential of its collector terminal Increases. This Increase of voltage at collector of Q_2 must be Quickly transmitted to base of Q_1 so it change its state from OFF to ON. This is achieved by providing suitable capacitor C_2 across R_1.

R_1, R_2, C_1, C_2 together constitute a perfectly compensated attenuator. Full voltage rise at collector terminal of transistor Q_2, and Q_1 would be ON. C_2 must be designed properly it should not be too large (or) too small.

The main feature of the commutating capacitors is that they reduce transition time and Increase the switching speed. Hence the name speed-up capacitors.

The Smallest permissible Interval between 2 succesive triggers is called Resolving time of the flipflop.

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The reciprocal of the resolving time represents the max. frequency at which binary can respond.

$$\therefore f_{max} = \frac{1}{\text{Resolving time}}$$

The following relation ship finds to use in design of speed-up capacitors.

$$C_1 = C_2 = \frac{1}{2.3 f_{max} (R_1 || R_2)}$$

$$\boxed{C_1 = C_2 = \frac{R_1 + R_2}{2.3 f_{max} R_1 R_2}} \qquad \left(\because R_1 || R_2 = \frac{R_1 R_2}{R_1 + R_2}\right)$$

Triggering of Bi stable multivibrator:-

The process of applying an external signal to Induce a transition from one state to another is called triggering. Triggering signal is either a pulse of short duration (or) step voltage.

There are 2 methods of triggering they are

i) un symmetrical triggering (or) Asymmetrical triggering

ii) symmetrical triggering

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1. Unsymmetrical triggering :-

In this triggering, two triggering pulses from two separate sources are needed to change the states of the binary. when an external trigger is applied, the transistor changes its state and continues to be in that state until another trigger is applied to change the state. It also called the set-reset triggering

The unsymmetrical triggering is used in logic circuits (registers, counters, etc.) and used as a generator of gate whose width equals the Intervals between the triggers.

2. symmetrical triggering :-

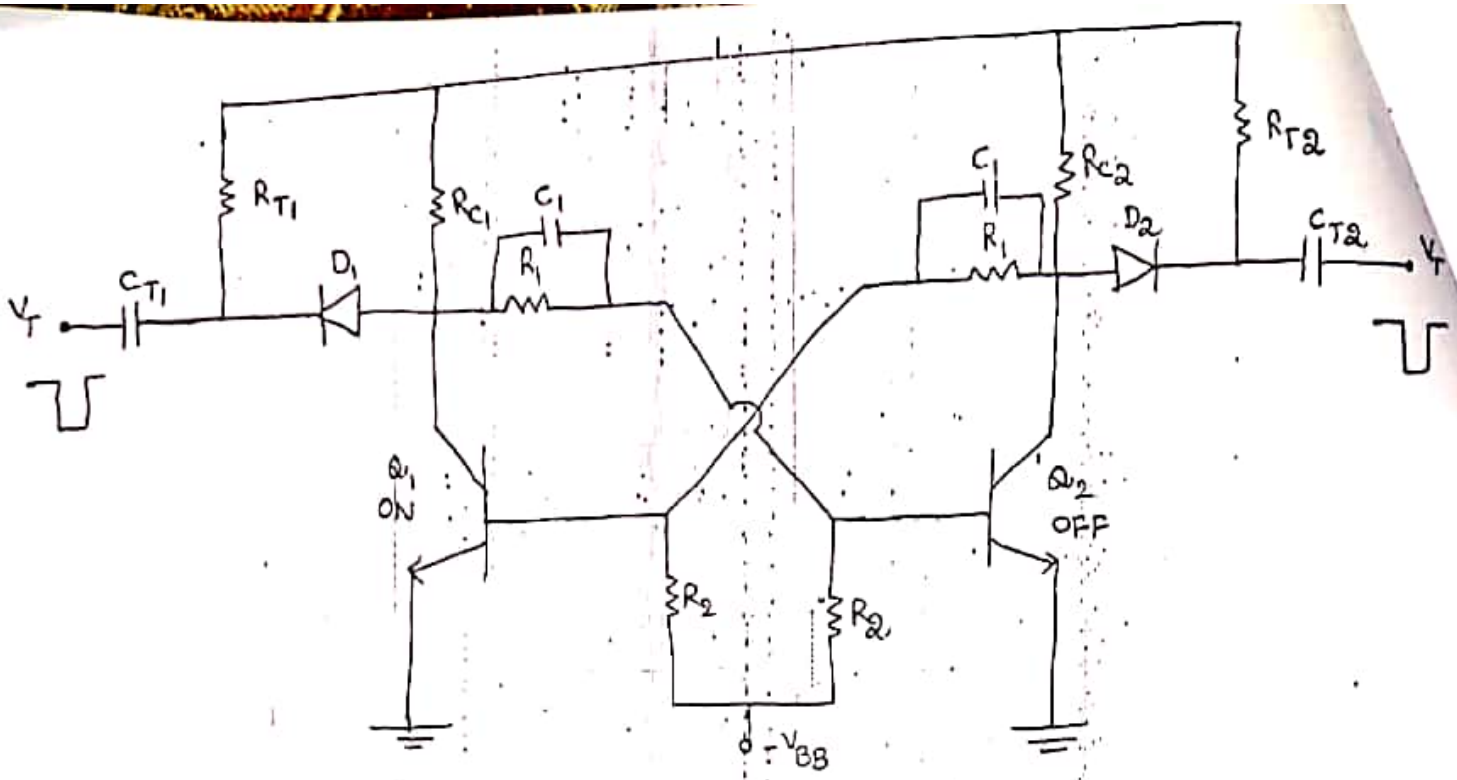
In this type, only one triggering pulse is needed to bring about a change of state, and each time the pulse is applied, there results a transition from ON state to OFF state (or) vice versa.

It is mainly used in counting circuits.

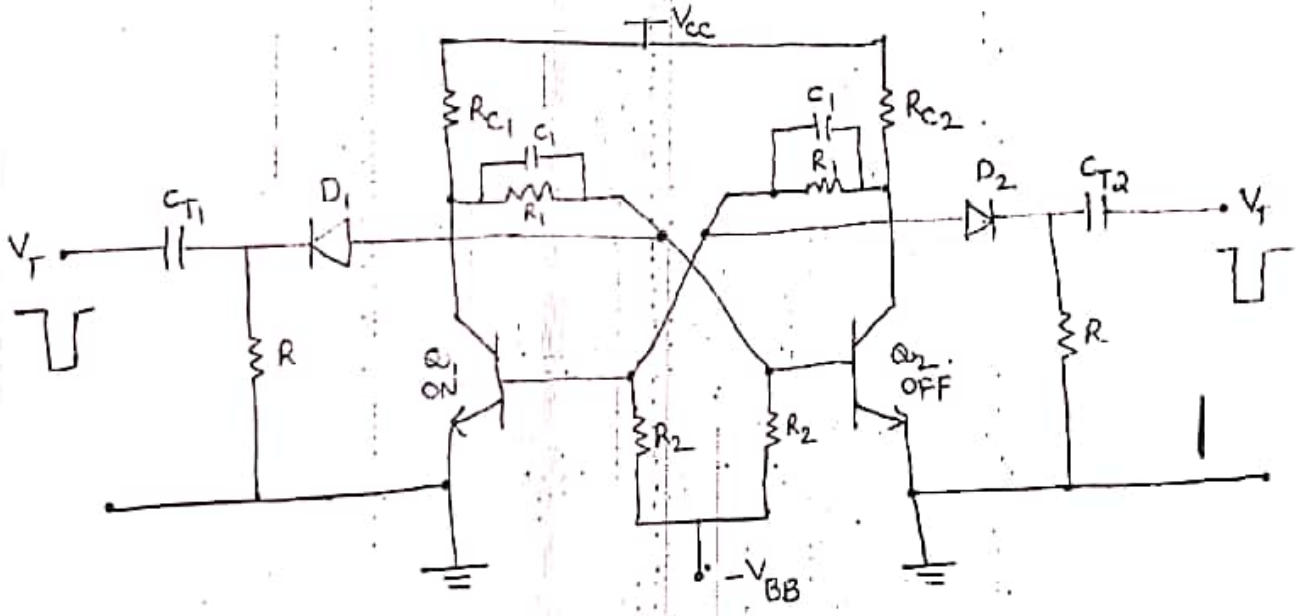
1. unsymmetrical triggering :-

Below fig(a) & (b) shows unsymmetrical triggering circuits when the signals are applied at the collectors and bases respectively.

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a) un symmetrical triggering at collectors



b) un symmetrical triggering at bases

Suppose in one stable state Q_1 is ON, Q_2 is OFF. when Q_1 is ON, diode D_1 at the collector of transistor Q_1 is back biased by the drop across R_{C1} because its anode is at $V_{CE(sat)}$ and cathode is at V_{cc}.

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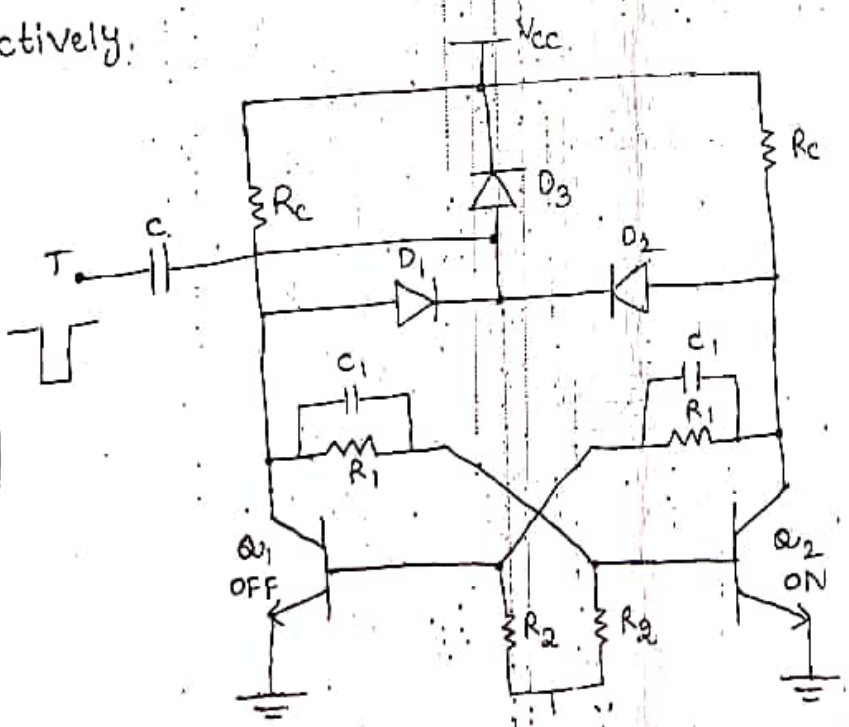
when Q_2 is OFF, both the anode and cathode of the diode at its collector are at V_{cc} and the drop across 'D' is zero. so when Q_1 is ON, Q_2 is OFF only a -ve pulse applied at R can change the state.

on the application of -ve pulse, diode D is forward biased (transistor T_2) which reduces the voltage at collector of Q_2 and in turn the base potential of Q_1 decreases which makes ON transistor to OFF.

The voltage at the collector of Q_1 is at V_{cc} which when applied at base of Q_2 makes its ON.

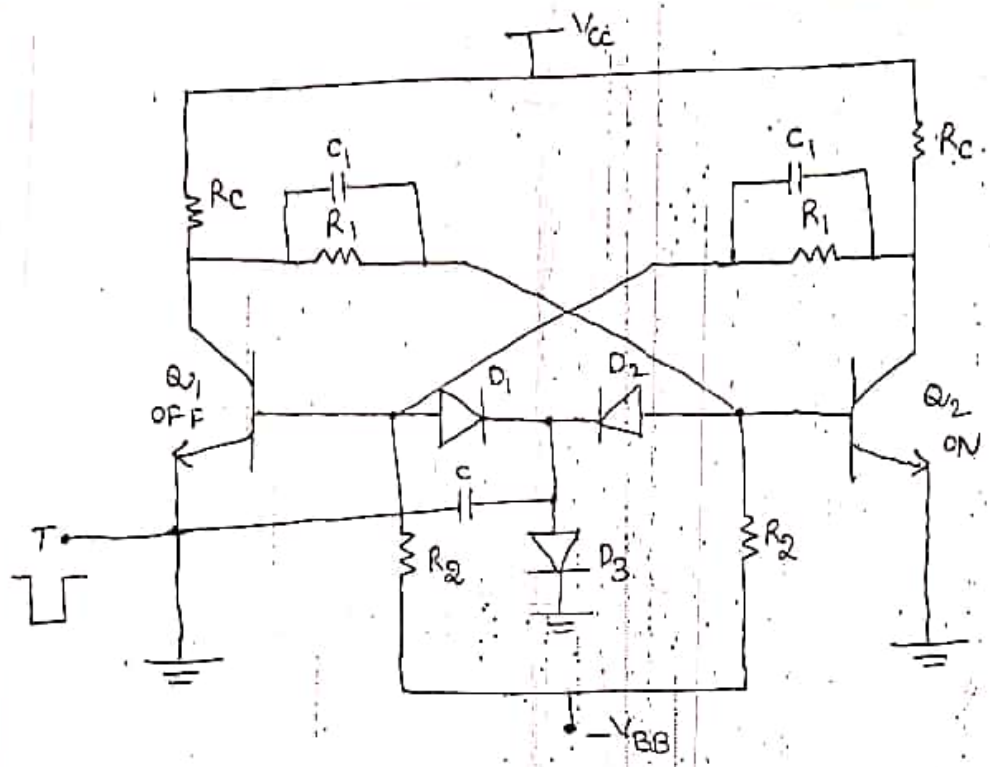
2. Symmetrical triggering

Below fig (a) & (b) shows symmetrical triggering circuits when the signals are applied at the collectors and bases respectively.



a) symmetrical triggering at collectors

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b) symmetrical triggering at bases.

operation

If Q_2 is ON, Q_1 is OFF in one of the stable states. The output at collector of Q_2 is $V_{CE(sat)}$ and output at collector Q_1 is V_{cc}.

Therefore: D_2 is reverse biased by V_{cc}. hence a -ve Input signal will be transmitted through D_1 to the collector of Q_1 and the base of ON transistor Q_2 via the R_1C_1 combination connecting the output of Q_1 to the Input of Q_2. This -ve pulse at base of Q_2 which turns ON to OFF state thus causing a transistion. So D_1 will be reverse biased and D_2 is zero bias.

The next -ve pulse will pass through D_2 Instead of D_1. The binary will transfer at each successive -ve Input

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pulse (or) step but will not respond to the triggers of posite Polarity.

Emitter-coupled bistable multivibrator (schmitt trigger):-

It is also known as regenerative comparator.

The circuit diagram of an emitter-coupled bistable multivibrator using npn transistor is shown in fig.

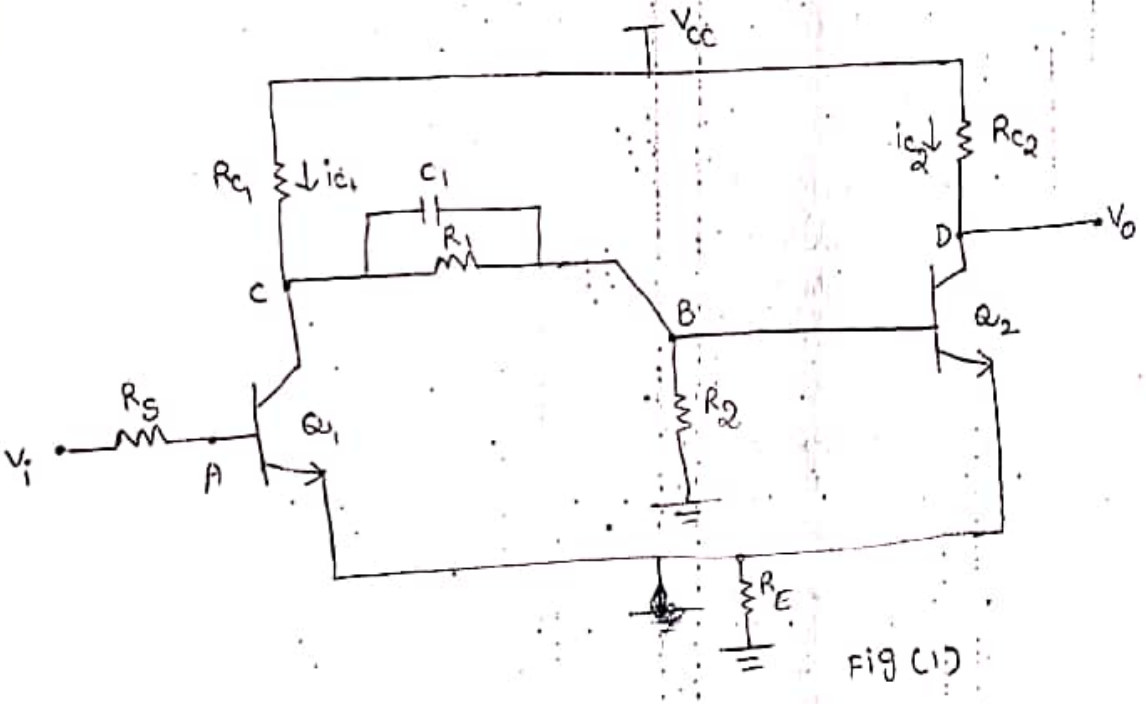


Fig (1)

In this,

i) The coupling from the output of second stage to the Input of 1st stage is removed.

ii) The feed back is obtained through a common emitter resistor R_E.

Before the Input is applied the transistors Q_1 is OFF and Q_2 is ON.

Q_1 is connected to ai voltage source V_i.

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Let the Input to the transistor Q_1 be [illegible]

$$V_i = V_m \sin \omega t$$

when $V_i = 0$, Q_1 is OFF then the output voltage is V_{cc} it is at node 'B' then the transistor Q_2 is ON. So, the output voltage

$$V_0 = V_{cc} - I_{c_2} R_{c_2}$$

when Input is applied, the transistor Q_1 comes out of cut-off region when the Input reaches $V_E + V_{BE}(sat)$.

The transistor Q_1 starts conducting results in amplification of circuit, thus the collector voltage at Q_1 decreas and emitter voltage Increases therefore Q_2 turned OFF.

The output voltage $V_0 = V_{cc}$ as Q_2 is turned OFF.

UTP

UTP → upper trigger point (or) Upper threshold point ~~(or) up~~

It is defined as the voltage $V = V_1$ at which the transistor Q_1 enters into conduction is called UTP.

when $V_i > V_E + V_\gamma$ the Q_1 changes from OFF to ON this is refered as UTP point.

LTP

LTP → Lower triggering point (or) lower threshold point.

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It is defined as the voltage $V = V_2$ at which the transistor Q_2 resumes conduction is called LTP.

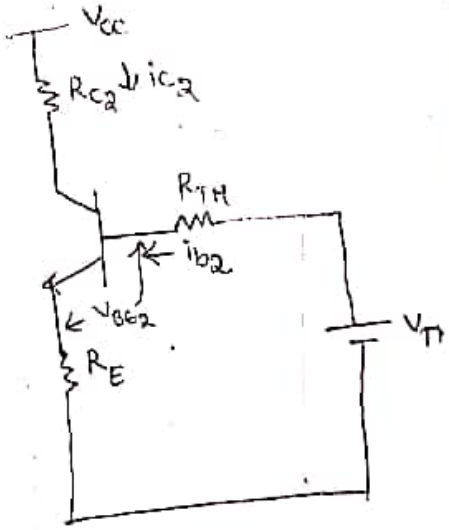
when $V_i < V_E + V_\gamma$ then Q_1 is OFF and automatically Q_2 goes from OFF to ON state.

* At LTP, transistor Q_1 ON and Q_2 OFF
* At UTP, transistor Q_1 OFF and Q_2 ON

calculation of UTP :- when Q_1 OFF; Q_2 ON

From fig (i), $V_{TH} = \dfrac{V_{CC} R_2}{R_1 + R_2 + R_{C_1}}$

$$R_{TH} = \frac{(R_1 + R_{C_1}) R_2}{R_1 + R_2 + R_{C_1}}$$



APPLY KVL

$$V_{TH} = i_{b_2} R_{TH} + V_{BE_2} + (i_{b_2} + i_{c_2}) R_E \quad \text{---(1)}$$

we know that

$$h_{fe} = \frac{i_{c_2}}{i_{b_2}} \Rightarrow i_{c_2} = h_{fe} i_{b_2} \quad \text{---(2)}$$

substitute eq (2) in eq (1)

$$V_{TH} = i_{b_2} R_{TH} + V_{BE_2} + (i_{b_2} + h_{fe} i_{b_2}) R_E$$

$$V_{TH} = V_{BE_2} + i_{b_2} (R_{TH}) + i_{b_2} (1 + h_{fe}) R_E$$

$$= V_{BE_2} + \left[(1 + h_{fe}) R_E + R_{TH}\right] i_{b_2}$$

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$$\Rightarrow i_{b2}' = \frac{V_{TH} - V_{BE2}}{R_{TH} + (1+h_{fe}) R_E} \quad \text{---} (3)$$

But $V_{UTP} = V_{E2} + V_2$

$= (i_{b2} + i_{c2}) \cdot R_E + V_2$

$= (i_{b2} + h_{fe} i_{b2}) R_E + V_2 \quad \left[\because h_{fe} = \frac{i_{c2}}{i_{b2}}\right]$

$= i_{b2} [1+h_{fe}] R_E + V_2 \quad \text{---} (4)$

Substitute eq (4) in eq (3)

$$V_{UTP} = \frac{V_{TH} - V_{BE2}}{R_{TH} + (1+h_{fe}) R_E} (1+h_{fe}) R_E + V_2$$

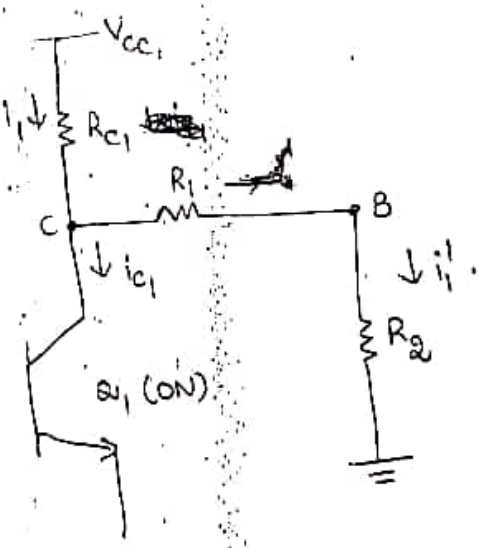
Calculation of LTP :-

Apply KCL at node c,

$i_1 = i_{c_1} + i_1'$

$i_{c_1} = i_1 - i_1'$

$$i_{c_1} = \frac{V_{cc} - V_c}{R_{c_1}} - \frac{V_B}{R_2}$$



But $i_1' = \frac{V_c}{R_1 + R_2} \Rightarrow V_c = i_1' (R_1 + R_2)$

$$V_c = \frac{V_B}{R_2} (R_1 + R_2) = m V_B$$

where, $m = \frac{R_1 + R_2}{R_2}$

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$$i_{c_1} = \frac{V_{cc} - mV_B}{R_{c_1}} - \frac{V_B}{R_2}$$

$$V_{LTP} = i_{c_1} R_E + V_\gamma$$

$$= \left[\frac{V_{cc} - mV_B}{R_{c_1}} - \frac{V_B}{R_2} \right] R_E + V_\gamma$$

substitute $V_B = V_{LTP}$

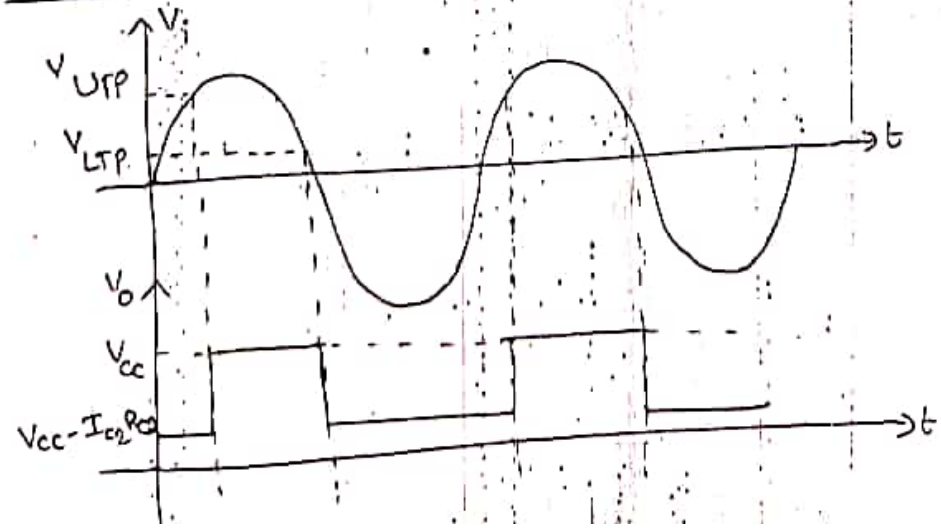
$$V_{LTP} = \left[\frac{V_{cc} - mV_{LTP}}{R_{c_1}} - \frac{V_{LTP}}{R_2} \right] R_E + V_\gamma$$

$$= \frac{V_{cc} R_E}{R_{c_1}} - \frac{mV_{LTP} R_E}{R_{c_1}} - \frac{V_{LTP}}{R_2} R_E + V_\gamma$$

$$V_{LTP} \left[1 + \frac{mR_E}{R_{c_1}} + \frac{R_E}{R_2} \right] = V_\gamma + \frac{V_{cc} R_E}{R_{c_1}}$$

$$\therefore V_{LTP} = \frac{V_\gamma + \frac{V_{cc} R_E}{R_{c_1}}}{1 + \frac{mR_E}{R_{c_1}} + \frac{R_E}{R_2}}$$

Input and output characteristics :-



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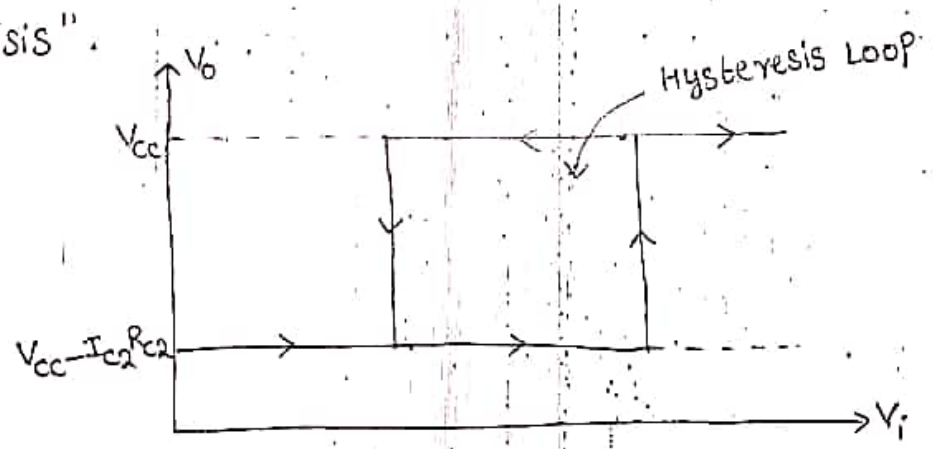
Schmitt trigger also known as [illegible] (or) Squaring circuit.

Applications

1. It act as a voltage comparator
2. It converts sinusoidal wave into a square wave i.e It also act as a square wave generator.
3. Flip-flops

Transfer characteristics of Schmitt trigger :- (or) Hysteresis :-

The graph of output voltage against Input voltage is called transfer characteristics. These characteristics also called "Hysteresis".



when the output changes its state from Low to high at UTP, it remains there until Input crosses LTP and Vice Versa.

→ It is also called "Dead band" (or) "Dead zone".

→ The loop characteristics is called "Hysteresis Loop".

→ The difference between UTP and LTP is called the width of hysteresis.

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ω = width of hysteresis = UTP − LTP

The characteristics of hysteresis can be changed by the values of R_{C_1}, R_{C_2}.

Elimination of hysteresis :-

When the schmitt trigger is used as a comparator, the hysteresis should be eliminated. There are 2 methods to eliminate hysteresis. They are

1. By selecting proper values of R_1 and R_2, UTP and LTP values can be made closer.
2. By Introducing a resistance R_{C_1} in series with emitter of Q_1
   (or) By Introducing a resistance R_{E2} in series with emitter of Q_2.

The circuits shown in fig (a) & (b)

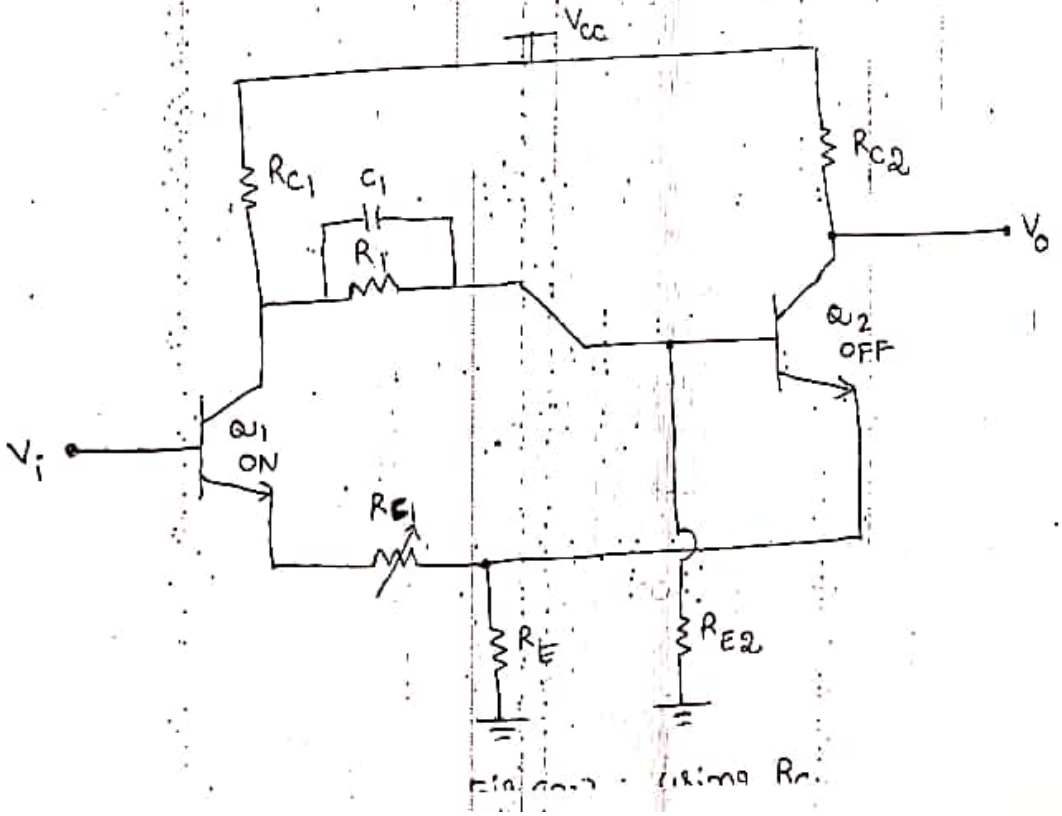


Fig (a) using R_E

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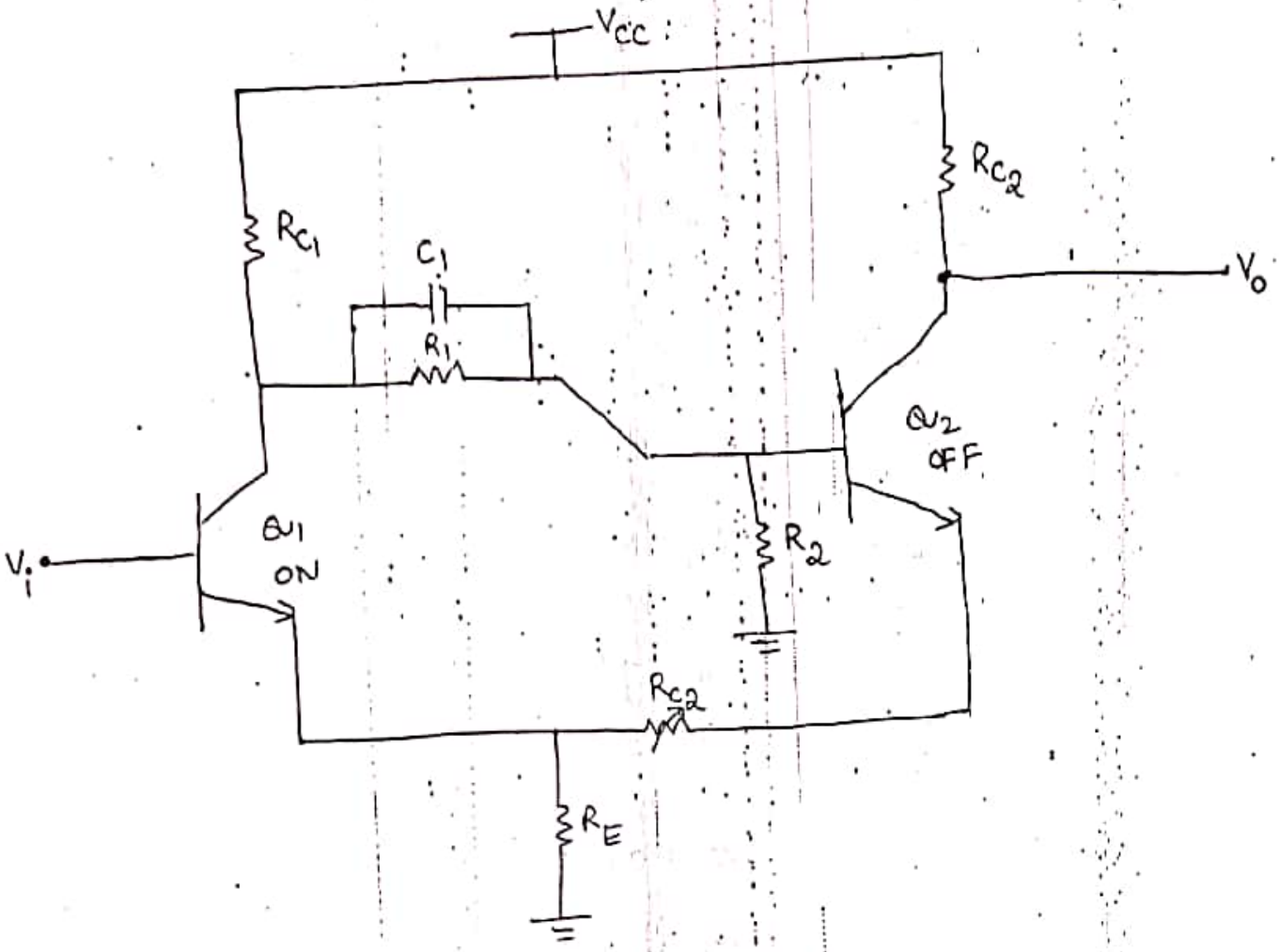


Fig (b) :- using R_{C_2}

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