Code No: R19ES1213 **R19** SET - 1

I B. Tech II Semester Regular Examinations, December - 2020
DIGITAL LOGIC DESIGN
(Com. to CSE, IT)

Time: 3 hours Max. Marks: 75

Answer any five Questions one Question from Each Unit
All Questions Carry Equal Marks

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1.	a)	What is binary number system? And convert $(101101110001.00101)_2=(\ )_8$.	(8M)
	b)	Write the rules for subtraction using 1`s complement and 2`s complement.	(7M)
		Or	
2.	a)	What is a Reflected Code? Write about reflected codes by giving examples.	(7M)
	b)	Convert the following numbers to Binary and Decimal: (i) $(25.325)_8$ (ii) $(BA.125)_{16}$.	(8M)
3.	a)	List out the postulates and write the properties used in Boolean Algebra.	(8M)
	b)	Prove that wx+ y′(w′+z′)= wx+xz+x′z′+wy′z′ if w′x+yz′=0	(7M)
		Or	
4.	a)	Simplify the following with K-map $F(A,B,C,D)=\sum(0,1,4,5,7,8,10,13)+\phi\sum(2,6)$.	(8M)
	b)	Prove that NAND and NOR operations are commutative but not associative.	(7M)
5.	a)	What do you mean by half-adder and full-adder? How will you implement full-adder using half-adder? Explain with circuit diagram.	(8M)
	b)	Design a combinational circuit for a 2-bit magnitude comparator.	(7M)
		Or	
6.	a)	What is mean by Demultiplexer? Discuss briefly about it.	(8M)
	b)	Implement the following Boolean function using decoder and OR-gates F1 $(A,B,C,D)=\sum(2,4,7,9)$. F2 $(A,B,C,D)=\sum(10,13,14,15)$.	(7M)
7.	a)	Draw the circuit of a D-latch and explain its working with the help of its truth table.	(8M)
	b)	Convert JK flip-flop to T flip-flop.	(7M)
		Or	
8.	a)	Write the conversion procedure of flip-flops. Convert D-flip flop to T-flip flop.	(8M)
	b)	Explain the SR flip-flop with the help of a neat logic diagram and excitation table.	(7M)
9.	a)	Draw the circuit and explain the function of 4-bit bidirectional shift register with flip-flops.	(8M)
	b)	With suitable waveforms explain the problems faced by ripple counter.	(7M)
		Or	
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10. a) Explain synchronous and ripple counter and compare their merits and demerits. (8M)

    b) Draw the 4-bit Johnson counter and explain the operation with relevant output waveforms. (7M)

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Code No: R19ES1213 **R19** SET - 2

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Time: 3 hours Max. Marks: 75

Answer any five Questions one Question from Each Unit
All Questions Carry Equal Marks

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1.	a)	Represent the decimal number 599 in (i) Binary Code (ii) 2421 Code (iii) 54-2-1 Code (iv) BCD Code.	(8M)
	b)	Convert the following $(292)_{10}=(\ )_2$ and $(17.125)_{16}=(\ )_2$.	(7M)
		Or	
2.	a)	Perform the following addition using excess-3 code (i) 386+756. (ii) 1010+444.	(8M)
	b)	The binary number listed have a sign bit in the left most position and if negative are in 1`s complement form. Perform the arithmetic operations indicated and verify the answers. (i) 101011+111000 (ii) 001110+110010.	(7M)
3.	a)	Explain about basic theorems and properties of Boolean Algebra.	(8M)
	b)	Reduce the following Boolean expressions to minimum number of literals. (i) ((AB)′+A′+AB)′ (ii) AB+(AC)′+AB′+C(AB+C) (iii) ((AB′+ABC)′+A(B+AB′))′	(7M)
		Or	
4.	a)	Minimize the given function $F=\sum(1,2,3,5,7,9,11,13)$ use K-map method.	(8M)
	b)	Draw NOR logic diagram that implements the following function. $F(A,B,C,D)=\pi(0,1,2,3,4,8,9,12)$.	(7M)
5.	a)	Design half-adder using only NAND gates.	(8M)
	b)	Design a combinational circuit for an octal to binary encoder.	(7M)
		Or	
6.	a)	What is decoder? Construct a 4X16 decoder with two 3X8 decoders.	(8M)
	b)	Implement a Boolean function. $F(x,y,z)=\sum(2,4,6)$ with a multiplexer.	(7M)
7.	a)	What is SR-latch? Explain its operations.	(8M)
	b)	Draw the logic diagram of D-flip flop and explain.	(7M)
		Or	
8.	a)	Convert SR flip-flop to T flip-flop.	(8M)
	b)	Write the conversion procedure of flip-flops. Convert T-flip flop to JK-flip flop.	(7M)

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9. a) What is the difference between serial and parallel transfer? Explain how to convert serial data to parallel data and parallel to serial. What type of register is needed? (8M)

   b) Draw and explain 3-bit up/down asynchronous counter. (7M)

Or

10. a) Explain with the help of a neat diagram the operation of 4-bit universal shift register. (8M)

    b) What is Johnson counter? Explain its advantages and disadvantages. (7M)

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Code No: R19ES1213 **R19** SET - 3

I B. Tech II Semester Regular Examinations, December - 2020
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Time: 3 hours Max. Marks: 75

Answer any five Questions one Question from Each Unit
All Questions Carry Equal Marks

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1.	a)	Convert the following numbers to binary and decimal: (i) $(129.25)_8$ (ii) $(9F.15)_{16}$.	(8M)
	b)	Explain the classification of binary codes.	(7M)
		Or	
2.	a)	Subtract the following numbers using 2`s and 1`s complement. (i) 753-864 (ii) 20-100.	(8M)
	b)	What is an excess-3 BCD code? Which short coming of the 8421 BCD code is overcome in the excess-3 BCD code? Illustrate with the help of example?	(7M)
3.	a)	What are the properties and postulates of Boolean Algebra?	(8M)
	b)	Express the following functions in sum of min terms and product of max terms. (i) F(x,y,z)=(xy+z)(y+xz) (ii) F(x,y,z)=1.	(7M)
		Or	
4.	a)	Minimize the expression Y=AB′C+A′B′C+A′BC+AB′C′+A′B′C′.	(8M)
	b)	Realize the circuit using only NAND gates. F(A,B,C,D)=∑(0,1,4,5,7,8,10,13)+ϕ∑(2,6).	(7M)
5.	a)	Design full-adder using only NAND gates.	(8M)
	b)	Design a priority encoder of 4-bit.	(7M)
		Or	
6.	a)	Implement the following functions using PLA: $A=XY+XZ^1$; $B=XY^1+YZ+XZ^1$.	(8M)
	b)	Realize the following Boolean function using decoder and logic OR gate F1=∑(1,5,7,8,9), F2=∑(2,3,12,13,14,15).	(7M)
7.	a)	Explain the JK flip-flop with a neat logic diagram and truth table in flip-flops.	(8M)
	b)	What do you mean by triggering? Explain the various triggering modes with examples.	(7M)
		Or	
8.	a)	Explain the conversion of D-flip flop to T-flip flop.	(8M)
	b)	Explain the terms Preset and Clear in connection with a flip-flop.	(7M)
9.	a)	Differentiate Synchronous and Asynchronous counters.	(8M)
	b)	Draw and explain the 4-bit shift register with T flip-flops.	(7M)
		Or	
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10. a) What do you mean by Ripple Counter? Explain the basic principles of ripple counter. (8M)

    b) Draw the circuit diagram of 4-bit ring counter using d-flip flop and explain its operation. (7M)

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Code No: R19ES1213 **R19** SET - 4

I B. Tech II Semester Regular Examinations, December - 2020
DIGITAL LOGIC DESIGN
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Time: 3 hours Max. Marks: 75

Answer any five Questions one Question from Each Unit
All Questions Carry Equal Marks

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1.	a)	Perform arithmetic operation indicated below. Follow signed bit notation. (i) 001110+110010 (ii) 101011 – 100110.	(8M)
	b)	Explain BCD and Excess-3 code with an example.	(7M)
		Or	
2.	a)	Subtract the following numbers using 2`s and 1`s complement. (i) 5250 – 321 (ii) 3750 – 2100.	(8M)
	b)	The binary number listed have a sign bit in the left most position and if negative, are in 1`s complement form. Perform the arithmetic operations indicated and verify the answers. (i) 111001 – 001010 (ii) 101011 – 100110.	(7M)
3.	a)	Design a circuit with four inputs and one output where the output is 1 if input is divisible by 3 or 7?	(8M)
	b)	Reduce the following Boolean expression. (i) AB+A(B+C)+B′(B+D) (ii) A+B+A′B′C (iii) A′B′+A′BC′+A′BCD+A′BC′D′E.	(7M)
		Or	
4.	a)	Obtain minimal POS expression for the Boolean function using K-Map method. F(A,B,C,D)=Π(0,1,2,3,4,6,9,10)+d(7,11,13,15).	(8M)
	b)	Reduce the following Boolean function to four literals and draw the logic diagram: $(A^1+C)\ (A^1+C^1)\ (A+B+C^1D)$.	(7M)
5.	a)	What is Combinational Logic? Explain the analysis procedure for combinational circuits.	(8M)
	b)	Implement the following function with a multiplexer. F(A,B,C,D)=∑(0,1,3,4,8,9,15)	(7M)
		Or	
6.	a)	What is Encoder? Discuss Decimal to BCD Encoder	(8M)
	b)	Implement the following Boolean functions using PLA: (i) $F_1 = \Sigma(0,1,2,4)$; (ii) $F_2 = \Sigma(0,5,6,7)$;.	(7M)
7.	a)	Differentiate combinational and sequential logic circuits.	(8M)
	b)	Convert SR flip-flop to T flip-flop.	(7M)
		Or	
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8. a) Explain the T-flip-flop with a logic diagram and truth table. (8M)

   b) Convert a D-flip flop to JK-flip flop. (7M)

9. a) What is a Shift Register? Explain about following modes of operation. (8M)
   (i) Shift Right Method (ii) Shift Left Method.

   b) Design a mod-10 counter with SR flip-flops. (7M)

Or

10. a) With a logic diagram, explain the working of a 4-bit register which uses parallel load. (8M)

    b) Design a 3-bit ring counter with JK flip-flops. (7M)

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