

III B. Tech II Semester Regular/Supplementary Examinations, October/November - 2020**VLSI DESIGN**

(Common to Electronics and Communication Engineering, Electronics and Computer Engineering)

Time: 3 hours

Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)2. Answer **ALL** the question in **Part-A**3. Answer any **FOUR** Questions from **Part-B**

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**PART -A****(14 Marks)**

1. a) Describe the ION-IMPLANTATION steps in IC fabrication. [2M]
- b) Write a short note on MOS layers and symbolic diagram translation to MASK form. [2M]
- c) What are the sources of wiring capacitances? [2M]
- d) Define the Controllability. [3M]
- e) Define synthesis and explain its importance. [3M]
- f) What is a deep submicron digital IC design? [2M]

**PART -B****(56 Marks)**

2. a) Derive the relationship between drain to source current  $I_{ds}$  versus drain to source voltage  $V_{ds}$  in a non-saturated and a saturated region. [7M]
- b) What are the steps involved in the NMOS fabrication? Explain with neat sketches. [7M]
3. a) What is a stick diagram? Draw the stick diagram and layout for a CMOS inverter. [8M]
- b) Explain about double poly CMOS rules. [6M]
4. a) What is meant by sheet resistance( $R_s$ )? Explain the concept of  $R_s$  applied to MOS transistors. [7M]
- b) Calculate the resistance of an inverter from VDD to GND. If n-channel sheet resistance  $R_{sn}=104 \Omega$  per square and P-channel sheet resistance  $R_{sp} = 3.5 \times 104 \Omega$  per square. ( $Z_{pu}=4:4$  and  $Z_{pd}=2:2$ ). [7M]
5. a) Draw the circuit diagram of the Built-In Self Test(BIST) circuit and explain its operation. [7M]
- b) List out the different fault types that occurred in VLSI circuits and explain each fault in detail. [7M]
6. a) Draw and explain the FPGA design flow. [7M]
- b) Explain the step-by-step approach of the FPGA design process in the Xilinx environment. [7M]
7. a) Explain the concept of Low-power design through voltage scaling in detail. [7M]
- b) Write short notes on the following terms: [7M]
  - i) Interconnect Design, and ii) Power Grid.

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