

III B. Tech II Semester Regular/Supplementary Examinations, October/November - 2020**VLSI DESIGN**

(Electrical and Electronics Engineering)

Time: 3 hours

Max. Marks: 70

- Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
 2. Answer **ALL** the question in **Part-A**
 3. Answer any **FOUR** Questions from **Part-B**
- ~~~~~

PART -A**(14 Marks)**

1. a) What are the steps involved in IC fabrication? [2M]
- b) What are scalable design rules and list their disadvantages? [2M]
- c) List out the limitations of scaling. [2M]
- d) Define Observability. [3M]
- e) What is the need for an FPGA? Write its applications. [3M]
- f) What are the techniques to reduce power consumption? [2M]

PART -B**(56 Marks)**

2. a) Derive the expression for the ratio between $Z_{p,u}$ and $Z_{p,d}$ if an NMOS inverter is to be driven from another NMOS inverter. [7M]
- b) Derive the expressions for MOS transistor parameters g_m , g_{ds} , and ω_0 . [7M]
3. a) What is a Stick diagram? Design a stick diagram for inverter using CMOS and explain its operation. [7M]
- b) Write a short note on $2\mu\text{m}$ Double Metal, Double Poly, CMOS/Bi-CMOS rules. [7M]
4. a) Explain the following terms in detail: i) Switch logic ii) Gate logic. [7M]
- b) What are alternate gate circuits are available? Explain any one of them with a suitable sketch. [7M]
5. a) List out different types of Scan Based Techniques used in VLSI Design and explain them. [7M]
- b) Explain the concept of the On-Chip clock generation in detail. [7M]
6. a) Discuss different types of programming technologies used in an FPGA design. [7M]
- b) Write about the shift register design and implementation onto FPGA. [7M]
7. a) Explain the concept of reduction of switching capacitance along with one example. [7M]
- b) Write short notes on Interconnect Design in detail. [7M]
