Code No: R1621053 **R16** SET - 1

II B. Tech I Semester Supplementary Examinations, October/November - 2020
DIGITAL LOGIC DESIGN
(Com to CSE & IT)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1.	a)	$(22B)_x = (555)_{10}$ then Find the value of 'x'	(2M)
	b)	Simplify the following Boolean functions (i) $X(X^1+Y)$ (ii) $XY+YZ+X^1Z$	(3M)
	c)	Write the Max terms corresponding to the logical expression $Y = (A+B+C^1).(A+B^1+C^1).(A^1+B^1+C)$	(2M)
	d)	Implement XOR gate by using NAND gates.	(2M)
	e)	Write the excitation table for T Flip-flop.	(3M)
	f)	Define synchronous counter.	(2M)

PART -B

2.	a)	How do you convert a gray number to binary? Generate a 4-bit gray code directly using the mirror image property?	(8M)
	b)	Write the comparison between 1's complement and 2's complement.	(6M)
3.	a)	Simplify the following (i)$AB+BC+A^1C = AB+A^1C$ (ii) $(X+Y).(Y^1+Z) = X$	(7M)
	b)	Convert the following expression into SOP and POS (i) $(AB+C)(B+\bar{C}D)$ (ii)$\bar{x}+(x+\bar{y})(y+\bar{z})$	(7M)
4.	a)	Simplify the following function using K-Map $f(a,b,c,d)= \sum m(3,7,11,12,13,14,15)$	
	b)	Design an odd parity circuit using XOR gate.	
5.	a)	Draw and explain the 8×1 MUX.	(7M)
	b)	Convert the BCD to XS-3 and XS-3 to BCD by using a full adder.	(7M)
6.	a)	What is Race condition and explain about the operation of clocked RS flip-flop.	(7M)
	b)	Convert the JK Flip-flop into RS flip-flop.	(7M)
7.	a)	Design a 4-bit ring counter with as in table figure.	(7M)
	b)	Design a 4 bit shift left register using flip flops.	(7M)

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