17/08/19

UNIT-6

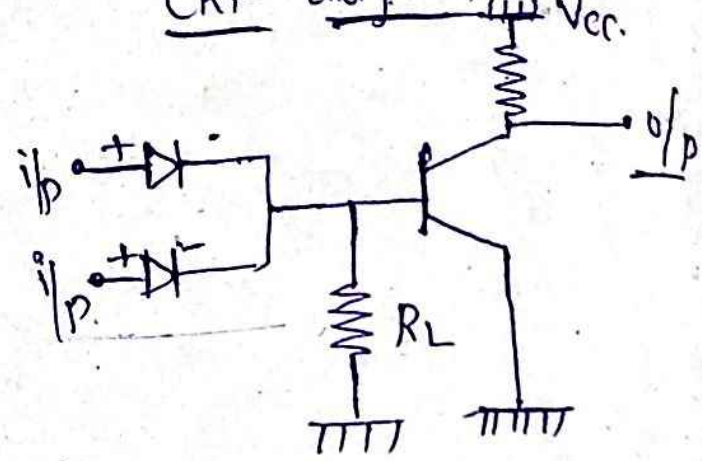
Realization of NOR Gate using DTL :-

(i) +ve logic :-

Truth Table :-

A	B	A+B	$\overline{A+B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Ckt diagram



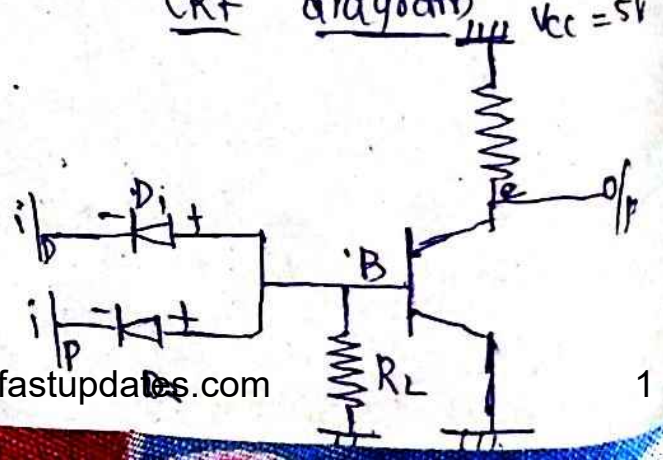
Truth Table :-

A	B	D_1	D_2	T	o/p
L	L	off	off	off	High
L	H	off	ON	ON	low
H	L	ON	off	ON	low
H	H	ON	ON	ON	low

(ii) -ve logic :-

A	B	A+B	$\overline{A+B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Ckt diagram

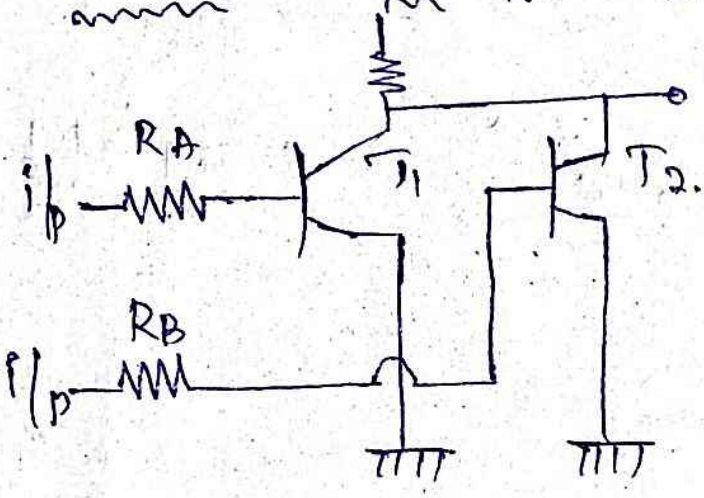


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Truth Table.

A	B	D_1	D_2	T	o/p
L	L	ON	ON	ON	High
L	H	ON	OFF	ON	low.
H	L	OFF	ON	ON	low.
H	H	off	off	off	low.

* Realization of NOR Gate using RTL :-



A	B	T_1	T_2	o/p
L	L	off	off	high.
L	H	off	ON	low
H	L	ON	off	low
H	H	ON	ON	low.

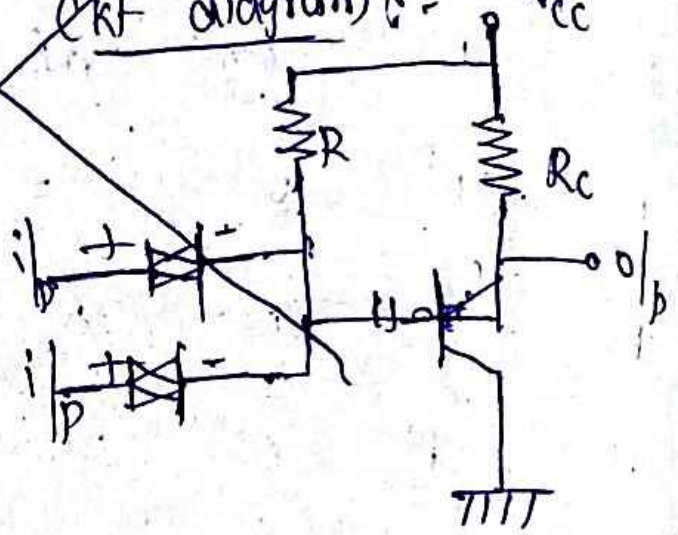
* Realization of And Gate using DTL :-

+ve logic :-

Truth Table

A	B	AB	$\overline{AB}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Ckt diagram :-

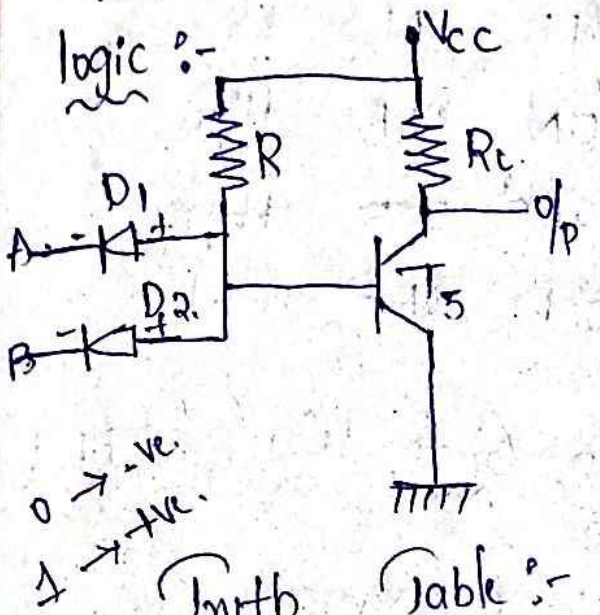


A B D_1 D_2 T o/

Realization of And Gate using DL :-

20/08/19.

* Realization of NAND Gate using DTL (+ve logic) :-



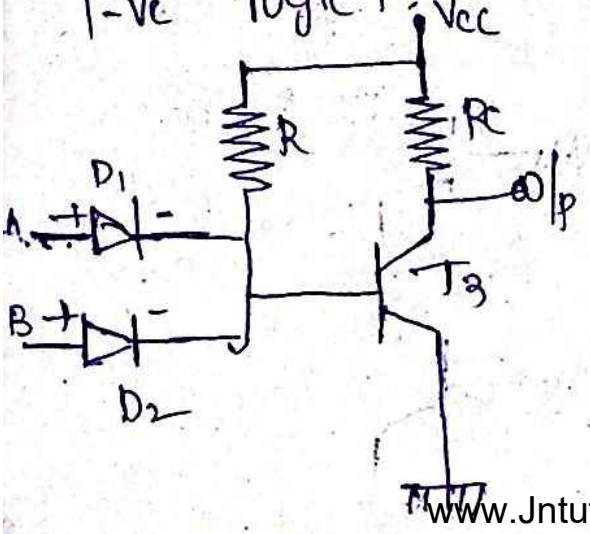
Truth Table :-

A	B	A.B	$\overline{A.B}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Truth Table :-

A	B	D_1	D_2	T_3	o/p.
L	L	ON	ON	OFF	High.
L	H	ON	OFF	OFF	High.
H	L	OFF	ON	OFF	High
H	H	OFF	OFF	ON	Low.

* Realization of NAND Gate using DTL



Truth Table :-

A	B	A.B	$\overline{A.B}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Truth Table :-

A	B	D_1	D_2	T_3	o/p
L	L	OFF	OFF	ON	High.
L	H	OFF	ON	OFF	High
H	L	ON	OFF	OFF	High
H	H	ON	ON	OFF	low.

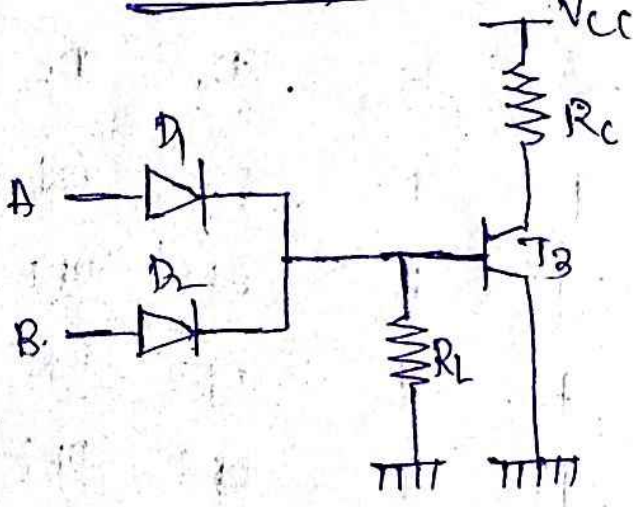
* Realization of NOR Gate using DTL :-

+Ve logic :-

Truth Table :-

A	B	A+B	$\overline{A+B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

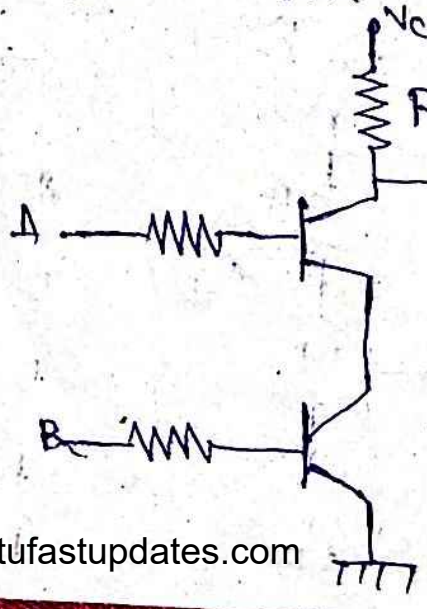
ckt diagram :-



* Realization of Nand Gate using RTL logic :-

General Truth Table :-

A	B	A.B	$\overline{A.B}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0



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Logic Truth Table :-

A	B	T_1	T_2	o/p
L	L	OFF	OFF	High
L	H	OFF	ON	High
H	L	ON	OFF	High
H	H	ON	ON	low.

* Applications Of logic Gates :-

(i) The logic Are Used in Digital Systems such as Computer, Digital Communication System, and Stimulation System.

(ii) logic Gates Embedded VLSI (very large Scale integration CKTS

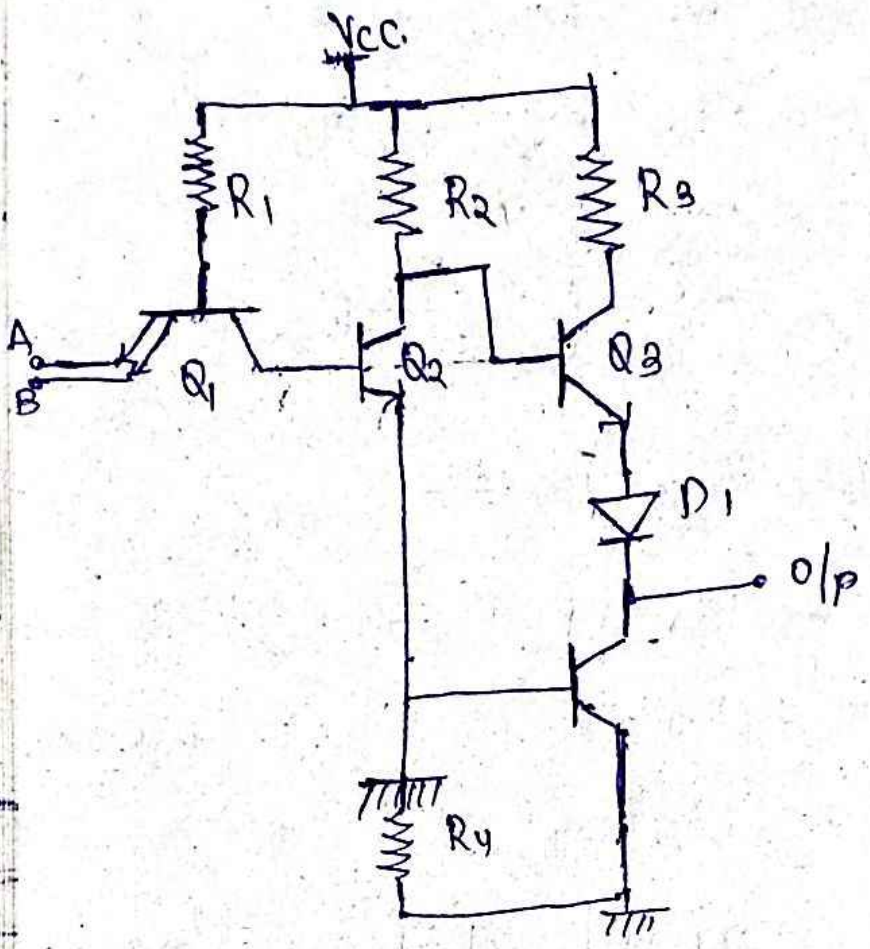
(iii) logic Gates are used for implementing Boolean Algebraic Expressions.

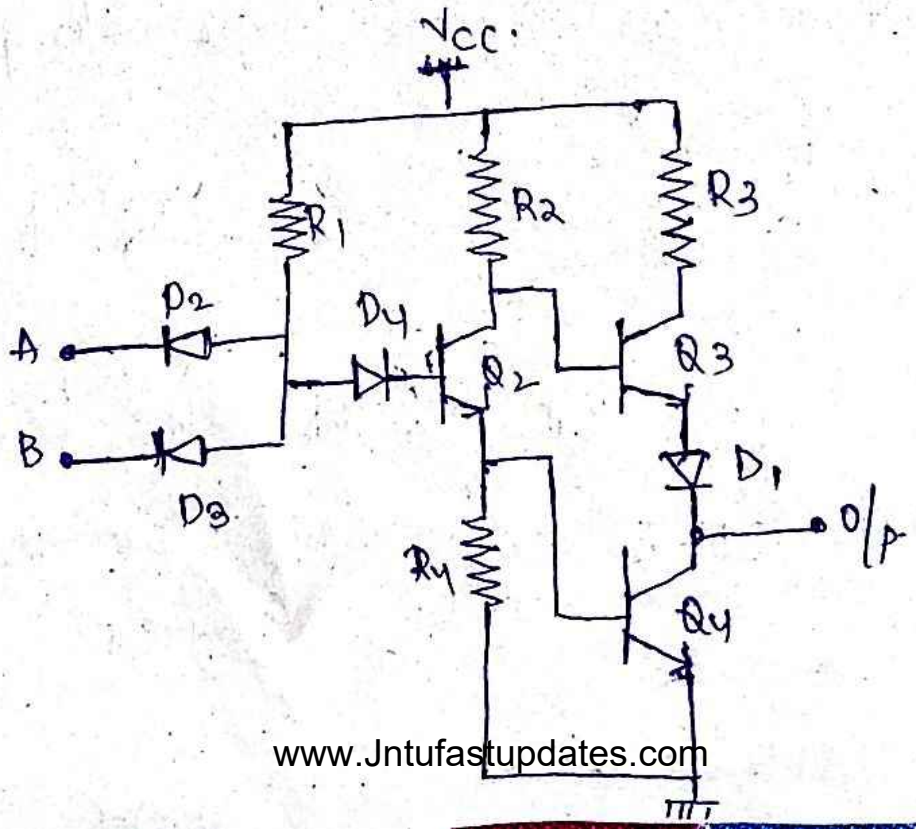
(iv) logic Gates are Used in integrated logic families

i.e., TTL (Transistor transistor logic)

CMOS (Complimentary metal oxide Semi Conductors).

TTL NAND Gate (TOTEMPOLE Nand Gate)





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Truth table :-

A	B	A·B	$\bar{A}\cdot\bar{B}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Case (i):- When all i/p's are high, If A & B are high Diode "D_1", Diode "D_3", "D_2" OF, D_4 is ON.

i.e., D_2 & D_3 are Reverse bias.. and hence their diodes are off position & there is no Conduction through them.

→ The Supply Voltage Vcc passing a Current through the Resistance "R_1" and the diode "D_4" get forward bias and It allows to the Based of transistor Q_2 then Q_2 is ON Condition.

∴ The Q_4 is "ON".

then the O/p from the Ckt is low.

logic truth table :-

A	B	D_2	D_3	D_4	Q_2	Q_3	Q_4	D_1	Q_p
L	L	ON	ON	ON	OFF	OFF	ON	OFF	High
L	H	ON	OFF	ON	OFF	OFF	ON	OFF	High
H	L	OFF	ON	ON	OFF	OFF	ON	OFF	High
H	H	OFF	OFF	OFF	ON	ON	OFF	ON	low

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C-MOS :-

→ The C-MOS logic gates Complimentary metal oxide Semi Conductor

→ The C-MOS Consists of '2' parts

(i) P MOS (or) P- Channel.

(ii) N MOS (or) N- Channel.

→ In C-MOS logic Gates are Constructed Design by using P-MOS & N-MOS

→ In the C-MOS logic Gates the top level having P- Channel, Bottom level having N-Chan

→ The o/p is Considered (or) taken in the P-MOS & N-MOS

Hence the o/p. of q

Sink:—

The considerable current gets grounded through the i/p terminal that i/p terminal having low voltage it acts as sink to the ckt. Hence, about to the TTL logic gates work as NAND gate.

CMOS logic gate:—

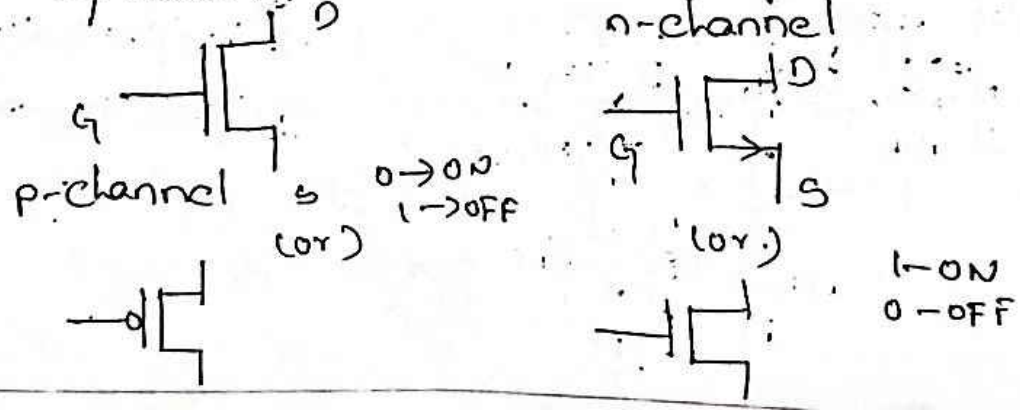
There are two types of FETS.

(i) JFET

(ii) MOSFET

Mos transistors can be fabricated in less area compared to by bipolar transistors.

Symbols:



PMOS, NMOS
AND Parallel series
OR - series Parallel

CMOS ckt having two types of MOS devicies.
i.e p-channel
n-channel.

CMOS devices are chips in which both p-channel, n-channel MOSFETS are connected in a push-pull arrangement.

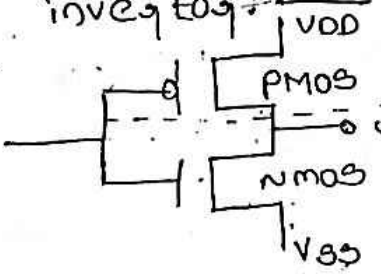
The n-channel MOSFET conducts when its gate to source voltage is positive.

The p-channel mos conducts when its gate to source voltage is negative.

Chaqacteqistics of CMOS:

* It is simple and cheapeq. in fabqication
* It is small in size and consume veqy less poweq.
* poweq dessipation is very low.
* Fabrication of MOS ICs is not so complex as TTL ICs.
* MOS ICs dont use the Ic qesistance element so they occupy veqy less space in chip
* Low operating speed

CMOS inveqtoq:



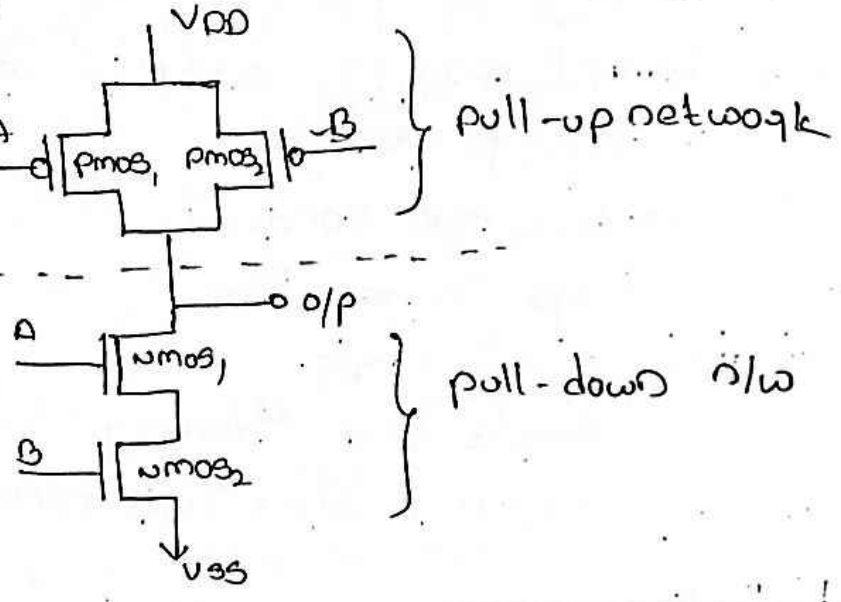
i/p	o/p
low	high
high	low.

when the i/p is low NMOS doesn't conduct it is open circuited, but PMOS will conduct and it acts as shqt ckt then VDD is appeqs

at the o/p. Hence o/p is high (1)
when the i/p is high pmos doesn't conduct it is open circuited and nmos will conduct. It acts as s.c to ground. Hence o/p is low(0)

CMOS NAND gate:—

A	B	$Y=\overline{A\cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0



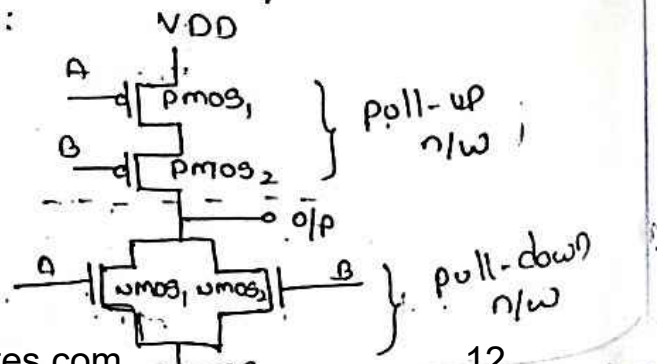
case(i):
when both the i/p's are A=0 & B=0 pmos conducts, nmos doesn't conducts so VDD appears at the o/p. Hence, o/p is high (1)

case(ii):
when both the i/p's are high i.e A=1 & B=1 PMOS doesn't conduct & nmos conducts it is connected to the ground hence o/p is low.

case(iii):
when any one of i/p is low one of the PMOS will conduct. Hence, o/p is high.

CMOS NOR gate:—

A	B	$Y=\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0



case(i):

when the both i/ps are low ie A=0 & B=0 then both PMOS are conduct and VDD is appeag at o/p. Both NMOS are doesn't conduct hence o/p is high.

case(ii):

when any one of i/p is high & both the i/p are high. The NMOS will conduct s.c to ground PMOS will'nt conduct hence VDD is not appeaging at the o/p. So o/p is Low (0).

pull-up network:

pull-up network is a PMOS switches with one terminal connected to VDD & another terminal is connected to the o/p.

pull-down network:

pull down network is a NMOS switches with one terminal is connected to o/p and another terminal is connected to Vss which is grounded

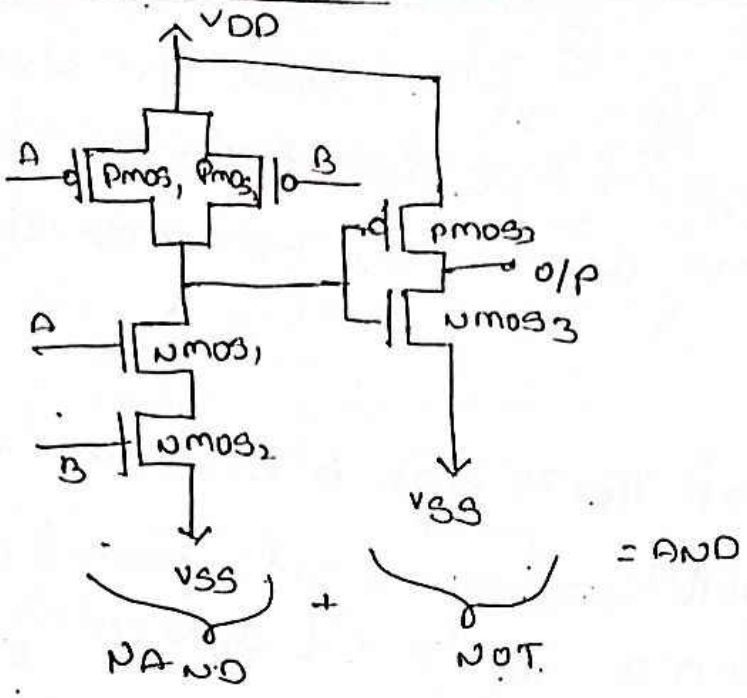
Demoycation line:

It is aline which seperates pull up network and pull down network.

CMOS AND gate:—

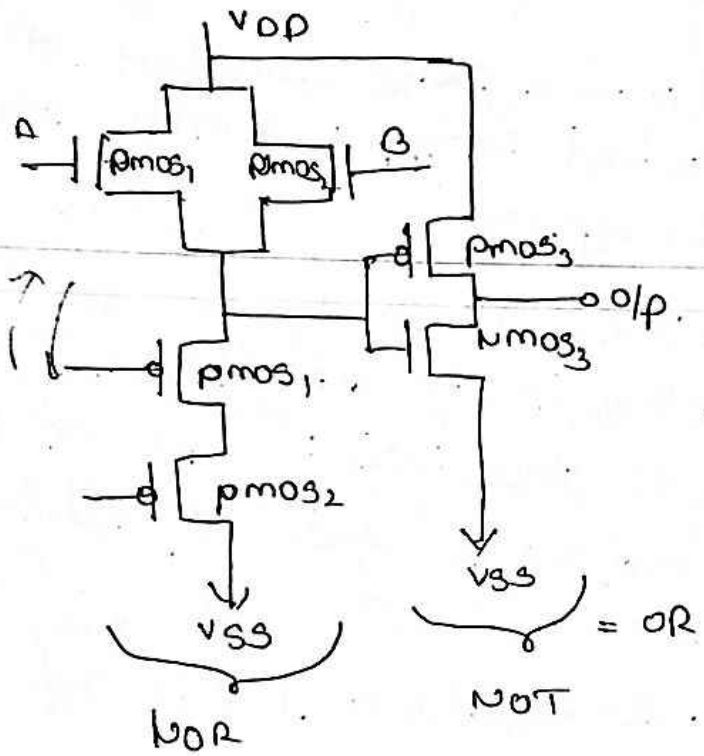
CMOS NAND gate followed by inverter is called CMOS AND gate.

A	B	$PMOS_1$, $PMOS_2$	$NMOS_1$, $NMOS_2$	$PMOS_3$	$NMOS_3$	o/p
0	0	ON	OFF	OFF	ON	1
0	1	ON	OFF	ON	OFF	0
1	0	OFF	ON	OFF	ON	0
1	1	OFF	ON	ON	OFF	1



A	B	Y = A.B
0	0	0
0	1	0
1	0	0
1	1	1

CMOS OR gate:—

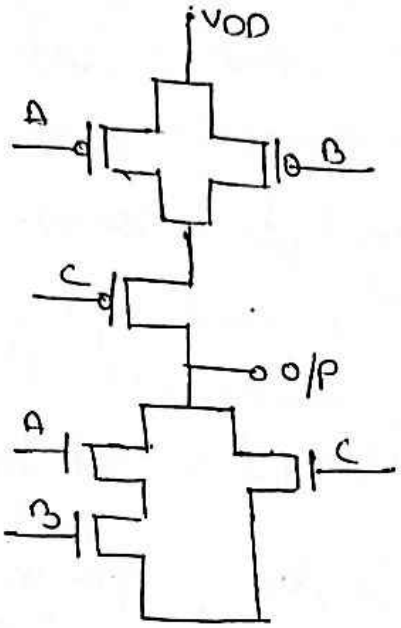


A	B	Y = A+B
0	0	0
0	1	1
1	0	1
1	1	1

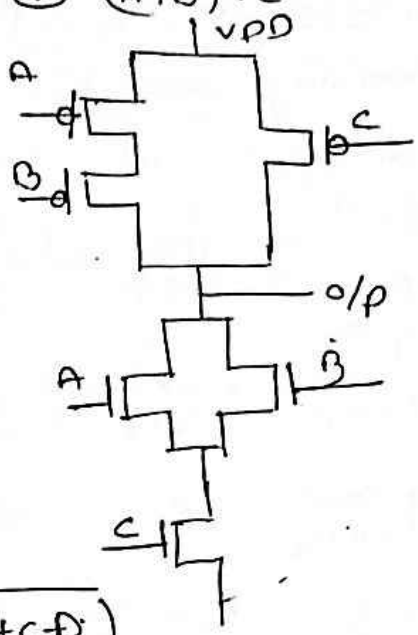
A	B	nmos1	nmos2	pmos1	pmos2	pmos3	nmos3	o/p
0	0	OFF	OFF	ON	ON	OFF	ON	0
0	1	OFF	ON	ON	ON	ON	OFF	1
1	0	ON	OFF	OFF	ON	ON	OFF	1
1	1	ON	ON	OFF	OFF	ON	OFF	1

NOT important:—

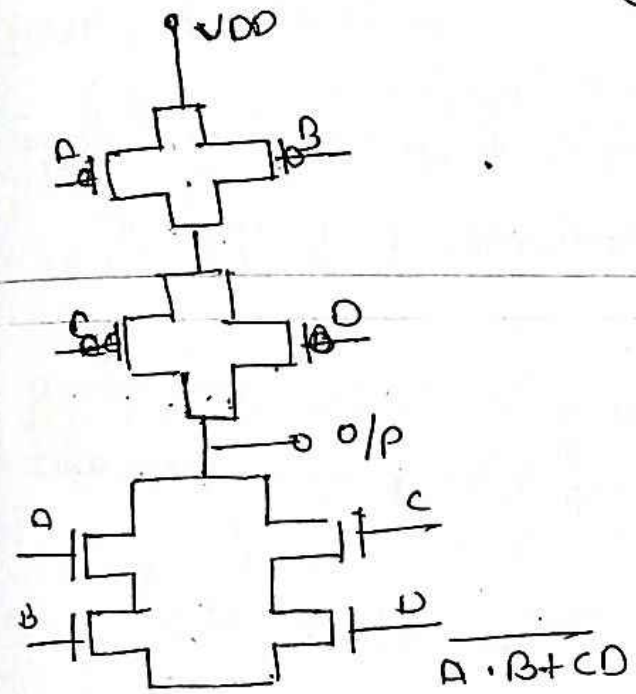
① $\overline{AB+C}$



② $\overline{(A+B)\cdot C}$

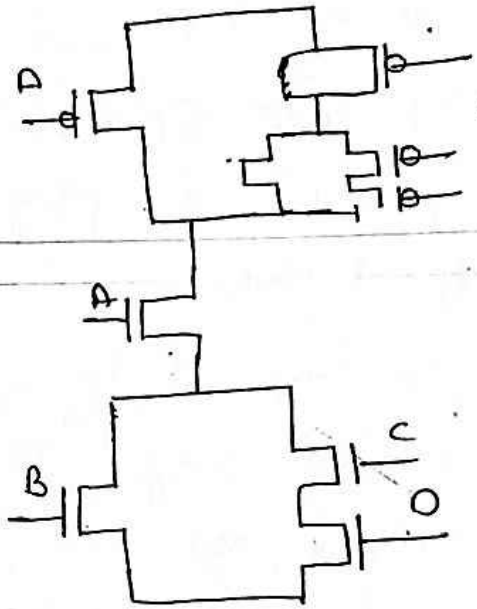


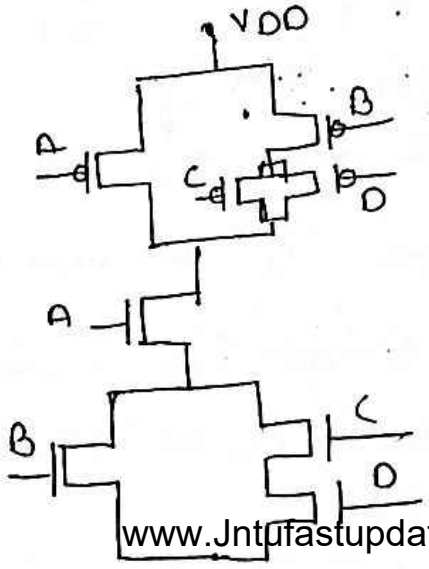
③ $\overline{AB+CD}$



$\overline{A\cdot B+CD}$

④ $\overline{A(B+C\cdot D)}$





Comparision b/n logic family:—

Parameter	RTL	DTL	TTL	ECL	CMOS
Noise immunity	average	good	very good	avg	very good
Power dissipation per gate	12	8-12	10	40-55	0.01 static. 1mw at 1MHz
Propagation delay per gate	14	30	10	2	70
fig of merit	168	300	100	95	0.7
clocking Rate (MHz	8	72	35	above 60	10
fan out	5	8	10	25	above 70.

Imp

Note:—

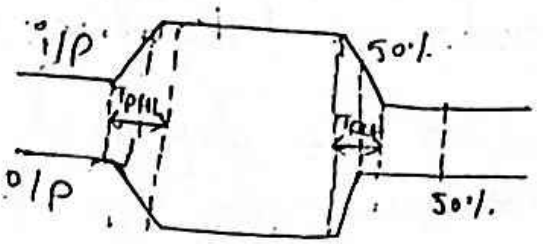
* ECL logic family is the fastest logic family compared to other logic families (propagation delay is low)
* High fan out logic family is CMOS and also it having very less power dissipation compared to other logic families.
* fig of merit point of view DTL is the suitable logic family.

Characteristics of logic family:—

Propagation delay:

Propagation delay is the maximum time taken by o/p to change its state in response to i/p, it determine the speed of operation of the gate.

propagation delay (tp) is average of two times t_{PHL} & t_{PLH} and the times are measured from 50% of voltage level.



* t_{PHL} is the time delay when o/p goes from high to low state.

* t_{PLH} is time delay taken by o/p to go from low to high state...

$$t_p = \frac{t_{PLH} + t_{PHL}}{2}$$

power dissipation:

power dissipation is defined as the power dissipated in an IC and it is measured in mw.

** Lower power dissipation is desirable in any digital IC

fig of merit: —

fig of merit is defined as the product of propagation delay and dissipation. It is measured in pico Joules. fig of merit is also known as speed power product.

fig of merit = propagation delay × power dissipation

$= t_p \times P_D$ = nanosec * milliwatts

$= 10^{-9}$ sec * 10^{-3} watts

$= 10^{-12}$ sec * watts

= pJ

fan in:

It is defined as the no. of i/p (coming from similar ckts) the logic gates can handle properly.

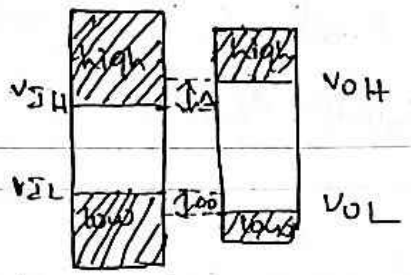
fan out:— (loading factor)

It is defined as the maximum no. of standard logic i/p that an o/p can drive without effecting i/p.

High fan out is desirable.

Noise immunity:

The ability of a logic ckt to tolerate the effect of noise is called noise immunity. The amount by which a ckt can effect of noise (or) quantitative measure of noise immunity is called noise margin.



$\Delta_1 = V_{OH} - V_{IH}$

$\Delta_0 = V_{IL} - V_{OL}$

fig i/p vol fig: o/p voltage

Δ_1 is noise margin at high state

Δ_0 is noise margin at low state.

operating temperature:

Digital Ic's operating for temperature range from 0 to 70° for industrial applications and the range of −55 to 125° for military applications.

X. Sampling gates (Part-B)

Introduction:

To produce the o/p that is same as i/p signal within a specified time interval is called sampling gates. Another name for sampling gates are transmission gates, linear gates, selection gates. The time interval for transmission is selected by external impressed signal which is called the gating signal (or) controlled signal (or) selector signal (or) enable signal.

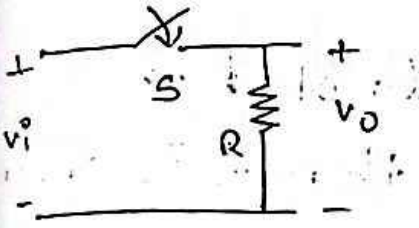


Fig: sampling gate using series switch

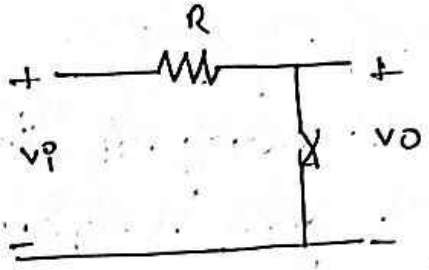


Fig: sampling gate using shunt switch.

The basic operating principle of sampling gate is shown in above fig (a) & (b). In fig (a) the switch is normally open but it is in closed position when a signal is transmitted. These switches are normally electronic devices like diodes (eg) transistor. when the diode is conducting it act as closed switch, and it is not conducting it act as open switch.

In fig(a):

S is open $\rightarrow v_o = 0$

S is close $\rightarrow v_o = v_i$

In fig(b):

S is open $\rightarrow v_o = v_i$

S is close $\rightarrow v_o = 0$

Types of sampling gates:—

Depending on polarities of i/p signal. There are two types of sampling gates.

(i) unidirectional sampling gates

(ii) Bi directional sampling gates.

unidirectional sampling gates:

If the sampling gate responds to an i/p signal of only one polarity then the sampling gate is called unidirectional sampling gates.

Bidirectional sampling gates:

If there are many i/p signals of both polarities that a gate responds then it is called bidirectional sampling gates.

unidirection diode gate:

A unidirectional diode gate which transmits only the +ve going i/p signal is shown in above fig.

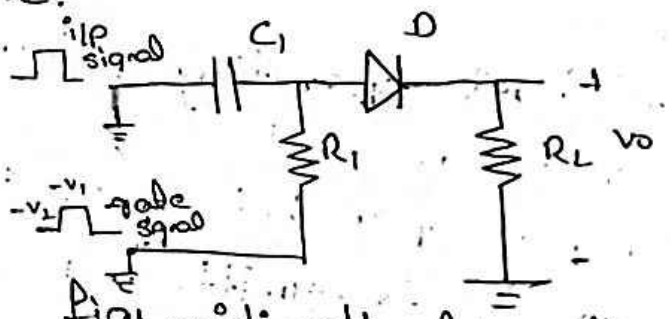


Fig: unidirectional sampling gate

The gate signal i.e the signal which determines transmission period is a rectangular wave form that make transmission b/n the two negative levels $-V_1$ & $-V_2$

when the gate signal is at its lower level $-V_2$ the diode is reverse bias and there will be no o/p.

To the i/p signal, the peak amplitude of i/p signal is greater than the magnitude of the reverse bias voltage, when the gate signal is at its upper level V_1, a time coinciding signal i/p pulse may be transmitted to o/p.

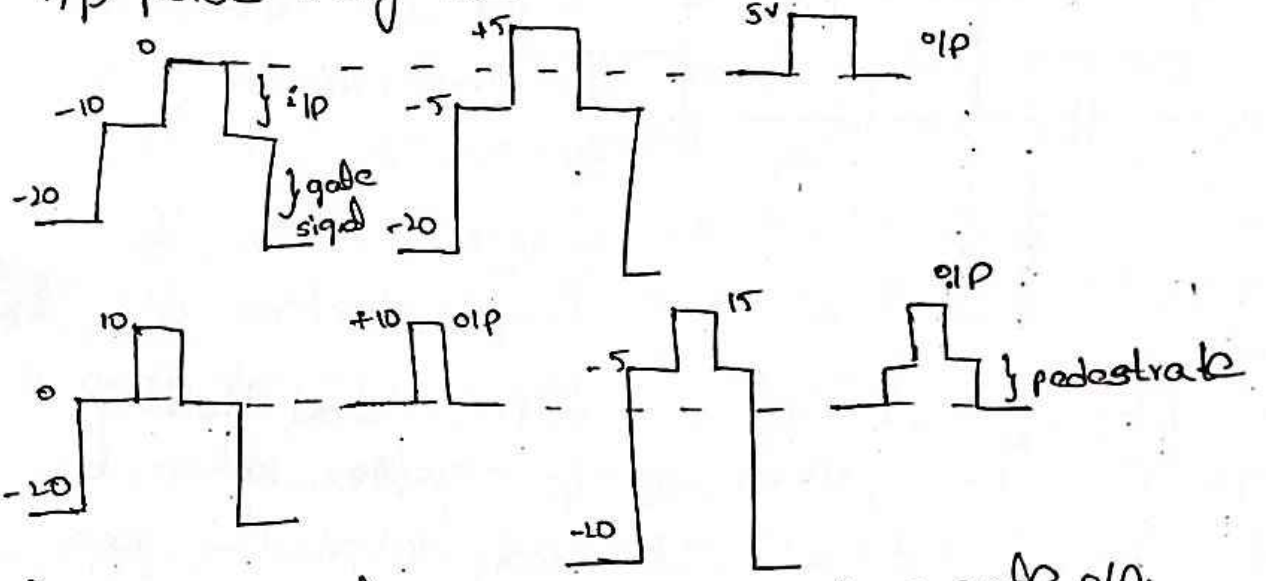


Fig: effect of control voltage (-V1) on gate o/p.

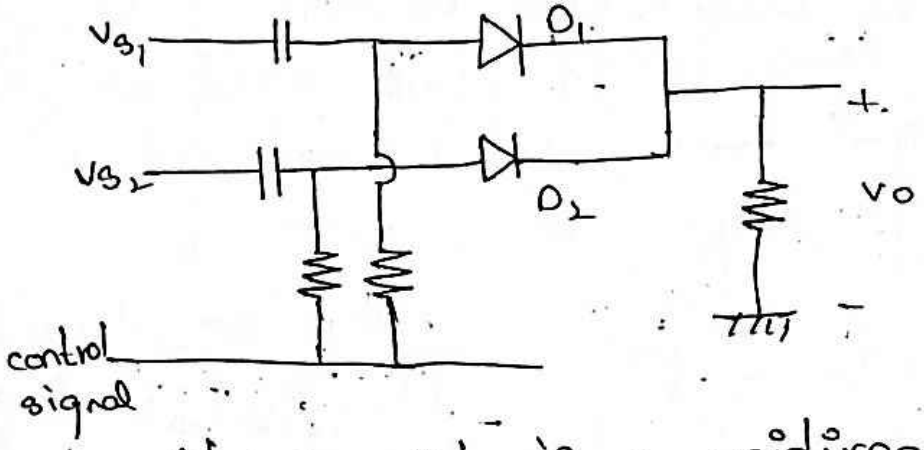
Advantages: —

* It is very simple ckt
* The time delay is small since i/p and o/p couple directly through the capacitor and diode.
* The sampling gate draws no current in its quiscent condition
* The sampling gate can be extended into a multi i/p OR gate with NOT terminal.

Disadvantages:

* There is interaction b/n the i/p signal source and the control voltage source and this is undesirable
* The sampling gate is only limited use in practically only modification made in the

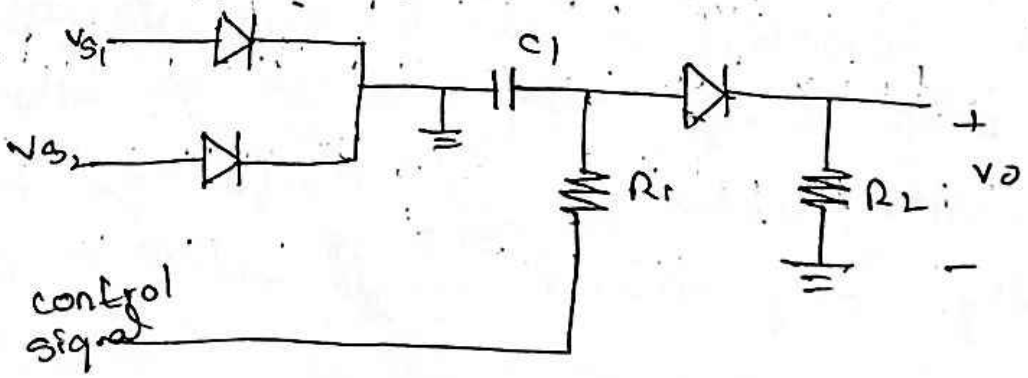
ckt to improve the performance may cause unwanted attenuation of i/p signals.
unidirectional diode gates to accommodate more than one i/p signals:



Above ckt is a unidirectional diode sampling gate with two i/p signals when the control signal is at its lower level the gate transmittes no i/p's. when the control signal is at its higher level the sampling gate acts as capacitively coupled 'OR' gate.

The drawback of this ckt is the no. of i/p increases, the loading and the control signal becomes excessively heavy. This difficulty may be overcome by using one more diode as shown in below fig.

In this ckt the control o/p voltage doesn't feed into the signal sources

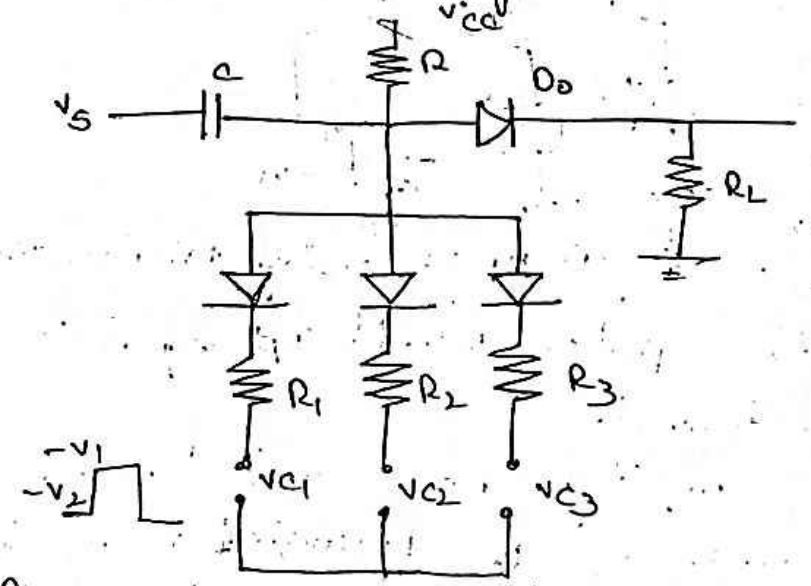


If the no of control signal are more and only one signal source having sampling gate as shown in below fig.

below figural having a diode gate which will transmits only when the no of gate voltage across simultaneous a no of control signals are V_{C1}, V_{C2}, V_{C3} are required.

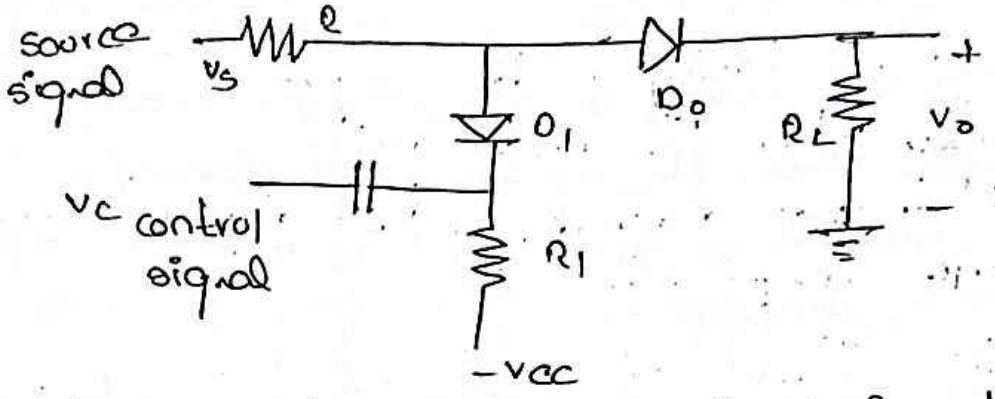
Let all the signals at levels $-V_2$ & $-V_1$ when any of the control signal is at $-V_1$ then total voltage is goes to ground. so o/p is zero.

when all control voltages are at $-V_1$ then the signal is sampled hence o/p equal to the i/p. This circuit acts as AND gate.



A sampling gate whose response is not sensitive to the upper level of the control voltage, is shown in below fig. Intially the absence of gating signal at the control terminals the diode D_1 conduct and D_0 is in reverse bias, when +ve going gate signal gives to the diode D_L is

in OFF state. Hence the source signal is sampled for the duration of the control pulse.



bidirectional sampling gate using transistors:

In the above ckt the i/p voltage source v_s and the control voltage v_c applied through the resistors R_1 & R_2 to the base of the transistor. The control voltage v_c is a pulse wave form b/w the levels V_1 & V_2 and with a pulse width T_p equal to desired Transmission interval.

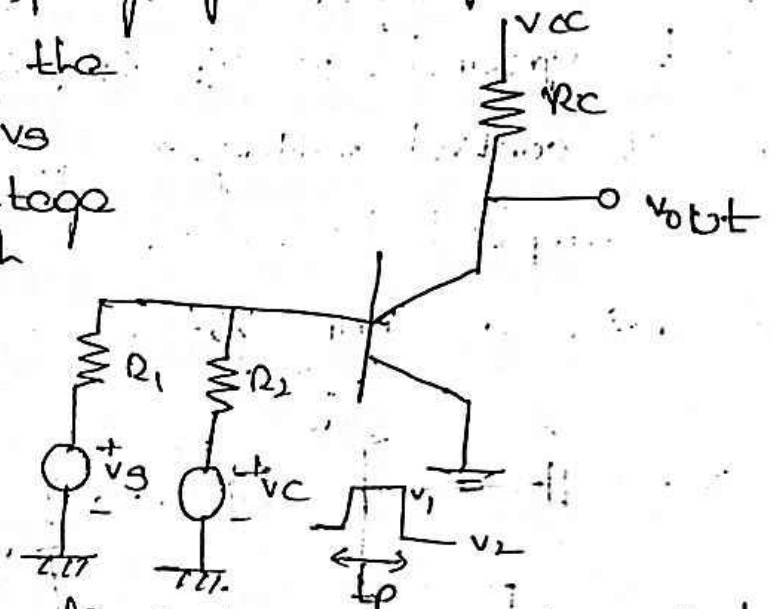
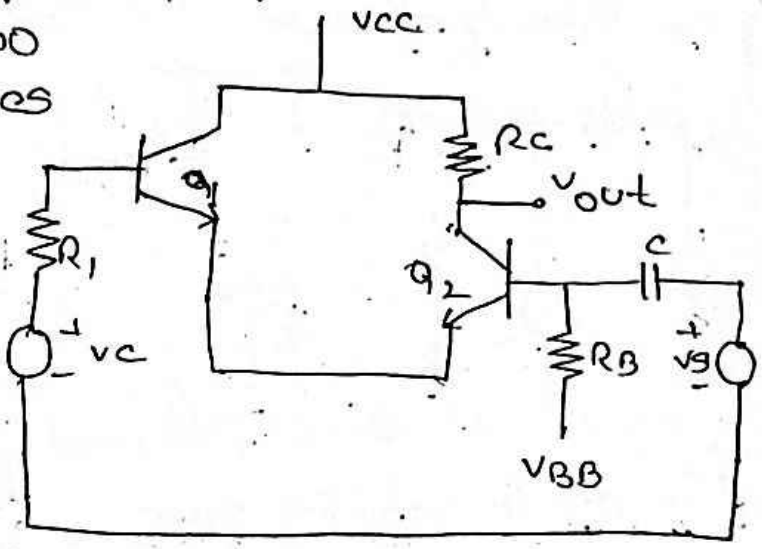


fig: A BDSG using transistor

when the sampling gate control voltage is at its lower level v_2 the transistor is in cut off region. when the control signal is at its upper level v_1 the bias brings the transistor into the active region: so, the signal both polarities +ve & -ve will amplified at the o/p. Hence the above ckt acts as bidirectional sampling gate.

Bidirectional sampling gate using two transistors:



In the above ckt two transistors seperate bases are available for the i/p signals and control signal. The control signal having two levels. The upper level V_1 and lower level V_2. when the control voltage V_c is at its upper level V_1, Q_1 becomes on and the resulting emitter current through the Re large enough to rise the emitter voltage of Q_2 then Q_2 goes to cut off region. Hence there is no transmission of the i/p signal to the o/p.

when the control voltage V_i at it's lower level V_2. The Q_1 is cut off and Q_2 is in active region, it acts as amplifier thus it transmits the i/p signal in the amplified form at the o/p for the duration of control signal.

Advantages:

During sampling interval Q_1 is cut off and hence there is no coupling b/w the i/p signal and control signal. This reduces the loading effect on the signal source.

Bidirectional sampling gates using diodes:—

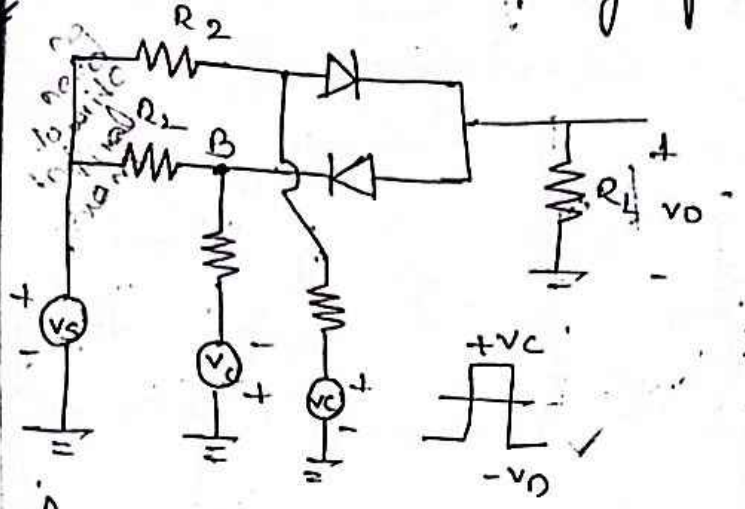


Fig: Diode sampling gate

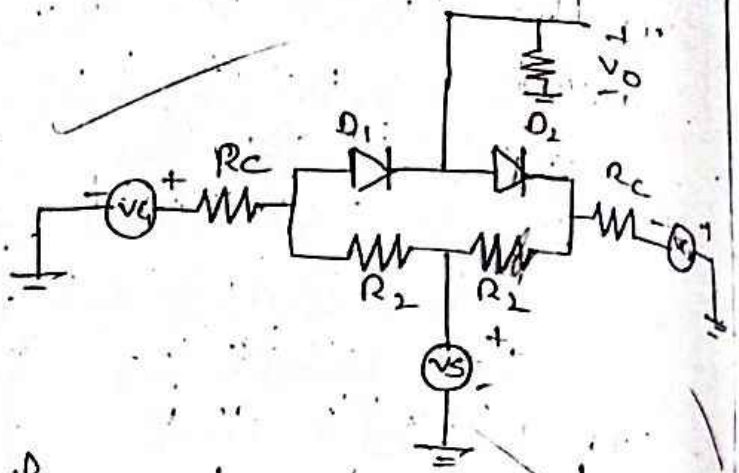


Fig: Diode sampling gate in the form of bridge n/w.

The main advantages of bidirectional sampling gates using diodes compared to bidirectional sampling gates using transistors.

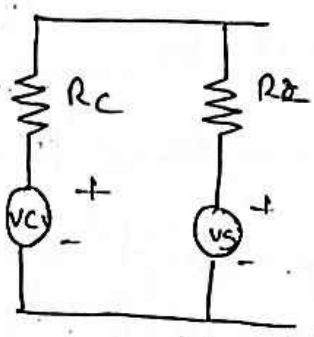
(i) Linearity of operation
(ii) reducing the pedestal.

Above ckt requires two symmetrical control signals $+V_c$ and $-V_c$ when the control voltages are at the levels $+V_0$ and $-V_0$ respectively the diodes are reverse biased and hence there is no transmission i/p signal to the o/p. when the control voltages are at the levels $+V_c$ and $-V_c$ then the diodes D_1 & D_2 are forward biased. And Hence there is the transmission of i/p signal to the o/p For the duration control signal pulses. If provide the characteristics of the diodes are identical and due to the symmetry

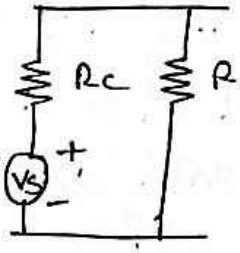
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of the o/p zero pedestral appearing at o/p. gain of two diodes sampling gates.

From the above bridge ckt left hand side is,



by applying superposition theorem & thevenins theorem, due to Vs



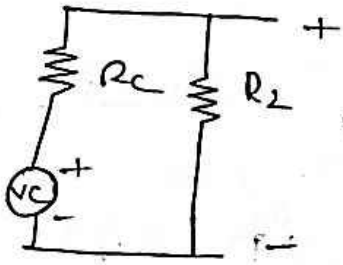
$$V_{th_1} = \frac{R_c}{R_2+R_c} V_s$$

If $\alpha = \frac{R_c}{R_2+R_c}$ then

$$V_{th_1} = \alpha \cdot V_s$$

$$R_{th_1} = \frac{R_c \cdot R_2}{R_c+R_2}$$

Due to V_c:



$$V_{th_2} = \frac{R_2}{R_2+R_c} V_c = \left(1-\frac{R_c}{R_2+R_c}\right) V_c$$

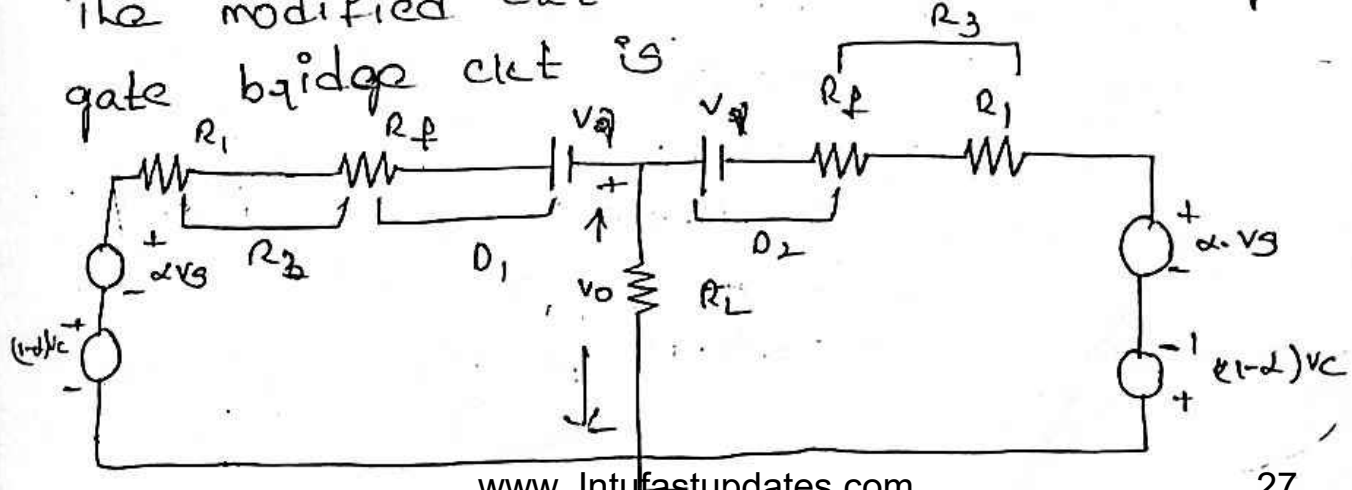
$$= (1-\alpha) V_c$$

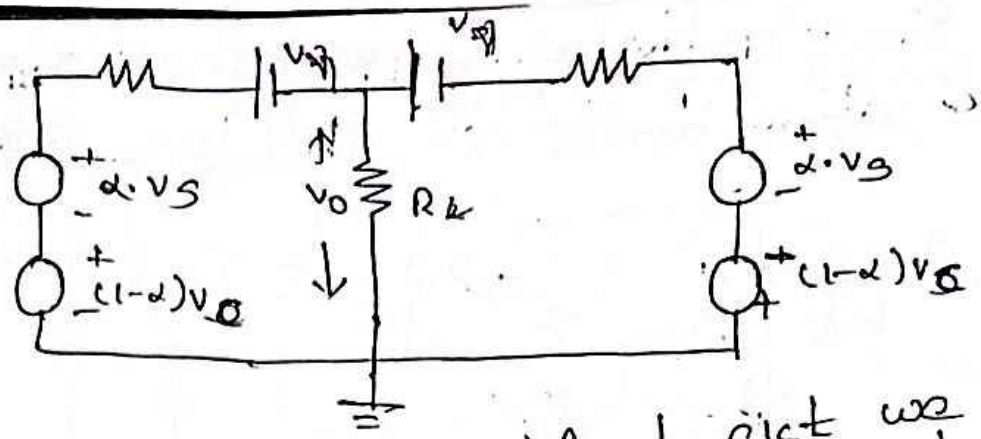
$$R_{th_2} = \frac{R_c \cdot R_2}{R_2+R_c}$$

$$R_{th_1} = R_{th_2} = \frac{R_2 R_c}{R_2+R_c}$$

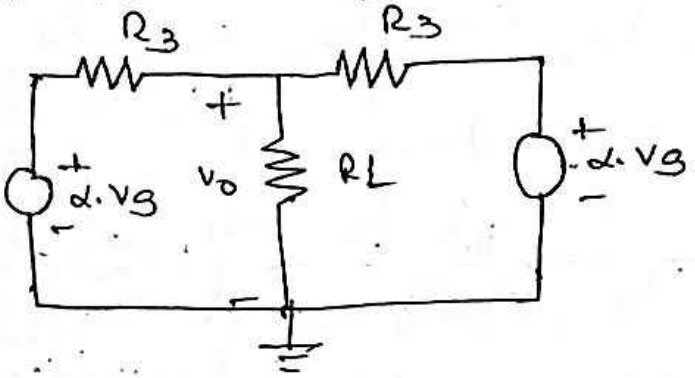
Let $R_1 = R_{th_1} \cdot R_{th_2}$

The modified ckt of two diode samping gate bridge ckt is





From the above equivalent ckt we can observe that the voltages V_y and $-V_y$ and the control voltages $(1-\alpha)V_c$ & $(1-\alpha)V_c$ tried to send equal currents in opposite directions in R_L and hence the current due to them is zero. so neglect the V_y and $(1-\alpha)V_c$ values.



$$V_{th_1} = \frac{R_3}{R_3+R_3/2}\,\alpha.V_g \qquad V_{th_2} = \frac{R_3}{R_3+R_3/2}\,\alpha.V_g$$

$$R_{th_1} = \frac{R_3 R_3}{R_3+R_3} \qquad R_{th_2} = \frac{R_3 R_3}{R_3+R_3}$$

$$= \frac{R_3}{2} \qquad = \frac{R_3}{2}$$

$$V_{th} = V_{AB} = \frac{R_L}{R_L+\frac{R_3}{2}} \cdot \alpha V_g$$

$$\therefore \frac{V_o}{V_g} = \alpha \cdot \frac{R_L}{R_L+\frac{R_3}{2}} \qquad \therefore \alpha = \frac{R_C}{R_C+R_2}$$

$$= \frac{R_C}{R_C+R_2} \times \frac{R_L}{R_L+\frac{R_3}{2}}$$

control voltages:——

$V_c min$ = minimum control voltages both the diodes are forward bias.

$V_B(min)$ = minimum control voltage both the diodes are reverse biased.

If v_s is a +ve signal the current in D_2 decreases and hence the difference current flows through the R_L as v_s is continuously increases. The current in diode D_2 becomes zero, i.e D_2 will be cut off. To compute $v_c(min)$ assume D_2 has just stopped conducting. In the equivalent ckt the voltage across R_3 is associated with D_2 is zero neglecting the V_γ.

The o/p voltage must be equal to the αv_s

$\alpha v_s - (1-\alpha) v_c$ (when calculate from RHS)

$\frac{R_L}{R_L+R_3} \times [\alpha v_s + (1-\alpha) v_c]$ is o/p voltage from

LHS side

L.H.S = R.H.S

$$\frac{R_L}{R_L+R_3} \times [\alpha v_s + (1-\alpha) v_c] = \alpha v_s - (1-\alpha) v_c$$

$$\alpha v_s \left[1 - \frac{R_L}{R_L+R_3}\right] = (1-\alpha) v_c \left[1 + \frac{R_L}{R_L+R_3}\right]$$

$$\alpha v_s \left[\frac{R_3}{R_L+R_3}\right] = (1-\alpha) v_c \left[\frac{2R_L+R_3}{R_L+R_3}\right]$$

$$v_c = \frac{\alpha}{1-\alpha} \cdot v_s \cdot \frac{R_3}{R_L+R_3} \times \frac{R_L+R_3}{2R_L+R_3}$$

$$V_c(min) = \frac{\alpha}{1-\alpha} V_s \cdot \frac{R_3}{2R_L+R_3}$$

$$\alpha = \frac{R_c}{R_2+R_c}$$

$$V_c(min) = \frac{R_c}{R_2} \cdot \frac{R_3}{2R_L+R_3} \cdot V_s$$

→ D_1 is conducting.

→ D_2 is just stopped conducting.

This is a minimum value to control voltage required to signal transmission over full range of i/p signal by keeping both the diodes are conducting.

$V_n(min)$:

It is the minimum voltage required to keep both the diodes are reverse biased.

The voltage across D_1 is $\alpha V_s - (1-\alpha)V_n$

Diode 'D_1' is reverse biased and hence o/p voltage is zero.

$$\alpha V_s - (1-\alpha)V_n = 0$$

$$V_{n\,min} = \frac{\alpha}{1-\alpha} V_s$$

$$\alpha = \frac{R_c}{R_c+R_2}$$

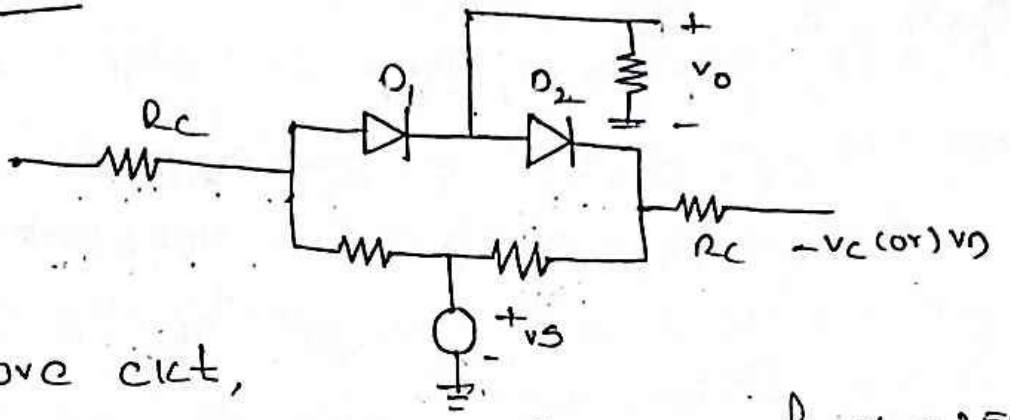
$$V_n(min) = \frac{R_c}{R_2} V_s$$

Disadvantages of two diodes sampling gates:

* It is sensitive to the control voltage
* It having low gain.

Problem:—

1.



In above ckt,

$R_L = R_S = 100k\Omega$, $R_2 = 2K$, $R_f = 50\Omega$. for $V_S = 25V$

calculate gain, $V_C(min)$, $V_O(min)$.

$$V_C(min) = \frac{\alpha}{1-\alpha} V_S \cdot \frac{R_3}{2R_L + R_3}$$

$$V_C(min) = \frac{R_C}{R_2} \cdot \frac{R_3}{2R_L + R_3} V_S$$

$$= \frac{100\times10^3}{2\times10^3} \cdot \frac{2.01\times10^3}{2(100) + 2.01k} \times 25 = 0.497k\Omega \times 25 = 12.4\,V$$

$R_1 = R_2 // R_C$

$= 2k // 100k\Omega$

$= 1.96k\Omega$

$R_3 = R_1 + R_f$

$= 1.96k + 50\Omega$

$= 2010$

$= 2.01k\Omega$

$$\text{Gain } A = \frac{R_C}{R_2 + R_C} \times \frac{R_L}{R_L + R_3/2}$$

$$= \frac{100}{2+100} \times \frac{100}{100 + \frac{2.01}{2}}$$

$$= 0.97$$

$$V_O(min) = \frac{R_C}{R_2} \cdot V_S$$

$$= \frac{100k}{2k} \times 25 \neq 12.5\,kV$$

$$= 1.25\,kV$$

② In the ckt $R_L = R_C = 100k$, $R_2 = 50k$ and the signal have peak value of 50V find the gain & $V_C min$, $V_O(min)$.

Gain, $A = \frac{R_c}{R_c+R_2} \cdot \frac{R_L'}{R_L+\frac{R_3}{2}}$

$R_3 = R_1 + R_f$ $\quad R_L = R_2 // R_c$

$= 33.3K$ $\quad = 50K // 100K$

$= 33.3K$

$= \frac{100K}{100K+50K} \cdot \frac{100K}{100K+\frac{33.3K}{2}}$

$= 0.571\ K$

(ii) $V_{c(min)}$

$\frac{R_c}{R_2} \cdot \frac{R_3}{R_3+2R_L}$

$\frac{100K}{50K} \cdot \frac{33.3K}{33.3+2(100)} = 0.285$

(iii) $V_{n(min)}$

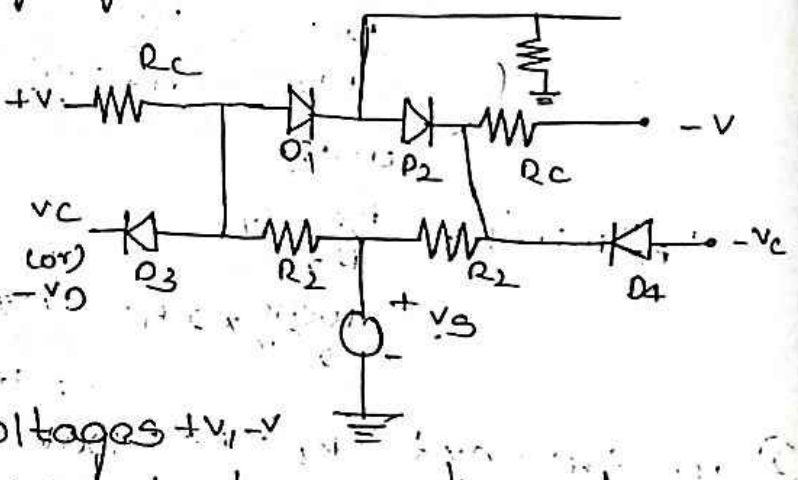
$= \frac{R_c}{R_2} \cdot V_s$

$= \frac{100}{50} \cdot 20 = 40KV$

VI-unit

Diode sampling gate:

Four diode sampling gate is used for improving the gain of the ckt. It having extra two diodes and two voltages $+V_1, -V$ required compared to 2- diode sampling gate. when the control voltages $+V_c$ and $-V_c$ then the diodes D_3 and D_4 reverse bias.



The diodes D_1 and D_2 forward bias. The signal source is coupled to the load through the R_2, during the transmission D_3 and D_4 are OFF condition the ckt is same as two diode sampling gate, except the voltages V_c and $-V_c$ replaced by $+V$ and $-V$. when the control voltages are $+V_{ss}-V_D$ the diodes D_3 & D_4 forward bias and D_1 & D_2 RB the o/p is If D_3, D_4 reverse bias then 4 diode sampling gate equal to 2 diode sampling gate so gain also same.

$$\therefore \text{gain } A = \frac{R_c}{R_c+R_2} \cdot \frac{R_L}{R_L+\frac{R_3}{2}}$$

The V_{min} of the ckt is same as the $V_c(min)$ of the 2 diode sampling gate. so,

$$V_{min} = \frac{R_c}{R_2} \cdot \frac{R_3}{R_3+2R_L} \cdot V_s$$

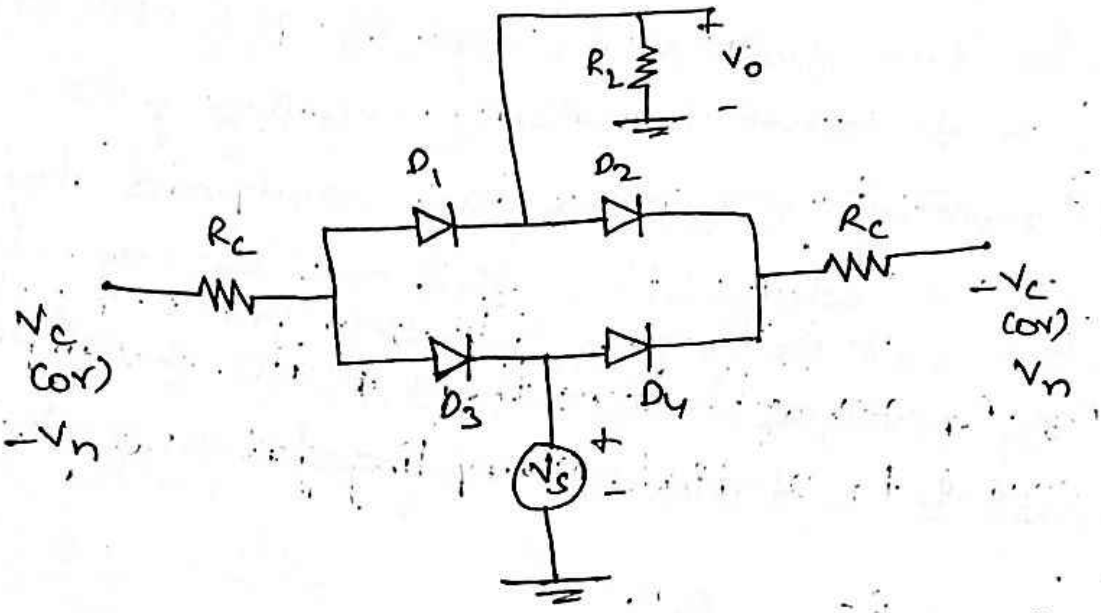
If the diode D_3 is continously reverse bias. The V_c must be equal to $A.V_s$

$$V_c(min) = A.V_s$$

The voltage V_D must be selected not only to keep the transmission diodes D_1 & D_2 reverse bias but also keep the diodes D_3 & D_4 in forward bias in the presence of i/p signal V_s.

$$V_D(min) = \frac{V_s \cdot R_c}{R_c+R_2} - \frac{V \cdot R_2}{R_2+R_c}$$

4 - diode sampling gate (Alternate form):-

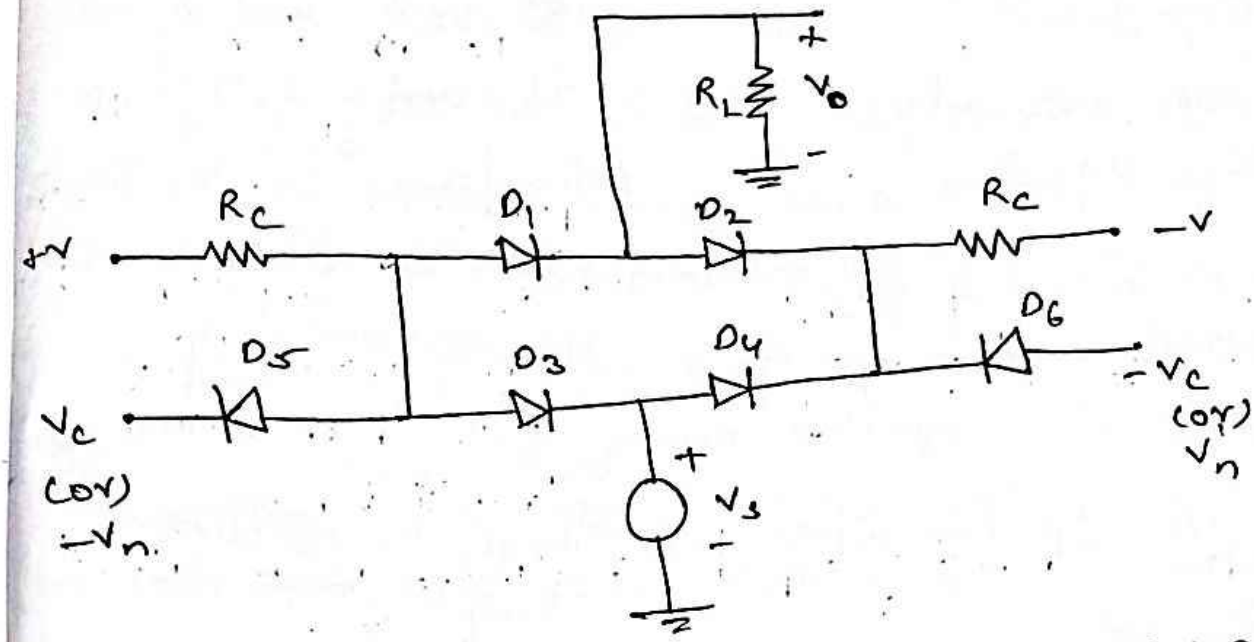


In this circuit, supply voltages +V & -V not present but to avoid pedestal $+V_c$ and $-V_c$ must be balanced.

when the control voltages are at the levels V_c and $-V_c$, all the 4 diodes forward bias and source signal is connected to the load through 2 parallel paths each consisting of two diodes in series, so the source signal goes to output.

when the control voltages are at the levels V_n & $-V_n$, all the 4 diodes are reverse bias. so, there is no transmission. the required voltages V_c and $-V_c$ depends on the amplitude of source signal 'V_s'.

6- diode sampling gate :-



During the transmission, diodes D_1, D_2, D_3 & D_4 in forward bias, but diode D_5 & D_6 are reverse bias, thus the 6-diode sampling gate becomes equivalent to the 4-diode sampling gate. when the o/p is zero i.e when there is no transmission, the diodes D_1, D_2, D_3 & D_4 are in reverse bias but the diodes D_5 & D_6 are forward bias.

For 6-diode sampling gate,

$$V_C(min) = V_n(min) = V_s$$

gain (A) $\cong 1$

$$V_C(min) = V_s \left[2 + \frac{R_C}{R_L}\right]$$

VI unit

(*) Diff b/n the unidirectional sampling gate and & bidirectional sampling gate.

unidirectional	Bi-directional
(i) It can pass only one polarity signal	(i) It can pass both polarities (+ve & -ve)
(ii) These sampling gates are constructed using diodes	(ii) These sampling gates are constructed using diodes and transistors.
(iii) I/p is directly coupled to the o/p	(iii) There is no direct coupling
(iv) As no. of i/p signals increases, the loading on the i/p increases heavily	(iv) There is no coupling b/n the i/p signal and control signal and hence the loading effect is reduced on the source signal.
(v) This ckt can be extended to a large no. of i/ps	(v) It is not possible to extend the ckt for many i/p signals.

Applications of sampling gates: —

(i) multiplexers
(ii) sample and hold ckt
(iii) Analog to digital converter (ADC)
(iv) chopper amplifier
(v) sampling scopes.

* In sample and hold ckts, the sampling gates are used to hold the voltage sample constant for a specified time.

* sampling gates are used to convert the amplitude samples of analog voltage to a digital number represented by the condition of flipflops.

* Sampling is done by synchronous, demodulate (or) which makes the output voltage 'V_o' to take the shape of input signal 'V_i' by passing 'V_o' through a low ~~shap~~ pass filter such that only signal frequency appears at output and the square wave rejected.

* In this way, the amplified replica of the original signal is obtained.

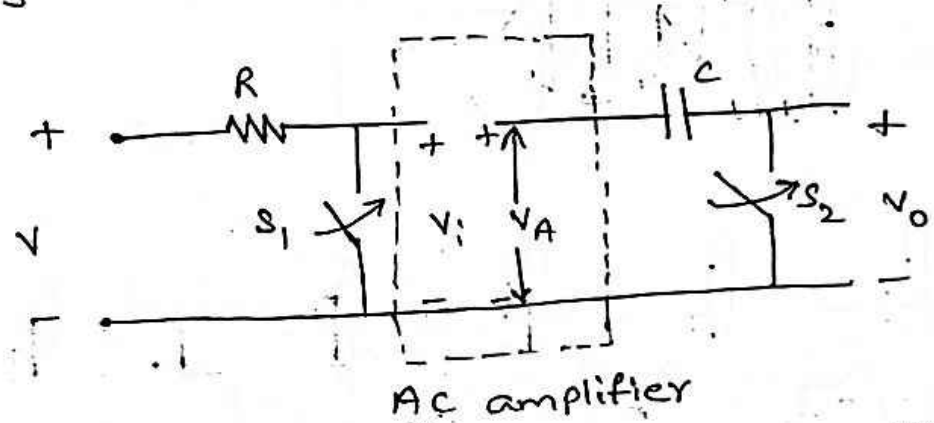
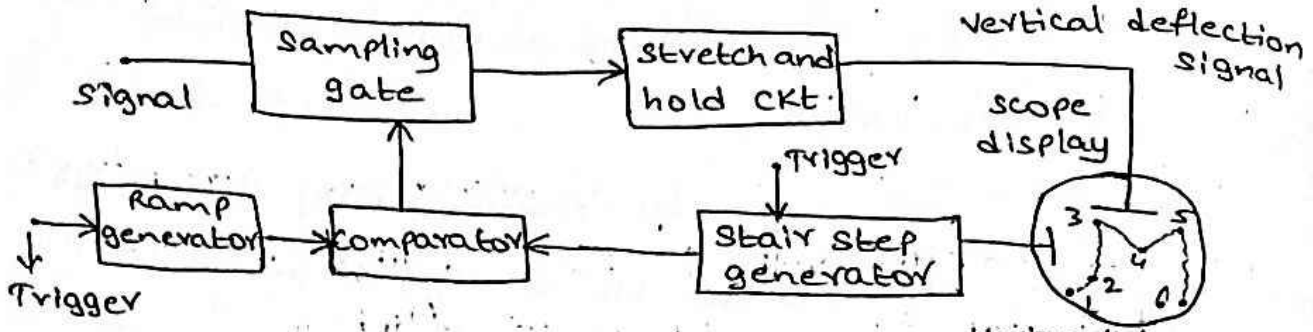
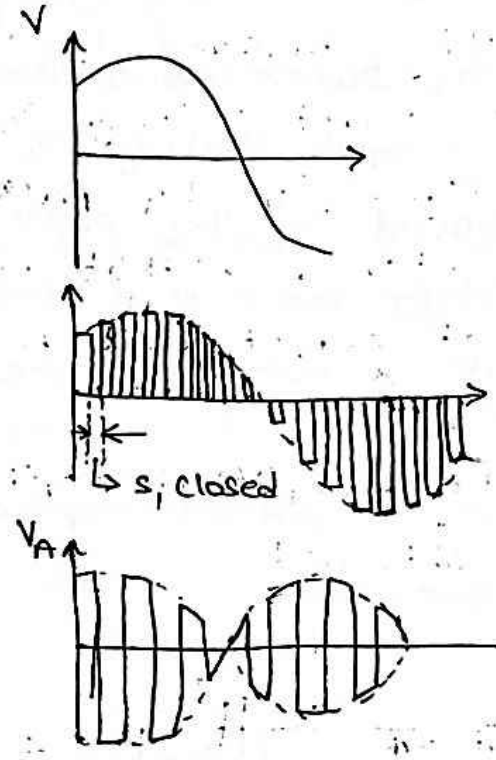
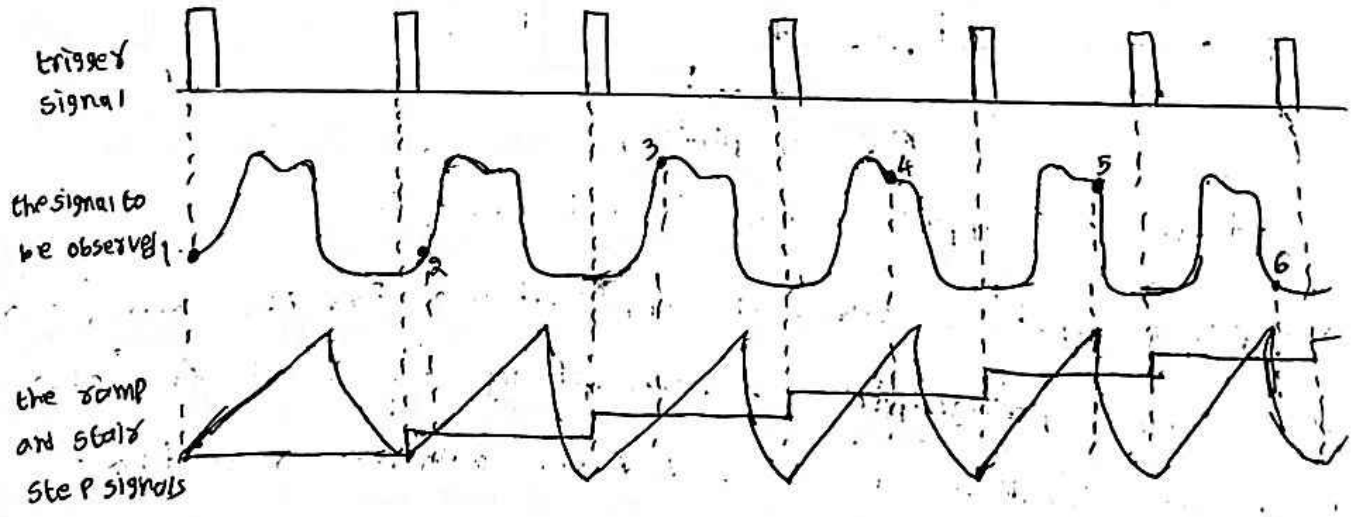


fig.: chopper stabilized amplifier.

* Sampling gates useful applications in the sampling scopes. The principle of sampling is used for the display of continuous waveform whose rise time may vary in nano seconds. It also eliminates the needless usage of wide band amplifiers with high gain.


Signal
Sampling gate
Stretch and hold CKT
Vertical deflection signal
scope display
Trigger
Ramp generator
Comparator
Stair step generator
Trigger
1
2
3
4
5
6
Horizontal deflection signal


V
S1 closed
VA


trigger signal
the signal to be observed
the ramp and stair step signals
1
2
3
4
5
6

Previous Questions

1) Compare unidirectional & bidirectional sampling gate.
2) TTL NAND gate
3) Draw & explain the CKt diagram of +Ve RLT RTL NOR gate.
4) Comparison b/w RTL and DTL incase of fanout, noise immunity, Propagation delay.
5) What are the other names of gate signals.
6) Applications of logic gates
7) What are the basic logic gates.

Reduction of Pedestal in a gate circuit:-

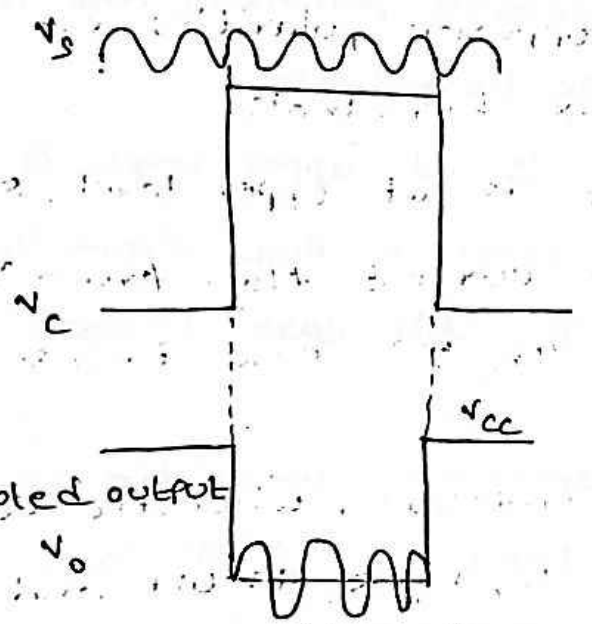


fig.: Pedestal associated with the sampling gate.

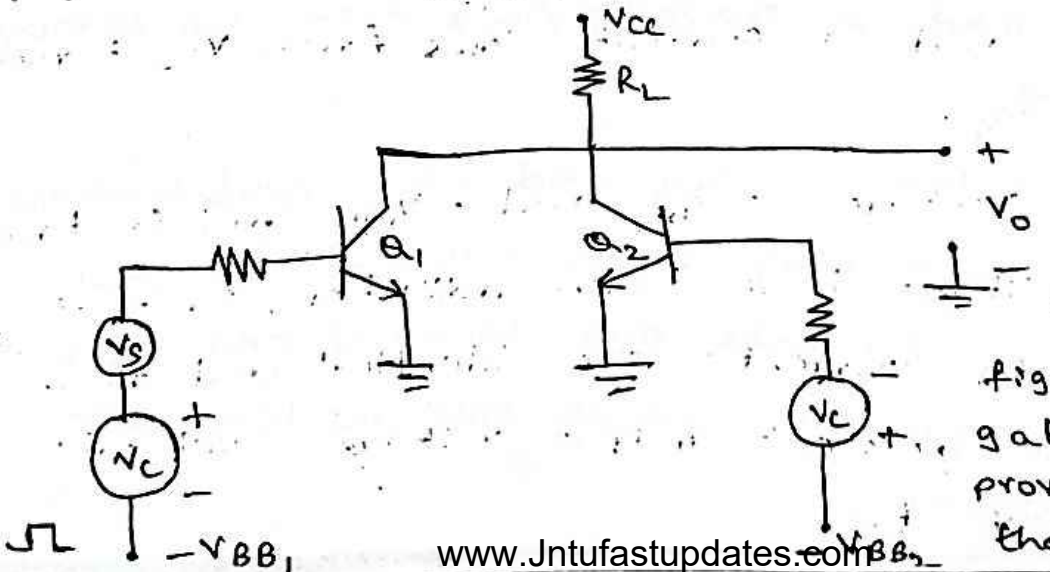
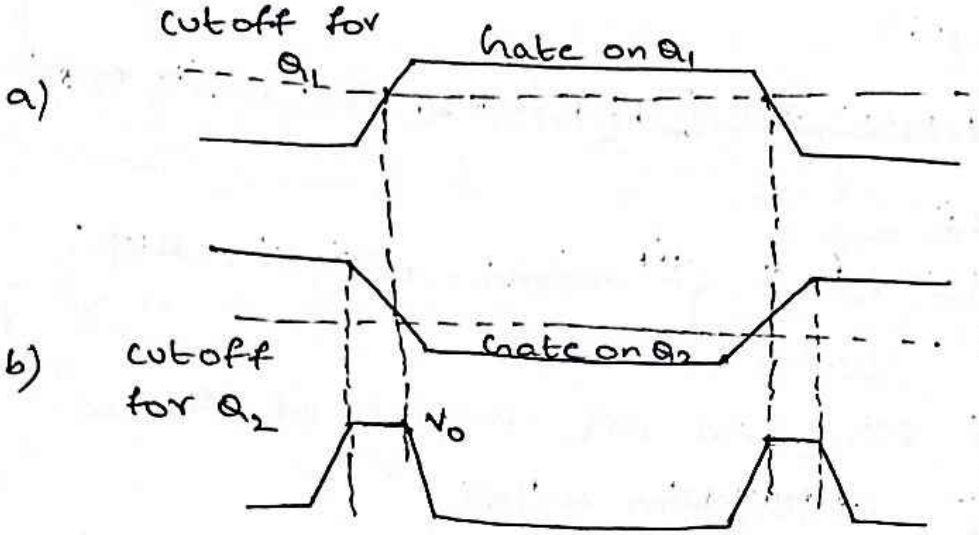


fig.: A sampling gate with provision to cancel the pedestal.



Above Ckt is a symmetrical arrangement that Supprcssess the pedestal to a great extent. 'Q_1' is a gating transistor and 'Q_2' is used to minimise the pedestal.

Control voltages of opposite polarities are applied to the transistor base terminals.

When Control voltage is at upper level, Q_1 Conducts and Q_2 Cut off, a current flow from V_{cc} through R_c and Q_1. In this case transmission is going.

During the non-transmission, when the control voltage is at lower level Q_1 is off and Q_2 Conducts, and a current flows from V_{cc} through R_c and Q_2.

The base voltages $-V_{BB_1}$ and $-V_{BB_2}$ and control signal amplitude have been adjusted, so that two transistor currents are identical and as a result, the quiscent output voltage level will remain Constant.

Drawbacks!-

There is a continuous flow of current through R_C and so it has to dissipate a lot of heat.

The circuit is complicated, it requires two bias voltages i.e., $-V_{BB_1}$ and $-V_{BB_2}$ and two control voltage sources which are complements of each other.

If the gate waveforms having definite rise time and fall times, two sharp spikes are generated at the output.