Digital Logic Families & Interfacing

Introduction: Now a days digital integrated circuits are most commonly used in the modern digital systems.

The most commonly IC logic families such as CMOS, bipolar, TTL (Transistor - Transistor Logic) & ECL (Emitter Coupled logic).

These logic families differ in the main components that they use in their circuitry.

Bipolar use diode whereas TTL & ECL use bipolar transistors.

The MOS & CMOS use unipolar MOSFET transistors

- Because the use of different principle component their electrical behavior are different.

In this chapter we will study the important characteristics, electrical behaviour of CMOS family.

CMOS Logic:

The basic building blocks in CMOS logic circuits are MOS transistors.

CMOS Logic Levels:

The CMOS ckt may interpret any voltage in the range 0 – 1.5V as a logic 0, & the range 3.5V – 5.0V as a logic 1.

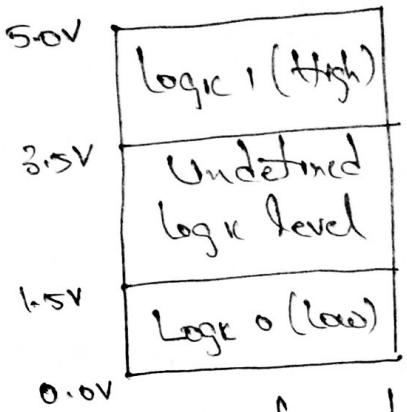


fig: logic levels for typical CMOS logic circuits.

The voltage in between 1.5V to 3.5V are not expected, if they occur, the ckt may interpret them as either 0 or 1.

MOS Transistors:

A MOS transistor is a three terminal device that acts as like a voltage controlled resistance.

An input voltage applied to one terminal controls the resistance between the remaining two terminals.

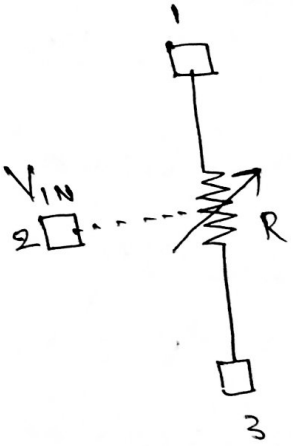


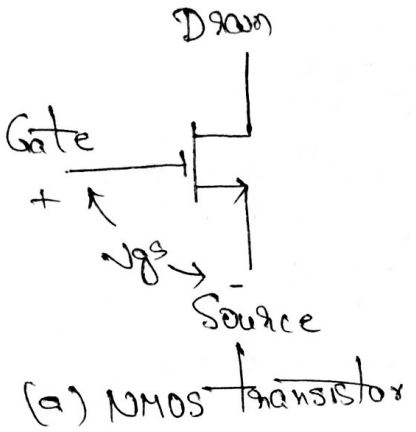
fig: MOS transistor as a voltage controlled resistance.

In CMOS logic circuits, MOS transistor is operated so that its resistance is always either very high or very low.

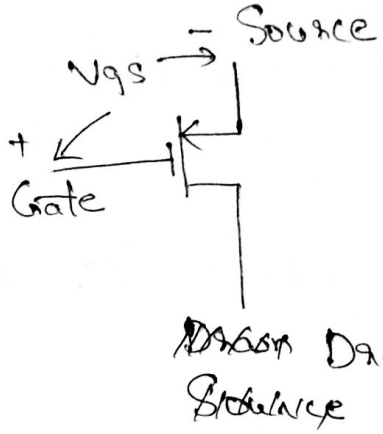
There are two types of MOS transistors:

n-channel (NMOS)

p-channel (PMOS).



(a) NMOS transistor



(b) PMOS transistor

In NMOS transistor, if the gate to source voltage $V_{gs} = 0$ then the resistance drain to source R_{ds} is very high. If V_{gs} is enough positive voltage then R_{ds} is very low.

$V_{gs} = 0 \Rightarrow R_{ds}$ = Very high (few Mega ohms).

V_{gs} = +ve $\Rightarrow R_{ds}$ = Very low (0 – 10 ohms).

In PMOS transistor, if the gate to source voltage $V_{gs} = 0$ then the resistance drain to source R_{ds} is very high. If V_{gs} is enough -ve voltage then R_{ds} is very low.

$V_{gs} = 0 \Rightarrow R_{ds} =$ Very high (few Mega ohms)

$V_{gs} =$ -ve $\Rightarrow R_{ds} =$ Very low (0 - 10 ohms)

The NMOS & PMOS transistors are used together in a complementary way to form CMOS logic. (complementary Metal Oxide Semiconductor).

Let us see the basic circuits for CMOS inverter, NAND & NOR gates.

Basic CMOS Inverter Circuit:

It consists of two MOSFET'S in series. The P- channel device has its source connected to $+V_{DD}$ & the N- channel device has its source connected to ground.

The gates of the two devices are connected together as the common input & the drains are connected together as the common output.

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Case 1:

When input is HIGH:

Q_1 = OFF

Q_2 = ON

∴ output = logic 0

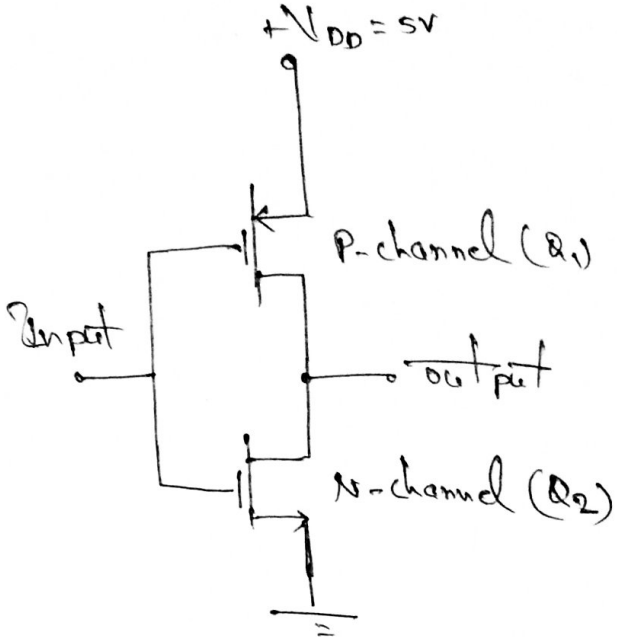


fig: CMOS inverter ckt

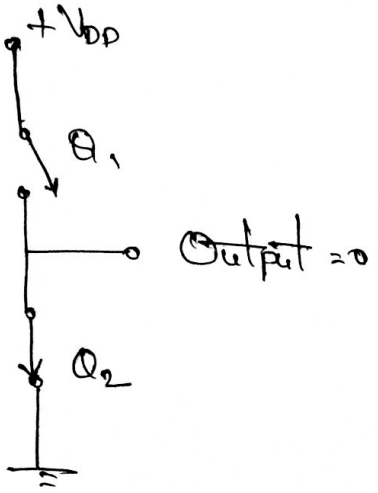
Case 2:

When input is LOW:

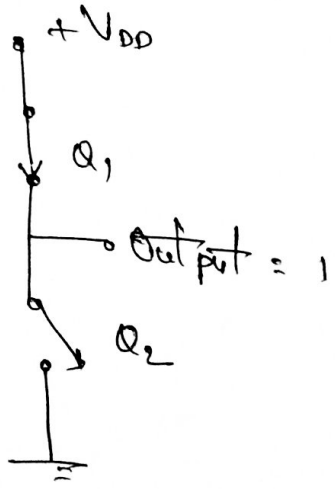
Q_1 = ON

Q_2 = OFF

∴ output = logic 1



(a) Input = 1



(b) Input = 0

CMOS Inverter truth table:

Input	Q_1	Q_2	output
0	ON	OFF	1
1	OFF	ON	0

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CMOS NAND GATE:

2-Input NAND gate:

→ It consists of two p-channel MOSFETs, Q_1 & Q_2, connected in parallel & two N-channel MOSFETs, Q_3 & Q_4 connected in series.

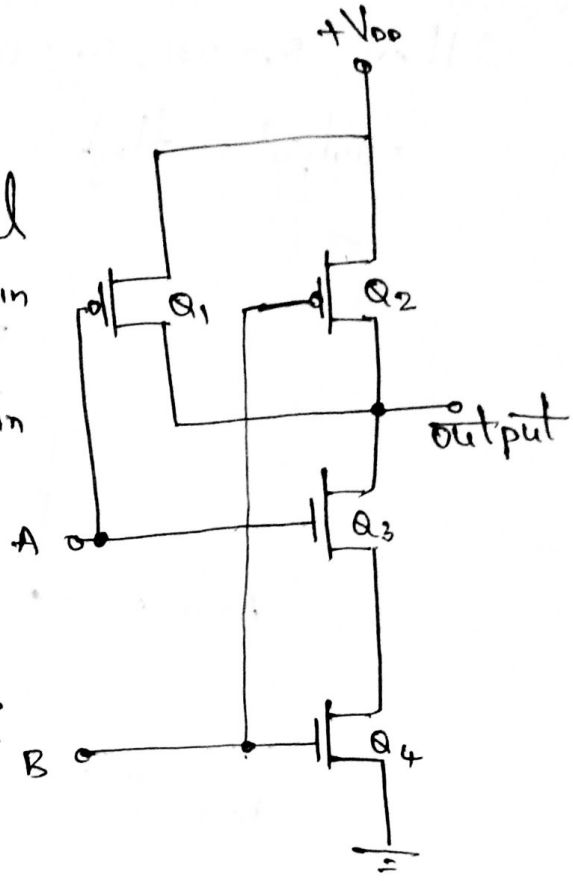


fig: 2-Input NAND gate

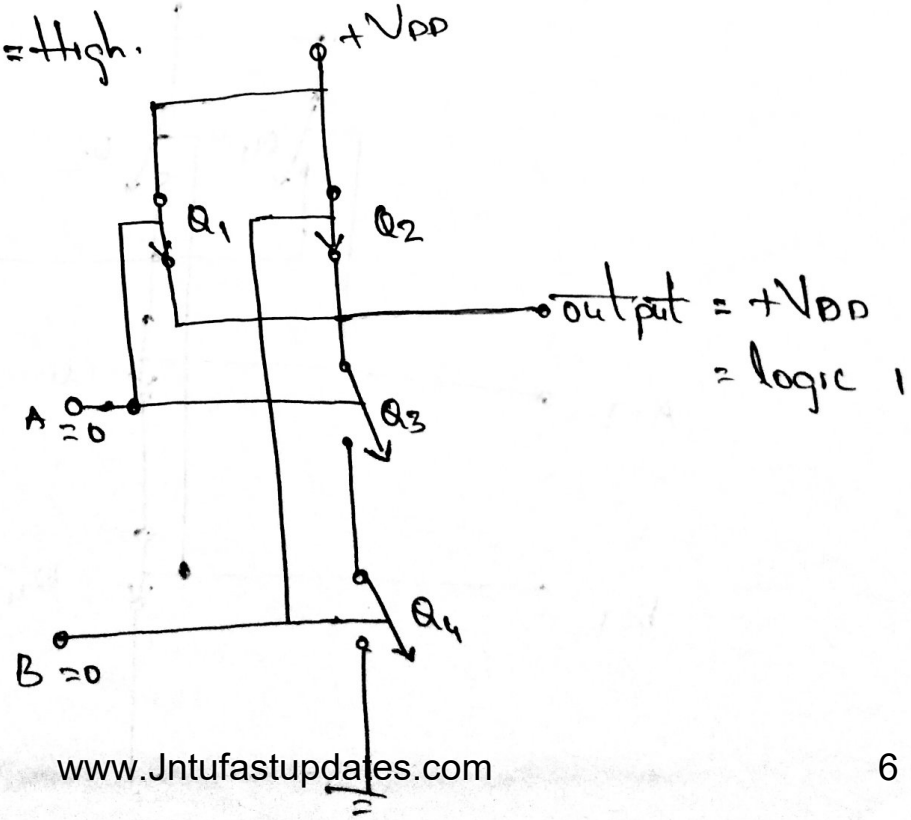
Truth table:

A	B	Q_1	Q_2	Q_3	Q_4	O/P
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

Case 1: If A=0, B=0;

Then Q_1=ON, Q_2=ON, Q_3=OFF, Q_4=OFF

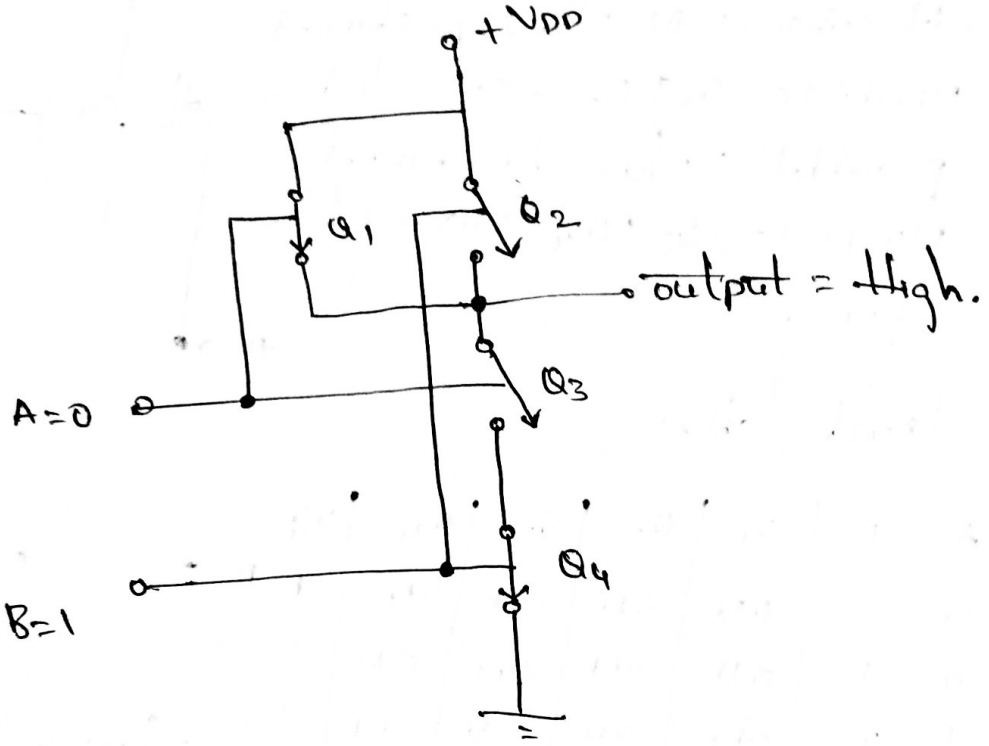
∴ output = High.



Case 2: If A = 0, B = 1

Then Q_1 = ON, Q_2 = OFF, Q_3 = OFF, Q_4 = ON

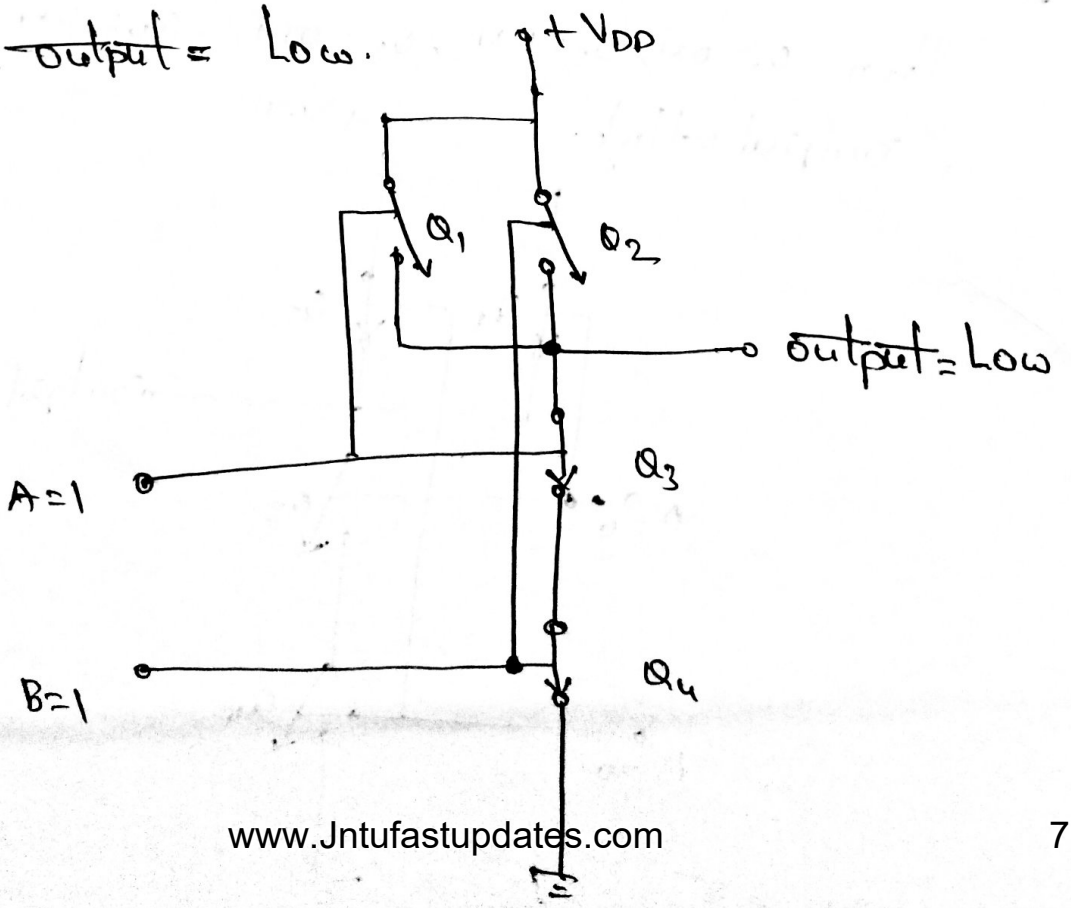
∴ output = High.



Case 3: If A = 1, B = 1

Then Q_1 = OFF, Q_2 = OFF, Q_3 = ON, Q_4 = ON.

∴ output = Low.



CMOS NOR Gate:

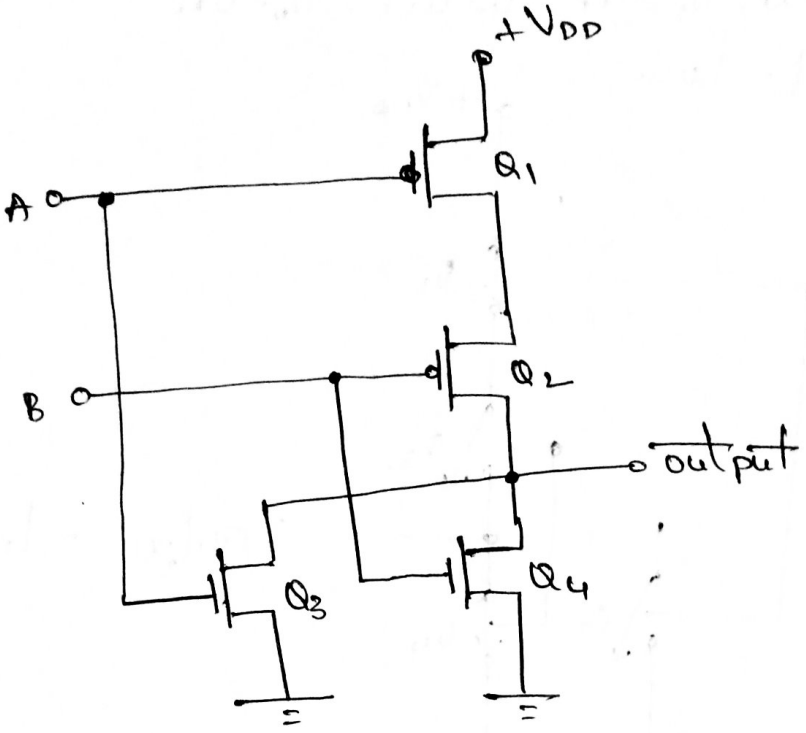
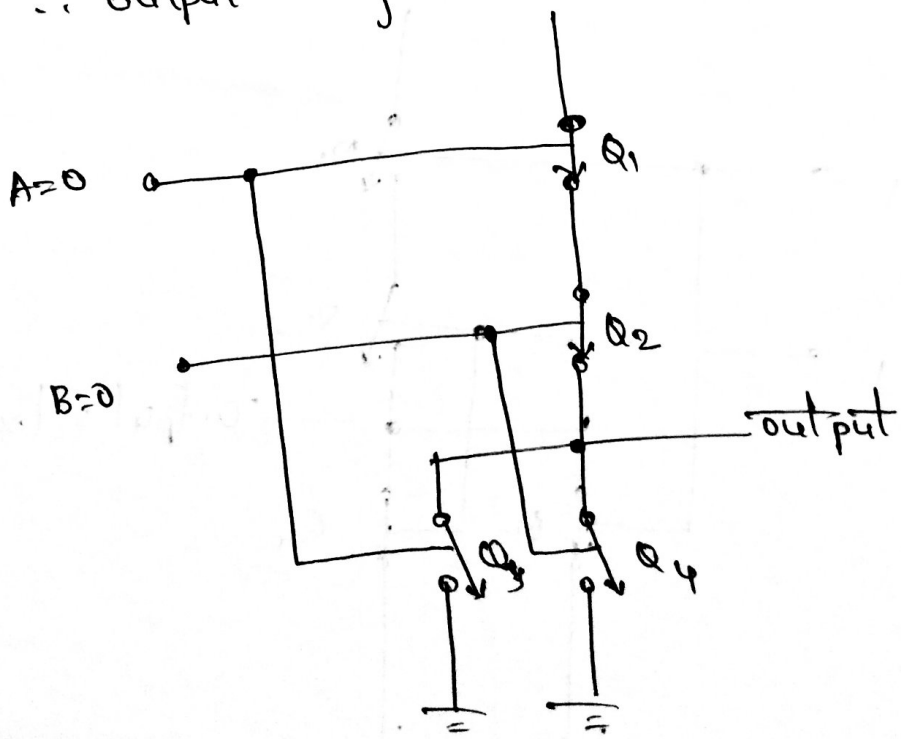


fig: 2-Input NOR Gate

Case 1: If A=0, B=0

Then Q_1=ON, Q_2=ON, Q_3= OFF, Q_4= OFF

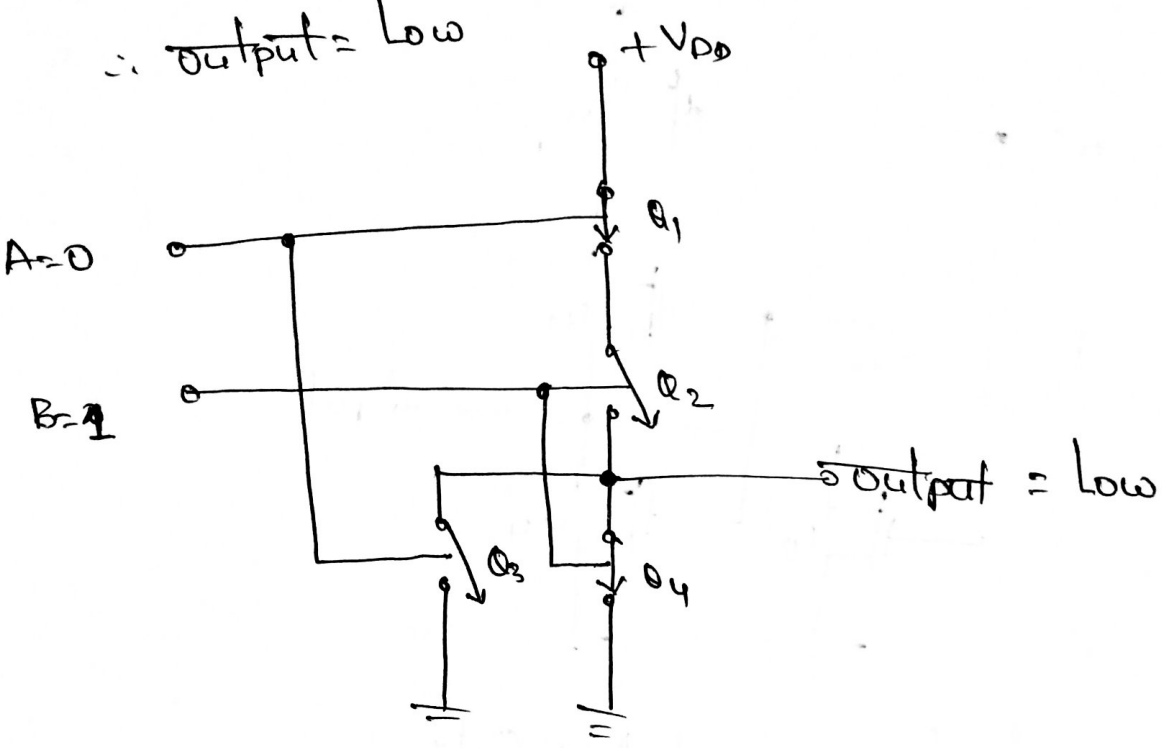
∴ output = High.



Case 2: If A=0, B=1

Then Q_1=ON, Q_2=OFF, Q_3=OFF, Q_4=ON

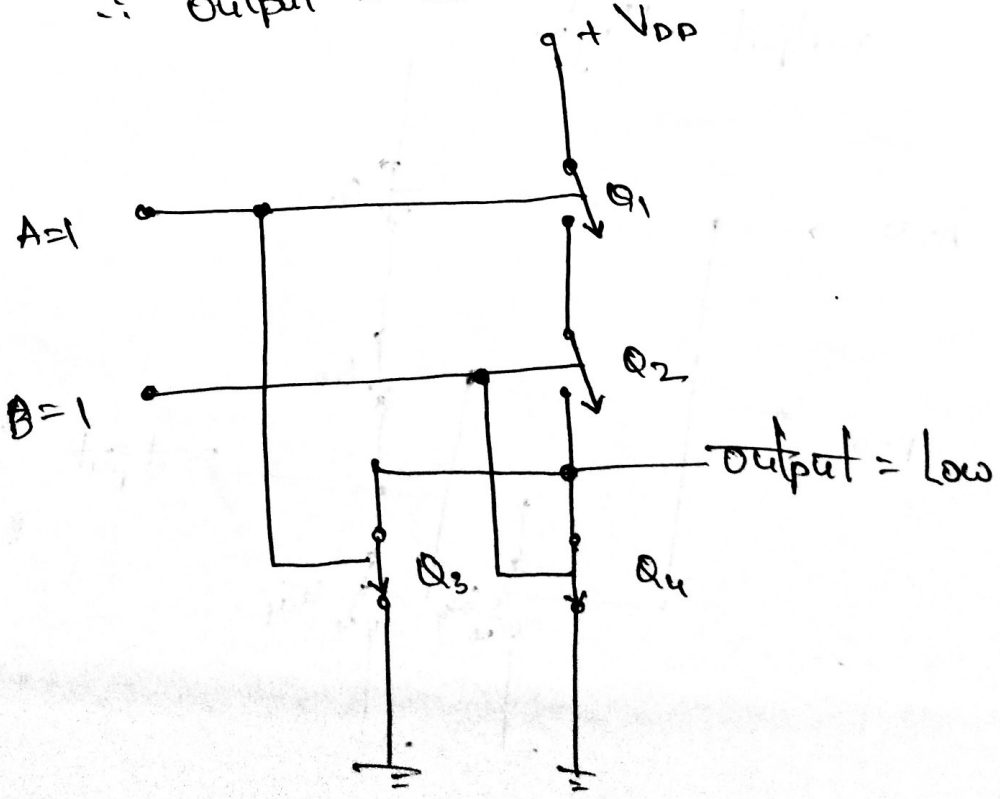
∴ output = Low



Case 3: If A=1, B=1

Then Q_1=OFF, Q_2=OFF, Q_3=ON, Q_4=ON

∴ output = Low



Electrical Behaviour of CMOS Circuits:

The electrical behaviour of CMOS circuits include (a) steady-state electrical behaviour & (b) Dynamic electrical behaviour of CMOS circuits.

(a) CMOS steady-state Electrical Behaviour

The steady-state behaviour is the behaviour of the ckt when the inputs & outputs are not changing.

Logic Levels & Noise Margin:

The CMOS device manufacturers specify the four voltage parameters.

These are:

(i) $V_{IH(min)}$ – High-Level Input Voltage:

It is the min. voltage level required for a logic 1 at an input. Any voltage below this level will not be accepted as a HIGH by the logic ckt.

(ii) $V_{IL(max)}$ – Low-Level Input Voltage:

It is the max. voltage level required for a logic 0 at an input. Any voltage above this level will not be accepted as a LOW by the logic ckt.

(iii) $V_{OH(min)}$ – High-Level Output Voltage:

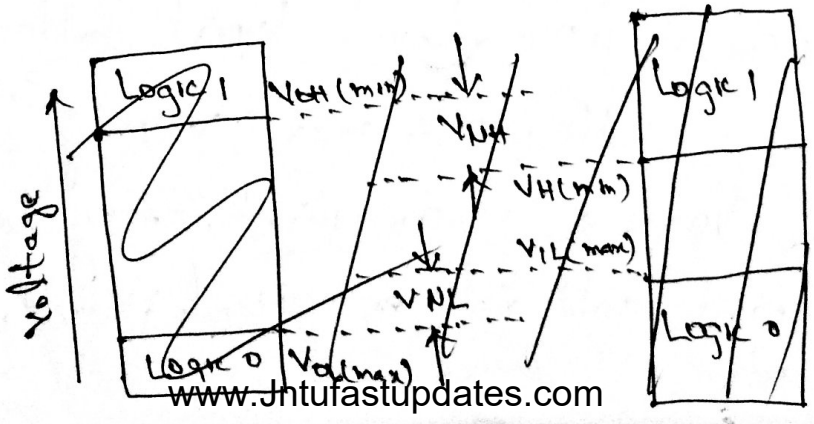
It is the min voltage level at a logic ckt output in the logic 1 state under defined load conditions.

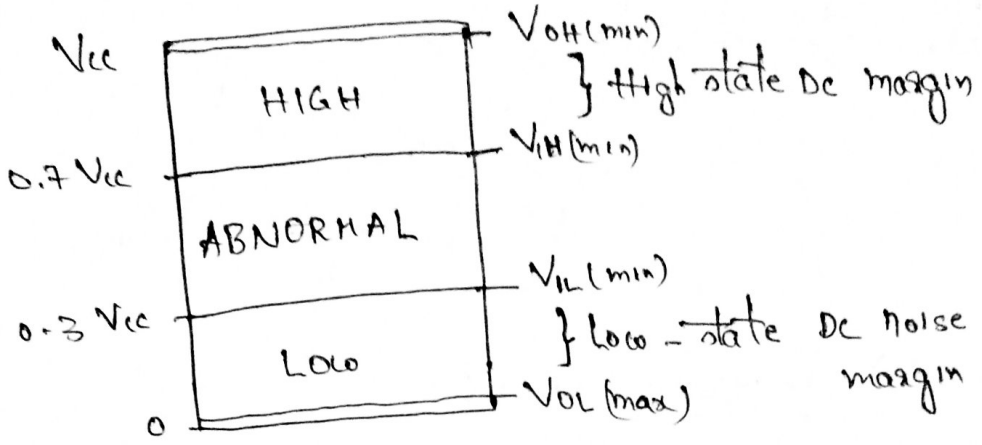
(iv) $V_{OL(max)}$ – Low-Level Output Voltage:

It is the max. voltage level at the a logic ckt output in the logic 0 state under defined load conditions.

In practice, due to the unwanted signal called noise, sometimes the voltage at the input drops below $V_{IH(min)}$ or rise above $V_{IL(max)}$, which produces unpredictable operation.

To avoid this problem due to noise, voltage level $V_{IH(min)}$ is kept a few fraction of volts below $V_{OH(min)}$ and voltage level $V_{IL(min)}$ is kept above $V_{OL(max)}$, at the design time.





Voltage Levels & Noise Margins:

$V_{OH(min)}$: $V_{cc} - 0.1V$ $V_{IH(min)}$: 70% of V_{cc}

$V_{IL(max)}$: 30% of V_{cc} $V_{OL(max)}$: Ground + 0.1V

Fan-IN: The max. number of digital inputs that a single logic gate can accept.

Fan-OUT: The max. number of digital inputs that the output of a single logic gate can feed.

(b) CMOS Dynamic Electrical Behaviour:

The speed & power consumption of CMOS devices are mostly depend on AC or dynamic characteristics of the device & its load.

The AC characteristics refers to the output changes between states.

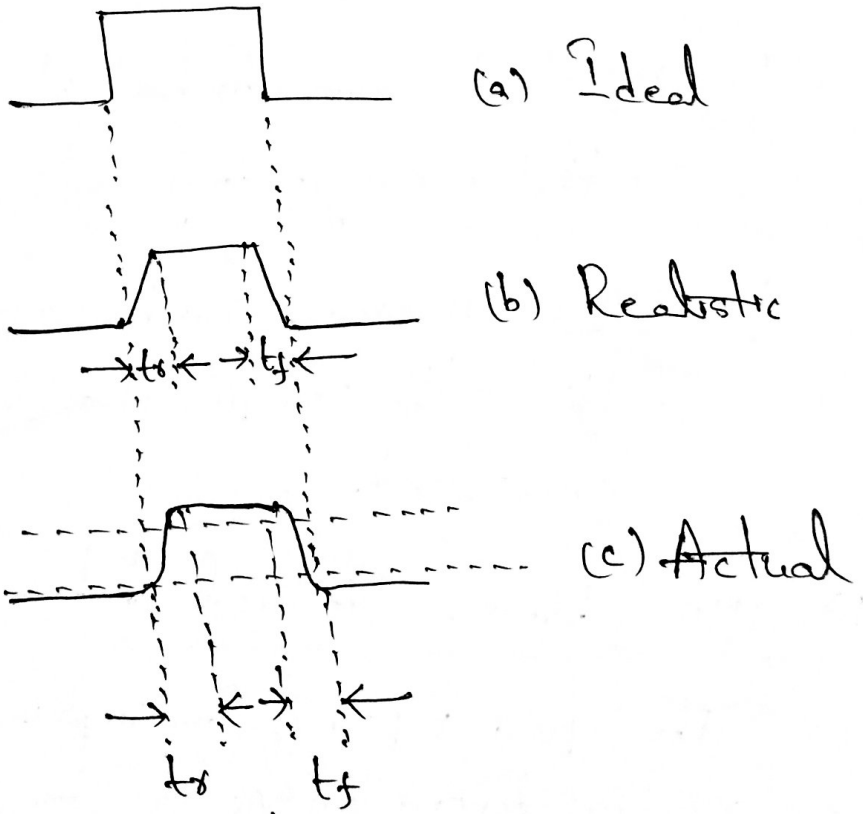
The speed of the CMOS device depends on two characteristics:

(a) Transition time

(b) Propagation delay.

(a) Transition Time:

The amount of time that the output of a logic ckt takes to change from one state to another is called the transition time.



In practice, the outputs cannot change instantaneously, because they need time to charge the stray capacitance.

The stray capacitance is also called a capacitive load or any AC load of the logic ckt.

Rise time (t_r): It is the time taken by the output to change from low to high.

Fall time (t_f): It is the time taken by the output to change from high to low.

The rise time & fall time of a CMOS output depend mainly on two factors; the ON transistor resistance & the load capacitance.

Since increase in load capacitance increases transition time.

However, the stray capacitance is present in every ckt due to the following sources:

→ Output ckts, output transistors, internal wiring & packing have some capacitance associated with them. The capacitance due to them is of the order of 2-10 picofarads (PF).

→ The wiring connections between an o/p & other inputs adds capacitance of the order of 1PF inch or more.

→ Input ckts, including transistors, internal wiring & packaging have capacitance of the order of 2 to 15 PF per input.

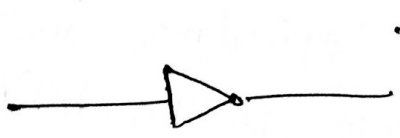
(b) Propagation Delay:

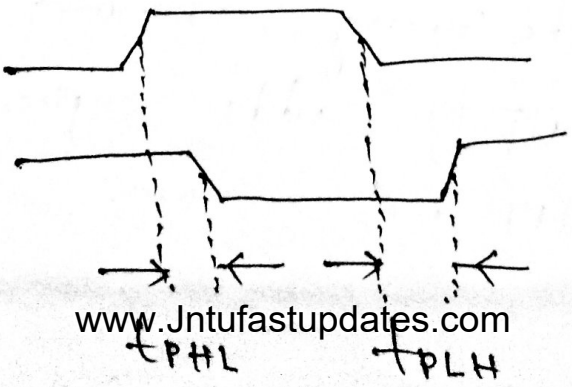
The propagation delay is the amount of time that it takes for a change in the input signal to produce in the output signal.

The shorter propagation delay, the higher the speed of the ckt & Vice-Versa.

The propagation delay is determined using two basic time intervals.

1. t_{PLH}: It is the delay time measured when o/p is changing from logic 0 to logic 1.
2. t_{PHL}: It is the delay time measured when output is changing from logic 1 to logic 0





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CMOS Logic Families:

The commercially available CMOS families are:

* 4000-series CMOS
* 74 series HC (High-speed CMOS)
* 74 series HCT (High-speed CMOS, TTL compatible)
* VHC (Very high speed CMOS)
* VHCT (Very high speed CMOS, TTL compatible).
* FCT (Fast CMOS, TTL compatible)
* FCT-T (Fast CMOS, TTL compatible with V_{OH})

4000-Series CMOS:

→ The first commercially available CMOS family was 4000-series CMOS.

→ Low power consumption; they were fairly slow & were not easy to interface with the most popular logic family, TTL (Transistor-Transistor Logic).

HC and HCT Families: (74 Series)

→ The prefix "74" is simply a number that was used by an early, popular TTL family.

→ CMOS IC are also fabricated in the same way.

→ The first two 74-series CMOS families are HC (High-speed CMOS) and HCT (High-speed CMOS,

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TTL compatible).

→ These families have higher speed, compatibility with TTL family having power-supply voltage same as TTL, +5V.

→ The power-supply voltage range for HC family is 2V to 6V.

→ The higher power-supply voltage is used for higher speed, & a lower voltage is used for lower power dissipation.

VHC and VHCT Families:

→ In 1980s and 1990s two more CMOS families were introduced. These families are

VHC (Very high speed CMOS) &

VHCT (Very high speed CMOS, TTL compatible).

→ These families are about twice as fast as HC/HCT families.

FCT & FCT-T Families:

→ In early 1990s, yet another family called FCT was introduced.

→ The main advantage of this family is to meet or exceed the speed of the output drive

capability of the best TTL families while reducing power consumption & maintaining full compatibility with TTL.

→ However the FCT family has a drawback of producing full 5V CMOS V_{OH}.

→ The family named FCT-T was quickly introduced to reduce the drawback of FCT family.