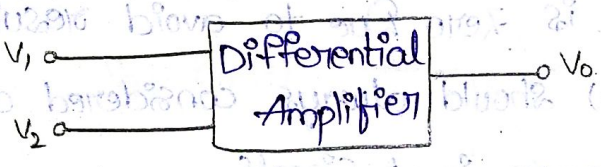
1. Integrated Circuits

Introduction to Differential Amplifier :-

Differential Amplifier is defined as "An amplifier which gives the output of the difference b/w the two different inputs. Such amplifier is called as Differential Amplifier i.e; $V_o = V_1 - V_2$

Basics of Differential Amplifier :-



For a differential amplifier basically there are three properties.

1. Differential Voltage gain (A_d)
2. Common Mode Voltage gain (A_c)
3. Common Mode Rejection Ratio (CMRR)

1. Differential Voltage gain (A_d) :-

Basically the differential amplifier output V_o is directly propotional to the difference b/w the two input signals i.e;

$$V_o \propto (V_1 - V_2) \quad \text{——} (1)$$

By using above equation

$$V_o = A_d (V_1 - V_2)$$

$$V_o = A_d \cdot V_d \qquad (\because V_d = V_1 - V_2)$$

$$\therefore \boxed{A_d = \frac{V_o}{V_d}} \quad \text{——} (2)$$

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Practically the differential voltage gain (A_d) is always considered as a larger value and it is expressed in decibels.

2. Common Mode gain (A_c):-

By using eq①,

$$V_o = A_c (V_1 - V_2)$$

$$V_o = A_c \cdot V_c$$

But when the common signals are applied to the differential amplifier, voltage is zero. Due to avoid result, the common mode voltage (V_c) should always considered as the Average value of the common input signals.

$$\text{i.e; } V_c = \frac{V_1 + V_2}{2}$$

3. Common Mode Rejection Ratio

When the same input signals are applied to the differential amplifier, it should be operated in a common mode configuration. Many disturbance signals, noise signals appears as a common input signals to both input terminals of a differential amplifier. Such a common signal should be rejected by the Differential Amplifier.

The ability of a differential amplifier to reject a common mode signal is expressed by the ratio is called Common Mode Rejection Ratio (CMRR). It is also defined as the ratio of differential voltage gain (A_d) to common mode voltage gain (A_c) i.e;

$$\boxed{CMRR(\rho) = \frac{A_d}{A_c}}$$

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Practically the differential amplifiers whose differential voltage gain (A_d) is large and Common Mode gain (A_c) is small. Hence the value of CMRR is also large value.

The CMRR is expressed in decibels is

$$\boxed{CMRR\ (\text{in dB's}) = 20 \log\left(\frac{A_d}{A_c}\right)}$$

The relation blw the output voltage (V_o) and CMRR can be expressed by using

$$V_o = A_d V_d + A_c V_c \quad \text{——} (3)$$

$$V_o = A_d V_d \left(1 + \frac{A_c}{A_d} \cdot \frac{V_c}{V_d}\right)$$

$$V_o = A_d V_d \left(1 + \frac{1}{\left(\frac{A_d}{A_c}\right)} \cdot \frac{V_c}{V_d}\right)$$

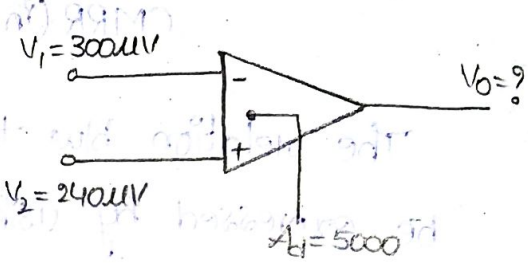
$$V_o = A_d \cdot V_d \left(1 + \frac{1}{CMRR} \cdot \frac{V_c}{V_d}\right) \quad \left(\because CMRR = \frac{A_d}{A_c}\right)$$

Features of Differential Amplifier :-

1. High differential Voltage gain (A_d) (↑)
2. Low Common mode Voltage gain (A_c) (↓)
3. High CMRR (↑) which is ∞
4. For a differential Amplifier, it should consists of two input terminals.
5. It should consists of high input Impedance (Z_i).
6. It should consists of low output Impedance (Z_o).
7. Bandwidth should always large.
8. It should consists of low offset (Null) voltages and currents.

Problem:-

① Determine the output voltage of a differential amplifier for the input voltages 300μV and 240μV. The differential gain of the amplifier is 5000 and the value of CMRR is (i) 100 (ii) 10^5.



Given V_1=300μV

V_2=240μV

Differential gain (A_d) = 5000

W.K.T $V_0 = A_d V_d + A_c V_c$

$V_d = V_1 - V_2 = 300 - 240 = 60\mu V$

$V_c = \frac{V_1 + V_2}{2} = 270\mu V$

Case 1:- CMRR = 100

$CMRR = \frac{A_d}{A_c}$

$100 = \frac{5000}{A_c} \Rightarrow A_c = 50$

$V_0 = A_d V_d + A_c V_c$

$= 5000(60) + 50(270)$

$= 3000000\mu V + 13500\mu V$

$= 313500\mu V$

$= 313.5mV$

$1\mu V = 10^{-6} V$

Case 2:- $CMRR = 10^5$

$CMRR = \frac{A_d}{A_c} \Rightarrow 10^5 = \frac{5000}{A_c} \Rightarrow A_c = 0.05$

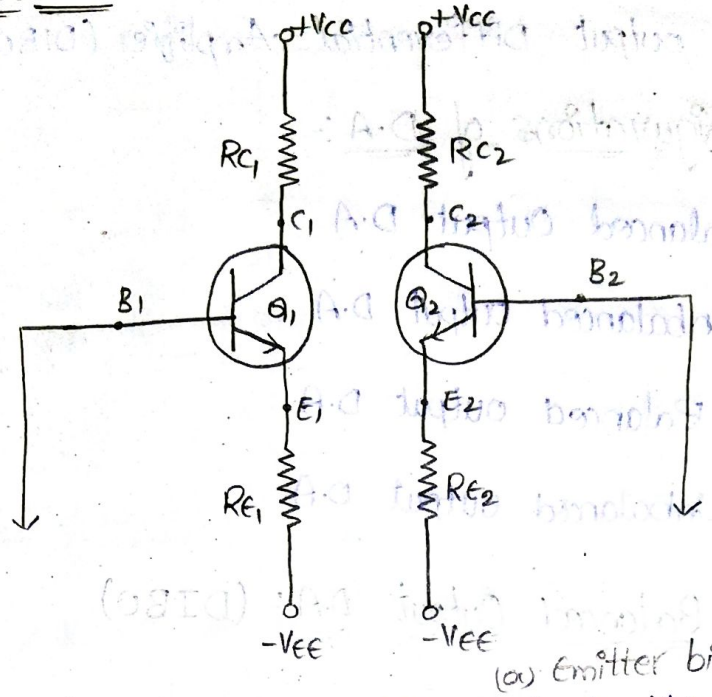
$V_0 = A_d V_d + A_c V_c$

$= 5000(60) + 0.05(270)$

$= 3,00,000\mu V + 13.5\mu V$

$= 300mV$

Transistorised Differential Amplifier :



(a) Emitter biased circuits

The transistorised Differential Amplifier basically uses emitter biased circuit which are identical in properties. The two transistors Q_1 and Q_2 have exactly matched characteristics.

From the fig. the two collector resistances R_{C_1} and R_{C_2} are equal while the two emitter resistances R_{E_1} and R_{E_2} are also equal i.e; $R_{C_1} = R_{C_2}$ and $R_{E_1} = R_{E_2}$.

The magnitude of $+V_{CC}$ and $-V_{EE}$ are also same i.e;

$|+V_{CC}| = |-V_{EE}| = 12V$.

The differential amplifier can be obtained by using two emitter biased circuits which is achieved by collecting emitter E_1 of Q_1 to emitter E_2 of Q_2. Due to this R_{E_1} in parallel with R_{E_2} then the combination can be replace by a single resistance R_E. Similarly the base B_1 of Q_1 is connected to input 1 which is V_{S_1}, while the base B_2 of Q_2 is connected to input 2 which is V_{S_2}. The supply voltages are measured w.r.t ground. The balanced o/p is taken b/w the collector C_1 of Q_1 and the collector C_2 of Q_2 such as designed Amplifier is

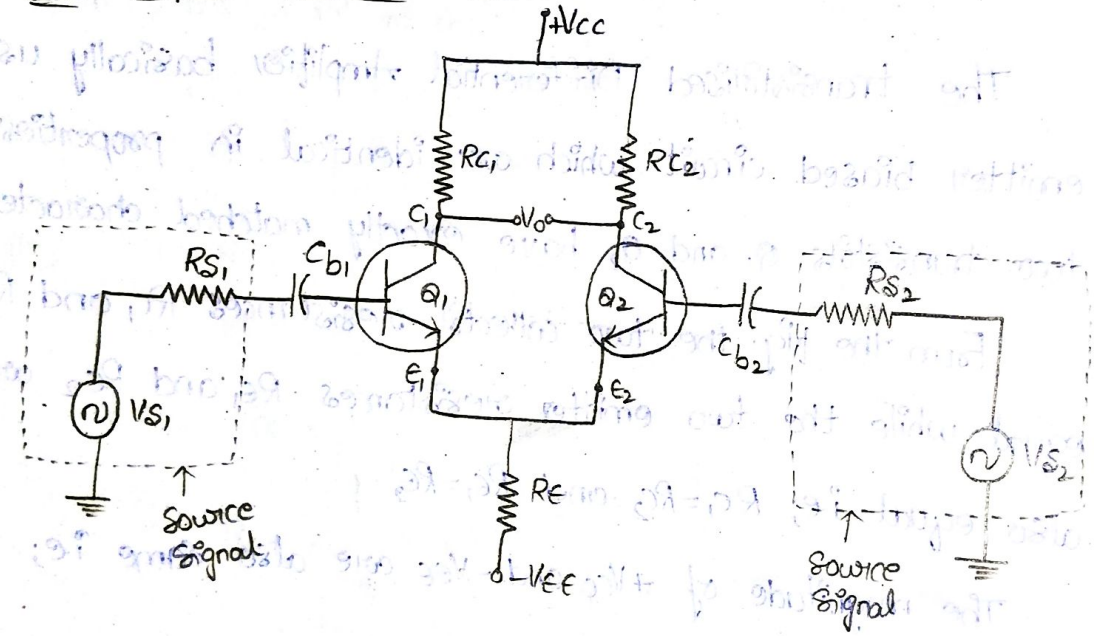
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Called as Emitter Coupled Differential Amplifier (or) Dual input Balanced output Differential Amplifier (DIBO).

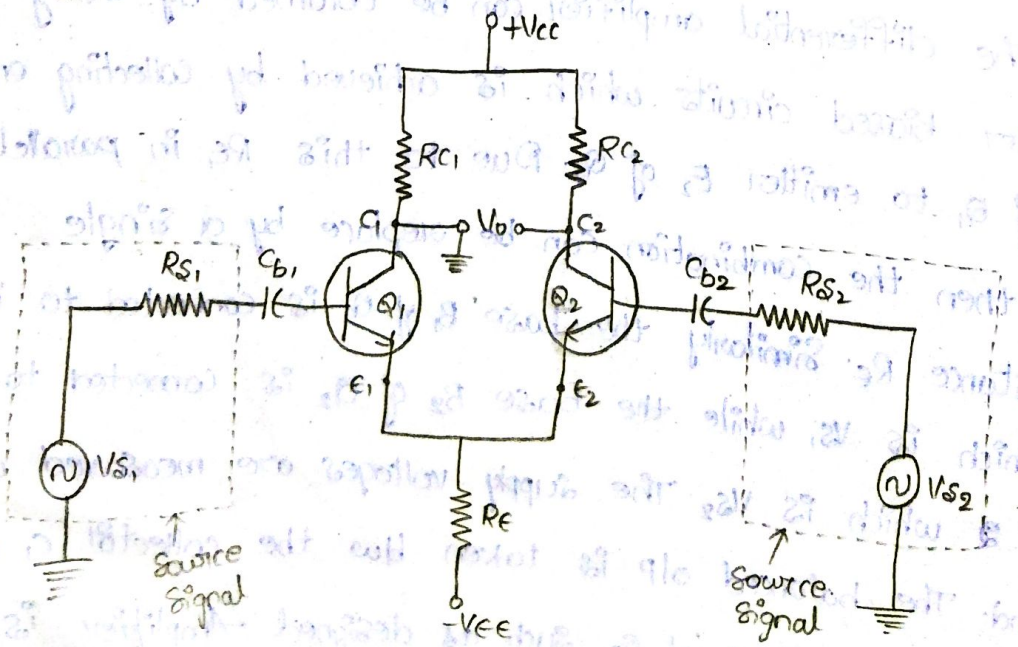
Types of Configurations of D.A :-

1. Dual input Balanced Output D.A
2. Dual input Unbalanced output D.A
3. Single input Balanced output D.A
4. Single input Unbalanced output D.A

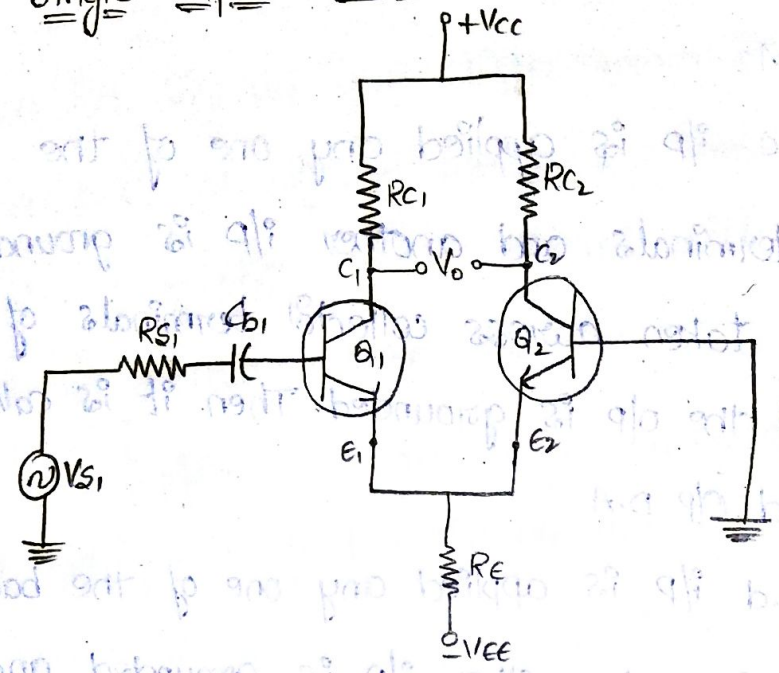
1. Dual input Balanced Output D.A :- (DIBO)



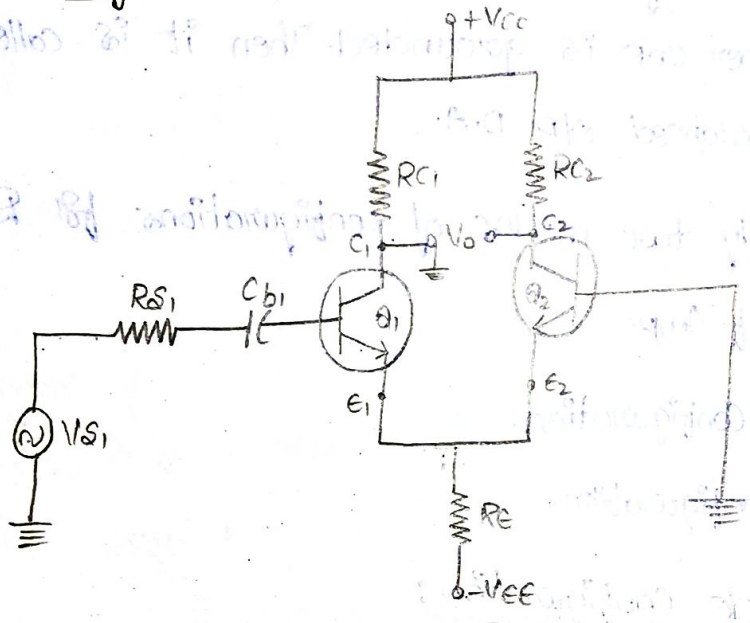
2. Dual input Unbalanced Output D.A :-



3. Single input Balanced Output D.A:-



4. Single input Unbalanced output D.A:-



19/6/18. From fig(a), when the two input signals are applied to the base terminals and the output is taken across the collectors of both transistors none of the output is grounded. Then it is called as Dual input Balanced output D.A.

From fig(b), two input signals are applied from the base terminals and the outputs is taken across the collector terminals of both transistors and any one of the

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output is grounded. Then it is called as Dual input unbalanced o/p D-A.

From fig.c i/p is applied any one of the transistor base terminals and another i/p is grounded and also o/p is taken across collector terminals of both transistors none of the o/p is grounded. Then it is called as Single i/p Balanced o/p D.A.

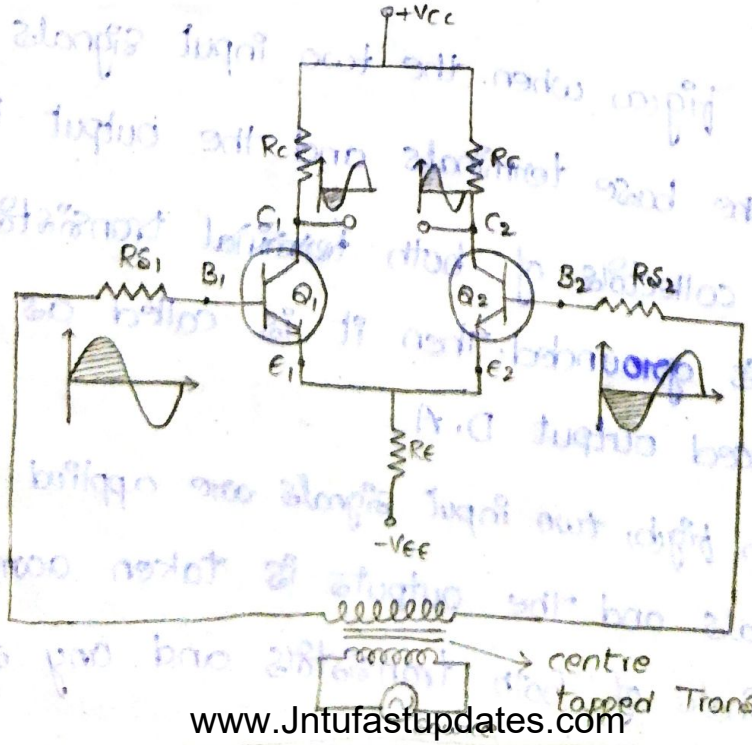
From fig.d i/p is applied any one of the base terminal of transistor and another i/p is grounded and also o/p is taken any one of the collector terminals of both transistors and another one is grounded. Then it is called as Single i/p Unbalanced o/p D.A.

Let us study two modes of configurations for Dual i/p Balanced o/p diff Amp.

(i) Differential Mode Configuration.

(ii) Common Mode Configuration.

(i) Differential Mode Configuration:-



In the differential mode configuration the two i/p signals are differ from each other. Consider the two i/p signals which are same in magnitude but 180° out of phase these signals with opposite phase can be obtained from the centre tapped transformer.

Assume that the sinewave on the base of Q_1 is +ve going signal while on the base of Q_2 is -ve going signal with a +ve going signal on the base of Q_1 an amplify -ve going signal develops on the collector of Q_1 due to this +ve going signal the current through the resistor R_E is also increases and hence +ve going signal develops across R_E.

Similarly due to the -ve going signal on the base of Q_2 an amplified +ve going signal develops on the collector of Q_2 and a -ve going signal develops across R_E because of emitter follower action.

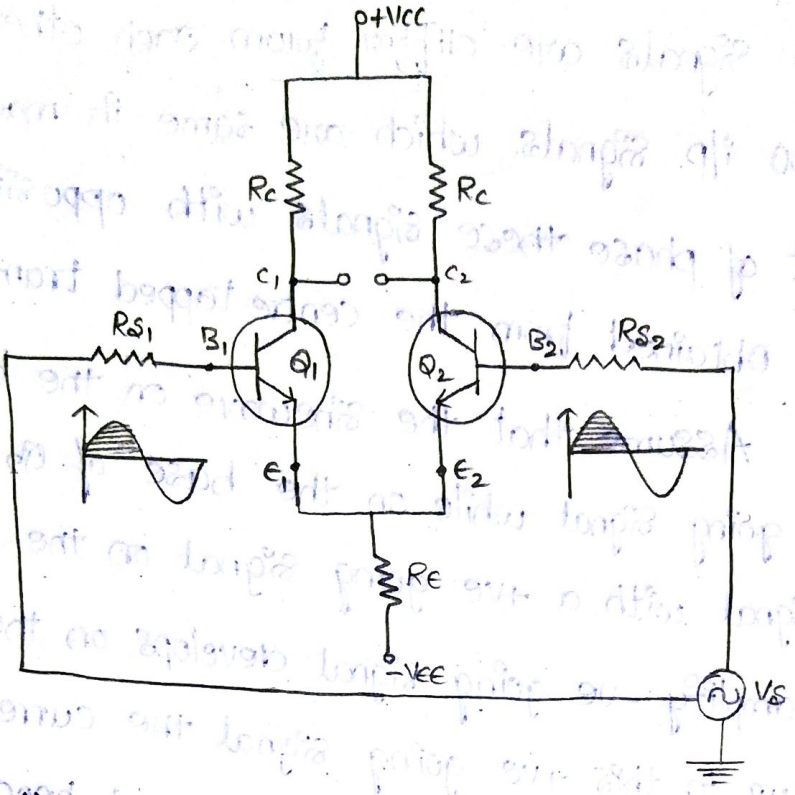
So, the signal voltage across R_E due to the effect of Q_1 and Q_2 are equal in magnitude and 180° out of phase with match pair transistor. Hence the two signals cancel with each other and there is no signal across R_E due to this effect the emitting resistance doesn't introduce a -ve feedback.

The final o/p V_o is taken across the collector of both terminals with opposite polarity but equal in magnitude

i.e; $V_o = (+10) - (-10)$

$= 20V.$

(ii) Common Mode Configuration:-



In this common Mode configuration the signals are applied to the basis of Q_1 and Q_2 are derived from same source. So the two signals are equal in magnitude as well as in phase also.

In phase signal voltages at the bases of Q_1 and Q_2 causes in phase signal voltages to appears across R_E resistance which are added together. Hence emitting resistance R_E carries a signal current and provides a -ve feedback. This feedback reduces the common mode gain of a D.A. For this configuration the o/p voltage is taken across the collector terminals of both transistors whose o/p voltage is $V_o = 10 - 10$

$= 0$

Thus the difference o/p V_o is almost zero and negligibly small. This is why we have to consider the averages of input signals.

Problem

② Determine the o/p voltage of a D.A with the i/p voltages of 20V and 30V. The differential gain of the amplifier is 1000 and the value of CMRR is
(i) 10^3 (ii) 10^6 (iii) 10^9

Sol:- Given $V_1 = 20V$.
$V_2 = 30V$.

Differential gain $(A_d) = 1000$

W.K.T $V_d = A_d V_d + A_c V_c$

$V_d = V_2 - V_1 = 30 - 20 = 10V$

$V_c = \frac{V_1 + V_2}{2} = \frac{30+20}{2} = 25V$.

Case(1):- CMRR = 1000

$CMRR = \frac{A_d}{A_c}$

$1000 = \frac{1000}{A_c} \Rightarrow A_c = 1$.

$V_o = A_d V_d + A_c V_c$.

$= 1000(10) + 1(25)$.

$= 10,000 + 25$

$= 10,025V$.

Case(2):- $CMRR = 10^6$.

$CMRR = \frac{A_d}{A_c}$

$10^6 = \frac{1000}{A_c} \Rightarrow A_c = \frac{1}{1000}$

$V_o = A_d V_d + A_c V_c$.

$= 1000(10) + \frac{1}{1000}(25)$

$= 10000 + 25000$.

$= 35,000V$.

$= 10000.025V$

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case(iii): CMRR = 10^9.

$$CMRR = \frac{A_d}{A_c}$$

$$10^9 = \frac{1000}{A_c} \Rightarrow A_c = 1/10^6.$$

$$V_o = A_d V_d + A_c V_c.$$

$$= 1000(10) + \frac{1}{10^6}(25).$$

$$= 10000.000025 V.$$

(3) Determine the CMRR if the differential voltage gain is 500 ~~decibels~~ and the common mode voltage gain is 300.

Sol:- Given data is

$A_d = 500.$

$A_c = 300.$

$$A_d = 20 \log(500)$$

$$= 53.97.$$

$$A_c = 20 \log(300)$$

$$= 49.54$$

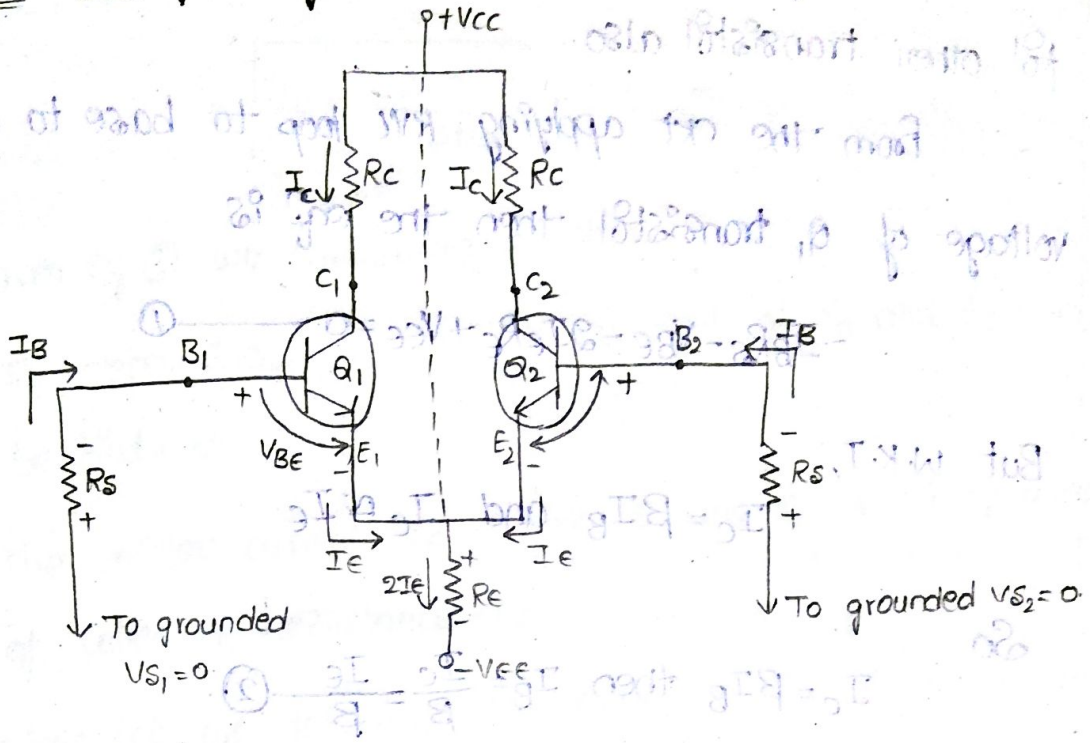
$$CMRR = \frac{A_d}{A_c}$$

$$= \frac{53.97}{49.54}$$

$$= 1.089.$$

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* DC Analysis of a Differential Amplifier :-



The DC analysis of a differential amplifier means to find out the operating point values of (or) Quisent point values of a transistor used i.e; ~~I_{CEQ}~~ "(I_{CEQ}, V_{CEQ})". The supply voltages are DC while the i/p signals are AC. So the DC equivalent circuit can be obtained simply by reducing the i/p AC signals to zero.

Assume that the source resistances are denoted by $R_{S_1} = R_{S_2} = R_S$ then the transistors Q_1 and Q_2 are matched transistors hence we can assume

(i) Both transistors have same characteristics.

(ii) $R_{E_1} \| R_{E_2} = R_E$.

(iii) $R_{C_1} = R_{C_2} = R_C$.

(iv) The magnitude of V_{CC} is equal to the magnitude of V_{EE}.

As the two transistors are matched and the ckt is symmetrical. It is enough to find out the operating

point for any one transistor. The same is applicable for other transistor also.

From the ckt applying KVL loop to base to emitter voltage of Q_1 transistor then the eqn is

$$-I_B R_S - V_{BE} - 2I_E R_E + V_{EE} = 0 \quad \text{——— (1)}$$

But W.K.T,

$$I_C = \beta I_B \text{ and } I_C \approx I_E$$

So

$$I_C = \beta I_B \text{ then } I_B = \frac{I_C}{\beta} = \frac{I_E}{\beta} \quad \text{——— (2)}$$

Sub. eq (2) in eq (1).

$$-\frac{I_E}{\beta} R_S - V_{BE} - 2I_E R_E + V_{EE} = 0$$

$$-\frac{I_E}{\beta} R_S - V_{BE} - 2I_E R_E = -V_{EE}$$

$$V_{EE} = \frac{I_E}{\beta} R_S + V_{BE} + 2I_E R_E$$

$$-I_E R_S - V_{BE}\beta - 2I_E R_E \beta + V_{EE}\beta = 0$$

$$-I_E(R_S + 2R_E\beta) - \beta(V_{BE} - V_{EE}) = 0$$

$$I_E = \frac{\beta(V_{EE} - V_{BE})}{R_S + 2R_E\beta}$$

$$\boxed{I_E = \frac{V_{EE} - V_{BE}}{\frac{R_S}{\beta} + 2R_E}}$$

W.K.T

$V_{BE} = 0.6$ to 0.7 for silicon transistor.

$= 0.2$ for germanium transistor.

In practically $\frac{R_s}{\beta} << 2R_E$ then neglecting $\frac{R_s}{\beta}$ value.

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E} \quad \text{——— (3)}$$

from eq (3) we can observe that

(i) R_E determines the emitter current of Q_1 and Q_2 can be find out.

(ii) The emitter current I_E through Q_1 and Q_2 is independent of collector resistance R_C.

(iii) Now let us determine V_{CE} value as I_E is known and $I_E \simeq I_C$ then we can determine the collector voltage (V_C) of a Q_1 transistor is

$$V_C = V_{CC} - I_C R_C \quad \text{——— (4)}$$

Neglecting the drop voltage across the source resistance R_s we can say that the voltage at the emitter of Q_1 is i.e;

$$V_E = -V_{BE} \quad \text{——— (5)}$$

Then the collector to emitter voltage is

$$V_{CE} = V_C - V_E \quad \text{——— (6)}$$

Sub. eq (4) and (5) in eq (6)

$$V_{CE} = V_{CC} - I_C R_C + V_{BE}$$

$$V_{CE} = V_{CC} + V_{BE} - I_C R_C \quad \text{——— (7)}$$

So the Quiscent point (or) Operating point values of a DC analysis D.A is

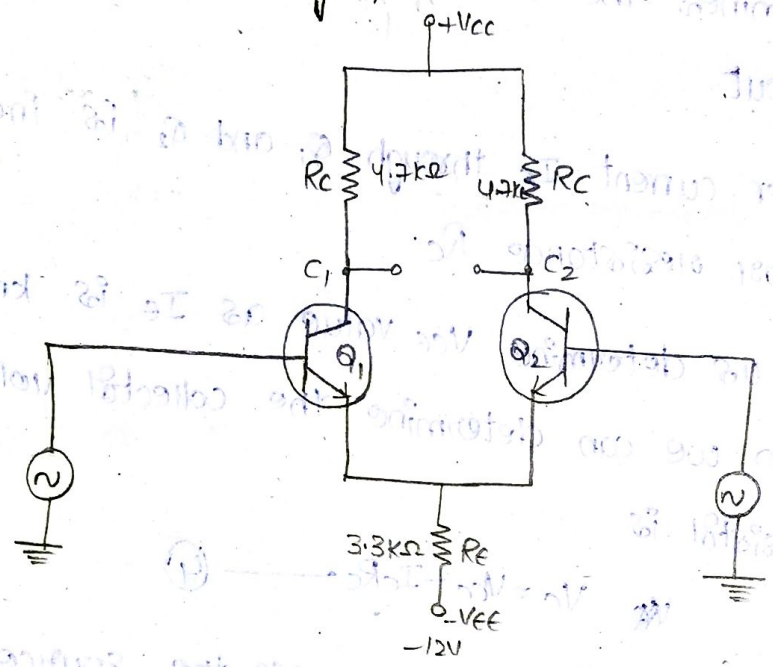
Q point values is.

$$I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E}$$

$$V_{CEQ} = V_{CC} + V_{BE} - I_C R_C$$

Problem:-

① Calculate the operating point values for the following ckt.



Sol:- Given data is

$R_C = 4.7K\Omega$

$R_E = 3.3K\Omega$

Magnitude of V_{CC} = Magnitude of $V_{EE} = 12V$.

$$I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E} \quad (\because \text{Assume } V_{BE} = 0.7)$$

$$= \frac{12 - 0.7}{2 \times 3.3 \times 10^3} = 1.7mA.$$

Assume $V_{BE} = 0.7V$ for silicon transistor then $\frac{V_{EE} - V_{BE}}{2R_E}$.

$$V_{CEQ} = V_{CC} + V_{BE} - I_C R_C \quad (\because I_C = I_{CQ} = I_E)$$

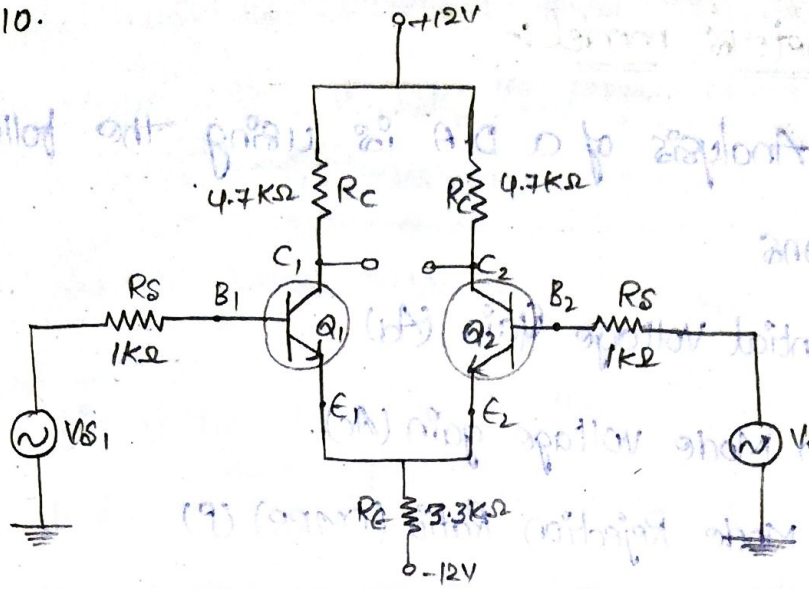
$$= 12 + 0.7 - 1.7 \times 10^{-3} \times 4.7 \times 10^3$$

$$= 4.7V.$$

② Determine the operating point values as shown in the fig.

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If $\beta = 10$.



Sol: Given data is

$R_C = 4.7K\Omega$

$R_E = 3.3K\Omega$

$R_S = 1K\Omega$

$\beta = 10$

Assume $V_{BE} = 0.7V$ then operating point values is

$$I_{CQ} = \frac{V_{BE} - V_{BE}}{\frac{R_S}{\beta} + 2R_E}$$

$$= \frac{12 - 0.7}{\left(\frac{10^3}{10}\right) + 2 \times 3.3 \times 10^3}$$

$$= 1.68\,mA$$

$$V_{CEQ} = V_{cc} + V_{BE} - I_C R_C$$

$$= 12 + 0.7 - 1.68 \times 10^{-3} \times 4.7 \times 10^3$$

$$= 4.8V$$

AC Analysis of a Differential Amplifier using h-parameters model :-

AC Analysis of a D.A is using the following specifications.

(i) Differential Voltage Gain (A_d).

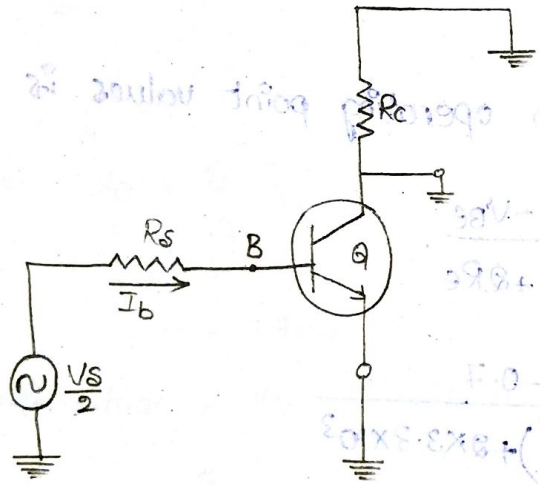
(ii) Common Mode voltage gain (A_c).

(iii) Common Mode Rejection Ratio (CMRR) (ρ).

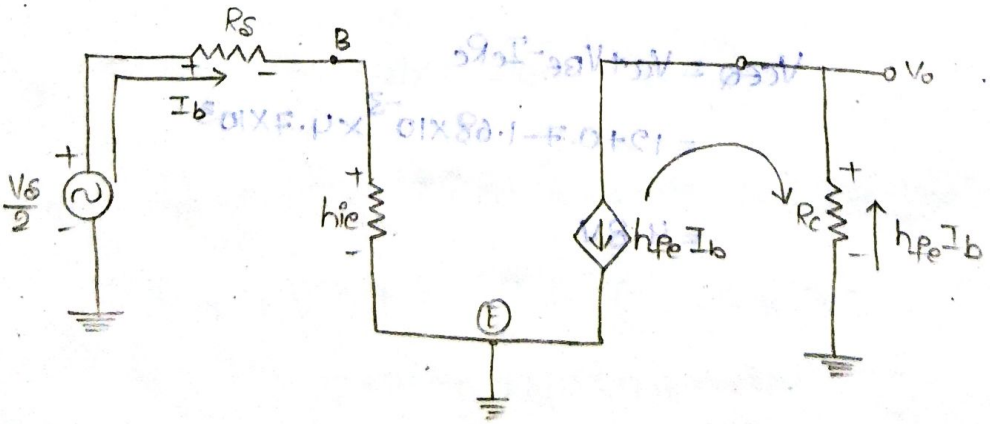
(iv) Input Resistance (R_i).

(v) Output Resistance (R_o).

(i) Differential Voltage Gain (A_d) :-



(a) AC equivalent for D.A



(b) Approximate Hybrid Model

The AC analysis differential gain calculation two i/p signals must be different from each other both are equal in magnitude but opp. in phase direction i.e;

$$V_{s_1} = \frac{V_s}{2}$$

$$V_{s_2} = -\frac{V_s}{2}$$

From fig(a) the two AC emitter currents I_{E_1} and I_{E_2} are equal in magnitude and 180° out of phase. Hence the currents through the emitter get cancelled with each other. For this purpose the AC emitter terminal can be grounded. The AC equivalent ckt for one transistor is find out for another transistor is applicable as same for the other transistor also. Thus the ckt concept is called as Half circuit Analysis.

From fig(b). By applying KVL around i/p loop is

$$\frac{V_s}{2} - I_b R_s - h_{ie} I_b = 0$$

$$\frac{V_s}{2} = I_b (R_s + h_{ie})$$

$$I_b = \frac{V_s}{2(R_s + h_{ie})} \quad \text{——— (1)}$$

Now applying KVL around o/p loop

$$V_o = -h_{fe} I_b R_c \quad \text{——— (2)}$$

Sub. eq(1) in eq(2)

$$V_o = -h_{fe} R_c \left[\frac{V_s}{2(R_s + h_{ie})} \right]$$

$$\frac{V_o}{V_s} = \frac{-h_{fe} R_c}{2(R_s + h_{ie})}$$

The $$|A_d| = \left|\frac{V_o}{V_s}\right| = \frac{h_{fe} R_c}{2(R_s + h_{ie})} \quad \text{---(3)}$$

eq(3) denoted that the differential voltage gain for unbalanced condition. If we want to calculate balanced condition diff. gain simply multiple with 2 of above eq? i.e,

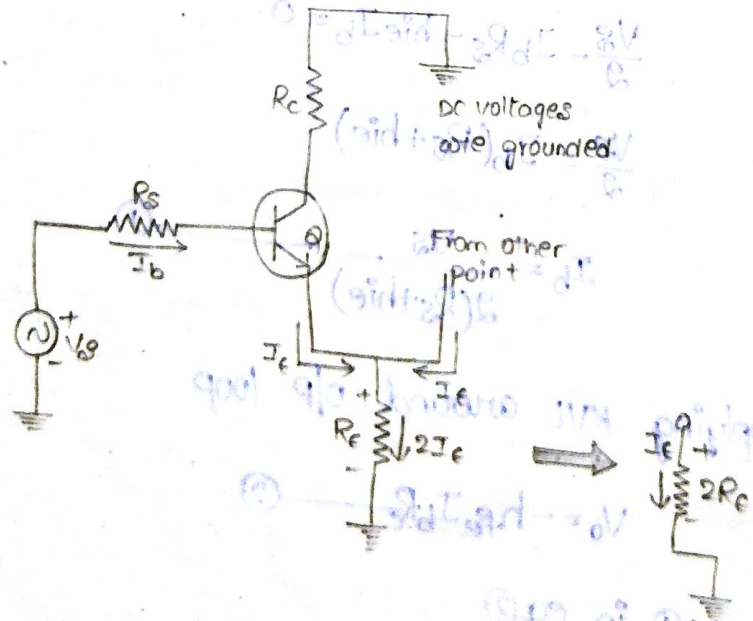
$$A_d = \frac{h_{fe} R_c}{2(R_s + h_{ie})} \longrightarrow \text{For unbalanced condition.}$$

$$A_d = 2\left[\frac{h_{fe} R_c}{2(R_s + h_{ie})}\right]$$

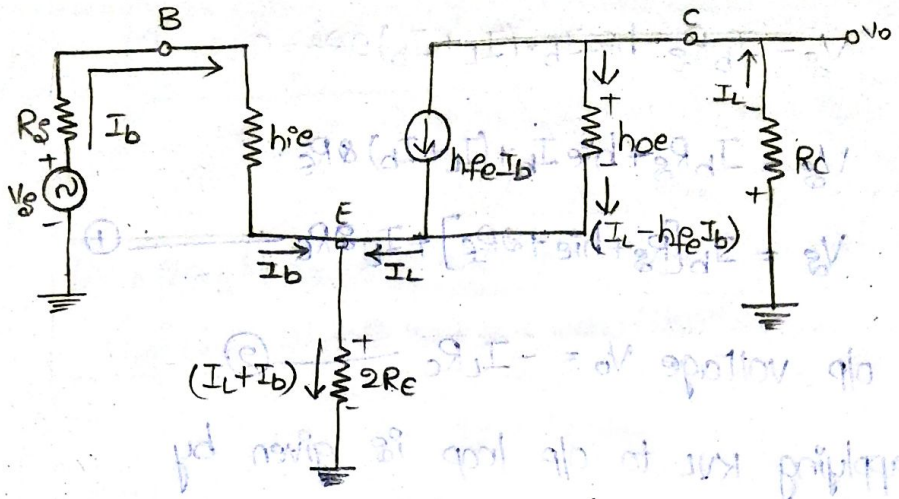
$$= \frac{h_{fe} R_c}{R_s + h_{ie}} \longrightarrow \text{For balanced condition.}$$

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(ii) Common Mode Voltage gain (A_c):-



(a) AC equivalent for common mode voltage gain operation.



(b) Approximate hybrid Model.

For a common Mode gain operation applying two inputs are same in magnitude and phase also then the common mode voltage V_c is

$$V_c = \frac{V_1 + V_2}{2}$$

Then the common mode gain $A_c = \frac{V_o}{V_c}$.

Here $V_c = \frac{V_s + V_s}{2}$

$$\therefore \boxed{A_c = \frac{V_o}{V_s}}$$

From the fig(a) the current through the emitting resistance (R_E) is two times of I_E ($2I_E$) but for the derivation purpose assume effective emitting resistance is $2R_E$ and current is I_E. Now from fig(b) we can observe that the current through $R_c = I_L$.

Current through effective emitting resistance $2R_E = I_L + I_b$ and current through hoe is

$$hoe = (I_L - h_{fe} I_b)$$

Now by applying KVL to i/p loop is given by

$$V_s - I_b R_s - h_{ie} I_b - (I_L + I_b) 2R_e = 0.$$

$$V_s = I_b R_s + h_{ie} I_b + (I_L + I_b) 2R_e$$

$$V_s = I_b [R_s + h_{ie} + 2R_e] + I_L \cdot 2R_e \quad \text{——— (1)}$$

While o/p voltage $V_o = -I_L R_c$ ——— (2).

Now by applying KVL to o/p loop is given by

$$-(I_L + I_b) 2R_e - \frac{(I_L - h_{fe} I_b)}{h_{oe}} - I_L R_c = 0.$$

$$+(I_L + I_b) 2R_e h_{oe} + (I_L - h_{fe} I_b) + I_L R_c h_{oe} = 0.$$

$$(I_L + I_b) 2R_e h_{oe} + (I_L - h_{fe} I_b) + I_L R_c h_{oe} = 0.$$

$$(I_L - h_{fe} I_b) + (I_L + I_b) 2R_e h_{oe} + I_L R_c h_{oe} = 0.$$

$$\frac{I_L}{I_b} = \frac{h_{fe} - 2R_e h_{oe}}{1 + 2R_e h_{oe} + R_c h_{oe}}$$

$$\frac{I_L}{I_b} = \frac{h_{fe} - 2R_e h_{oe}}{1 + h_{oe}[2R_e + R_c]} \quad \text{——— (3)}$$

Now from above eq? sub. I_b value in eq (1)

$$I_b = \frac{I_L [1 + h_{oe}(2R_e + R_c)]}{h_{fe} - 2R_e h_{oe}}.$$

$$\therefore V_s = \left[\frac{I_L [1 + h_{oe}(2R_e + R_c)]}{h_{fe} - 2R_e h_{oe}}\right](R_s + h_{ie} + 2R_e) + I_L \cdot 2R_e$$

$$V_s = I_L \left[\left(\frac{1 + h_{oe}(2R_e + R_c)}{h_{fe} - 2R_e h_{oe}}\right)(R_s + h_{ie} + 2R_e) + 2R_e\right].$$

$$= I_L \left[\left(\frac{1 + h_{oe}(2R_e + R_c)(R_s + h_{ie} + 2R_e)}{h_{fe} - 2R_e h_{oe}}\right) + 2R_e\right].$$

$$V_s = I_L \left[\frac{[1+h_{oe}(2R_e+R_c)](R_s+h_{ie}+2R_e)+2R_e h_{fe}-4R_e^2 h_{oe}}{h_{fe}-2R_e h_{oe}} \right]$$

$$= I_L \left[\frac{R_s+2h_{oe}R_eR_s+h_{oe}R_sR_c+h_{ie}+2h_{oe}R_eh_{ie}+2h_{ie}h_{oe}R_c+2R_e+ \cancel{4R_e^2 h_{oe}}+2h_{oe}R_eR_c+2R_eh_{fe}-\cancel{4R_e^2h_{oe}}}{h_{fe}-2R_eh_{oe}} \right]$$

$$= I_L \left[\frac{R_s+2h_{oe}R_eR_s+h_{oe}R_sR_c+h_{ie}+2h_{oe}R_eh_{ie}+h_{ie}h_{oe}R_c+2R_e+2h_{oe}R_eR_c+2R_eh_{fe}}{h_{fe}-2R_eh_{oe}} \right]$$

$$= I_L \left[\frac{2R_e(1+h_{fe})+R_s(1+2R_eh_{oe})+h_{ie}(1+2R_eh_{oe})+h_{oe}R_c(2R_e+R_s+h_{ie})}{h_{fe}-2R_eh_{oe}} \right]$$

from the above eqn neglecting the terms R_eh_{oe} and h_{oe} term has practically $h_{oe}R_c << 1$ then neglecting and get the eqn is

$$= I_L \left[\frac{2R_e(1+h_{fe})+R_s(1+2R_eh_{oe})+h_{ie}(1+2R_eh_{oe})}{h_{fe}-2R_eh_{oe}} \right].$$

$$V_s = I_L \left[\frac{2R_e(1+h_{fe})+(R_s+h_{ie})(1+2R_eh_{oe})}{h_{fe}-2R_eh_{oe}} \right] \quad \text{---------- (4)}$$

Sub. from above eqn 'I_L' value in eq (2).

$$V_o = \left[\frac{-V_s(h_{fe}-2R_eh_{oe})}{2R_e(1+h_{fe})+(R_s+h_{ie})(1+2R_eh_{oe})} \right] R_c.$$

$$\frac{V_o}{V_s} = \frac{-(h_{fe}-2R_eh_{oe})R_c}{2R_e(1+h_{fe})+(R_s+h_{ie})(1+2R_eh_{oe})}.$$

In practically h_{oe} is generally neglected and hence the expression for common mode gain (A_c) is given by

$$A_c = \frac{V_o}{V_s} = \frac{-h_{fe} R_c}{2R_e(1+h_{fe}) + (R_s + h_{ie})}$$

(iii) Common Mode Rejection Ratio (CMRR) :-

CMRR is defined as the ratio of differential gain (A_d) to common mode gain (A_c) i.e;

$$CMRR = \left| \frac{A_d}{A_c} \right|$$

W.K.T $A_d = \frac{h_{fe} R_c}{R_s + h_{ie}}$

$$CMRR = \left| \frac{\left(\frac{h_{fe} R_c}{R_s + h_{ie}} \right)}{\left(\frac{-h_{fe} R_c}{2R_e(1+h_{fe}) + (R_s + h_{ie})} \right)} \right|$$

$$\therefore CMRR = \left| \frac{A_d}{A_c} \right| = \left| \frac{2R_e(1+h_{fe}) + (R_s + h_{ie})}{R_s + h_{ie}} \right|$$

(iv) Input Resistance (R_i) :-

The i/p resistance R_i is calculated by using the approximate hybrid model fig. in differential voltage gain. By using that fig. i/p KVL loop eqn is

$$\frac{V_s}{2} - I_b R_s - I_b h_{ie} = 0.$$

$$\frac{V_s}{2} = I_b [R_s + h_{ie}].$$

$$V_s = 2 I_b [R_s + h_{ie}].$$

$\therefore$ **Input resistance** $(R_i) = \frac{V_s}{I_b} = 2[R_s + h_{ie}]$.

* **Note:-**

Input resistance R_i is common for all types of differential amplifiers.

(v) **Output Resistance (R_o):-**

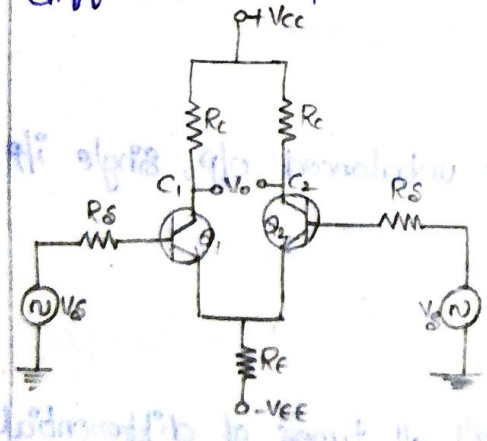
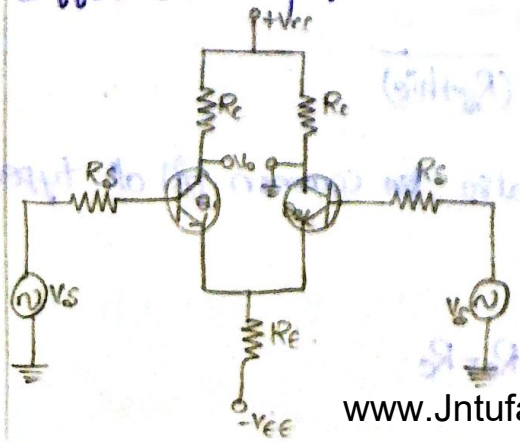
From the ckt the o/p resistance R_o is equal to collector resistance R_c

$$\therefore R_o = R_c$$

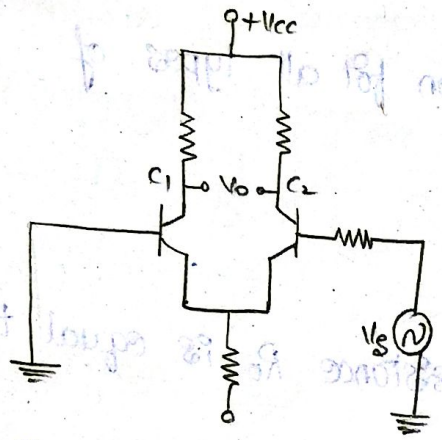
* **Note:-**

Output resistance R_o is also common for all types of differential amplifiers.

Table

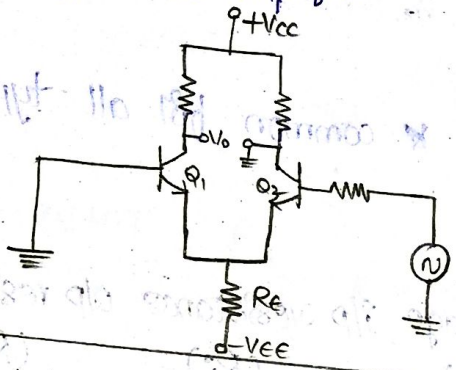
S.No	Types of Differential Amplifier	Diff. voltage gain (A_d)	i/p resistance (R_i)	o/p resistance (R_o).
1.	Dual input balanced o/p differential Amplifier. 	$A_d = \frac{h_{fe} R_c}{R_s + h_{ie}}$	$R_i = 2(R_s + h_{ie})$	$R_o = R_c$
2.	Dual i/p unbalanced o/p differential amplifier. 	$A_d = \frac{h_{fe} R_c}{2(R_s + h_{ie})}$	$R_i = 2(R_s + h_{ie})$	$R_o = R_c$

3. Single i/p balanced o/p Differential Amplifier.



$A_d = \frac{h_{fe} R_c}{R_s + h_{ie}}$ $R_i = 2(R_s + h_{ie})$ $R_o = R_c$

4. Single i/p unbalanced o/p differential amplifier.



$A_d = \frac{h_{fe} R_c}{2(R_s + h_{ie})}$ $R_i = 2(R_s + h_{ie})$ $R_o = R_c$.

Note:-

1. The differential gain for dual i/p balanced o/p, single i/p balanced o/p is same i.e;

$$A_d = \frac{h_{fe} R_c}{R_s + h_{ie}}$$

2. The differential gain for dual i/p unbalanced o/p, single i/p unbalanced o/p is same i.e;

$$A_d = \frac{h_{fe} R_c}{2(R_s + h_{ie})}$$

3. Common mode gain (A_c) is common for all types of differential amplifiers i.e;

$$A_c = \frac{-h_{fe} R_c}{2R_E(1+h_{fe}) + (R_s + h_{ie})}$$

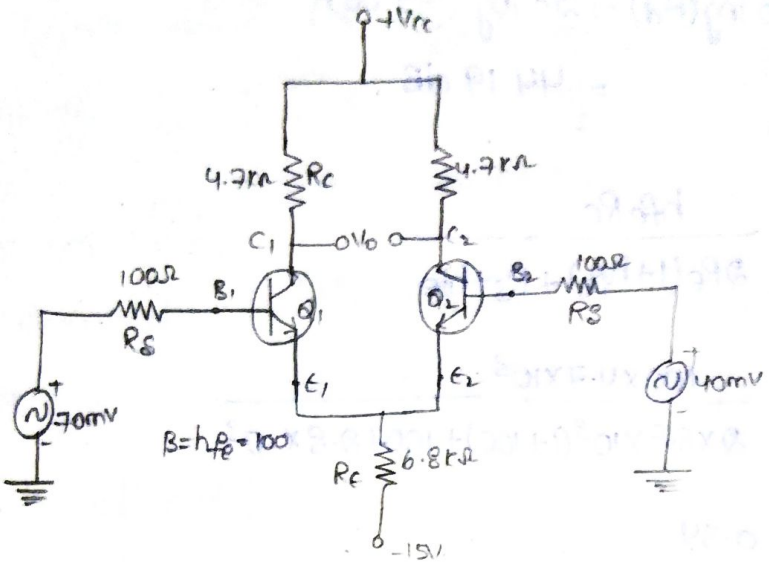
4. Input and Output resistances is also common for all types of differential amplifier.

$$R_i = 2[R_s + h_{ie}] \text{ and } R_o = R_c$$

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Problem:-

① Fig. shows Dual i/p balanced o/p D.A configuration assuming transistors with $h_{ie} = 2.8K\Omega$. Calculate (i) operating point values (ii) Diff. gain (iii) CMRR (iv) common mode gain (v) o/p voltage V_o if $V_{s_1} = 70mV_{p-p}$ at 1 KHz and $V_{s_2} = 40mV_{p-p}$ at 1 KHz.



Sol:- Given data is

$R_C = 4.7K\Omega$

$R_E = 6.8K\Omega$

$R_S = 100\Omega$

$\beta = h_{fe} = 100$

$h_{ie} = 2.8K\Omega$

$V_{S_1} = 70mV_{p-p}$

$V_{S_2} = 40mV_{p-p}$

(i) Operating point values (I_{CQ}, V_{CEQ})

$$I_{CQ} = \frac{V_{EE} - V_{BE}}{\frac{R_S}{\beta} + 2R_E} = \frac{15 - 0.7}{\frac{100}{100} + 2(6.8 \times 10^3)} = 1.05mA$$

$$V_{CEQ} = V_{CC} - I_C R_C + V_{BE}$$

$$= 15 + 0.7 - (1.05 \times 10^{-3})(4.7 \times 10^3)$$

$$= 10.76V$$

∴ The operating point values is 1.05mA and 10.76V.

(ii) $A_d = \frac{h_{fe} R_C}{R_S + h_{ie}}$

$= \frac{100 \times 4.7 \times 10^3}{100 + 2.8 \times 10^3}$

$= 162.06$

A_d (in dB) $= 20 \log(A_d) = 20 \log(162.06)$

$= 44.19$ dB.

(iii) $A_C = \frac{h_{fe} R_C}{2R_E(1+h_{fe}) + R_S + h_{ie}}$

$= \frac{100 \times 4.7 \times 10^3}{2 \times 6.8 \times 10^3 (1+100) + 100 + 2.8 \times 10^3}$

$= 0.34$

A_C (in dB) $= 20 \log(0.34) = -9.37$ dB.

(iv) $CMRR = \left| \frac{A_d}{A_C} \right|$

$= \frac{162.06}{0.34} = 476.6$

CMRR (in dB) $= 20 \log(476.6)$

$= 53.56$ dB.

(v) $V_0 = A_d V_d + A_C V_C$

$V_d = V_1 - V_2 = 70 - 40 = 30$mV.

$V_C = \frac{V_1 + V_2}{2} = \frac{70+40}{2} = 55$mV.

$V_0 = (162.06)\, 30 \times 10^{-3} + (0.34)(55 \times 10^{-3})$

$V_0 = 4.8 V_{p-p}$

AC analysis of a Differential Amplifier using r - parameters

S.No	Types of Diff. Ampl.	Diff. gain (A_d)	I/p resistance	o/p resistance
1.	Dual input Balanced output Differential Amplifier.	$A_d = \frac{R_c}{r_e}$	$R_i = 2r_e\beta_{ac}$	$R_o = R_c$
2.	Dual i/p unbalanced o/p differential Amplifier.	$A_d = \frac{R_c}{2r_e}$	$R_i = 2r_e\beta_{ac}$	$R_o = R_c$
3.	Single i/p balanced o/p differential Amplifier.	$A_d = \frac{R_c}{r_e}$	$R_i = 2r_e\beta_{ac}$	$R_o = R_c$
4.	Single i/p unbalanced o/p differential Amplifier.	$A_d = \frac{R_c}{2r_e}$	$R_i = 2r_e\beta_{ac}$	$R_o = R_c$

From the above observations the AC effective emitting resistance (r_e) is designed as

$$r_e = \left[\frac{26mV}{I_E}\right]\Omega$$

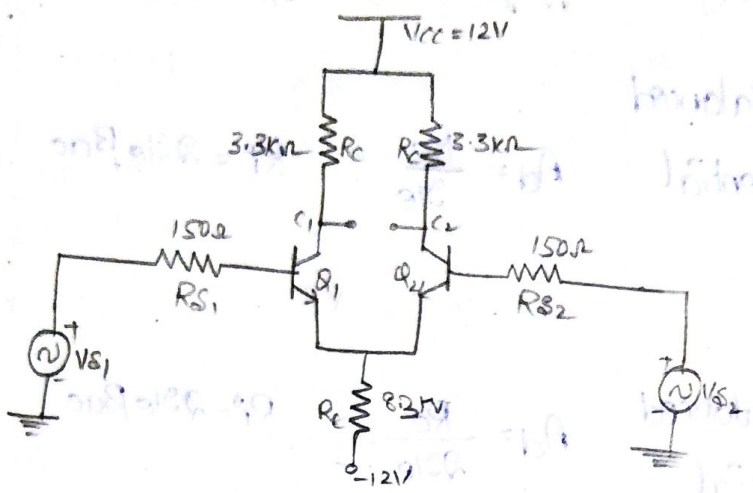
And also the relation b/w hybrid parameters and r parameters using the h_{ie}, h_{fe} and r_e is given by

$$h_{ie} = h_{fe} \cdot r_e$$

where $h_{fe} = \beta$ = gain.

1/7/18 Problem:-

1 For the D.A shown in fig. Calculate (i) operating point values (ii) voltage gain (iii) i/p and o/p resistances assume $\beta = 100$.



Note:- In problems, hie value is not given use R parameter analysis is otherwise h-parameter is used.

1. Operating point

$$I_{CQ} = \frac{V_{BE} - V_{BC}}{\frac{R_S}{\beta} + 2R_C}$$

$$= \frac{12 - 0.7}{\frac{150}{100} + 2(8.3 \times 10^3)} = 0.688 mA$$

$$V_{CEQ} = V_{CC} - I_C R_C + V_{BE}$$

$$= 12 + 0.7 - (0.68 \times 10^{-3})(3.3 \times 10^3)$$

$$= 10.46V$$

(iii) Voltage gain

$$A_d = \frac{R_C}{r_e}$$

$$\text{But } r_e = \left(\frac{26mV}{I_E}\right)\Omega$$

$$= \frac{26 \times 10^{-3}}{0.688 \times 10^{-3}}$$

$$= 38.2\Omega$$

$$A_d = \frac{3.3 \times 10^3}{38.2} = 86.3\Omega$$

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(iii) i/p and o/p resistance

$R_i = 2 r_e \beta_{ac}$ $\quad R_o = R_c$

$= 2 \times 38.2 \times 100$ $\quad = 3.3 K\Omega$.

$= 7.6 K\Omega$

Level Translation (or) Level shifter:-

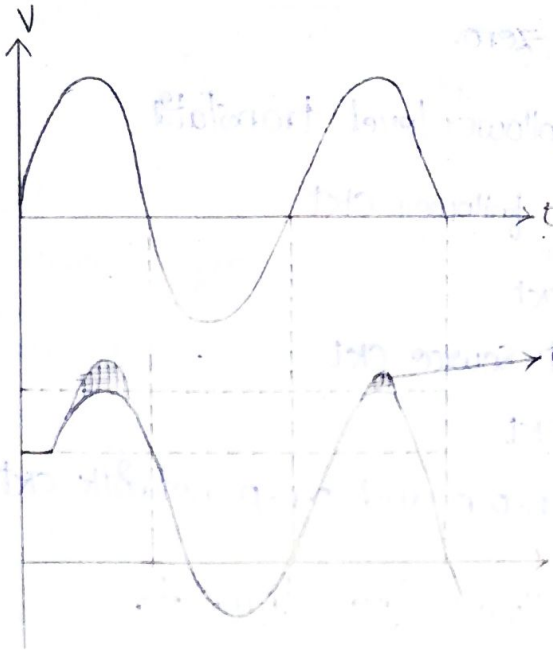




Fig:- Block diagram of OP-amp

Directly coupled without any elements. This op-amp amplifies not only AC signal but also amplifies DC signal. The DC biasing voltage level propagates through the amplifies stage then the o/p finally appears as a significant dc component along with AC o/p.

By the above considerations there will be effects the following responses. Those are

(i) The o/p get distorted.

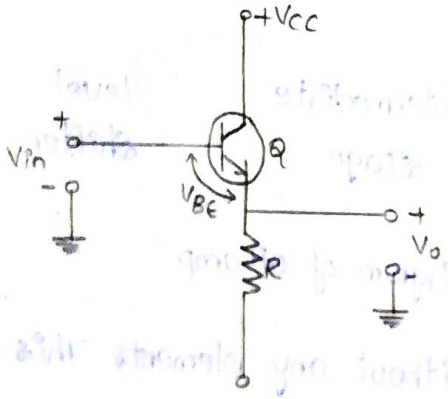
(ii) It limits the maximum o/p voltage swing.

From the fig. we can observe that the DC level is at zero, analog i/p when the signal level is shifted the o/p is also shifted with DC component then the above two effects will be produced

→ There are several circuits used to bring down to DC level down to zero.

1. Basic Emitter follower level translator
2. Modified emitter follower ckt
3. Current mirror ckt
4. Constant current source ckt
5. V_{BE} multiplier ckt
6. Combination of n-p-n and p-n-p network ckt

(1) Basic Emitter follower level translator:-



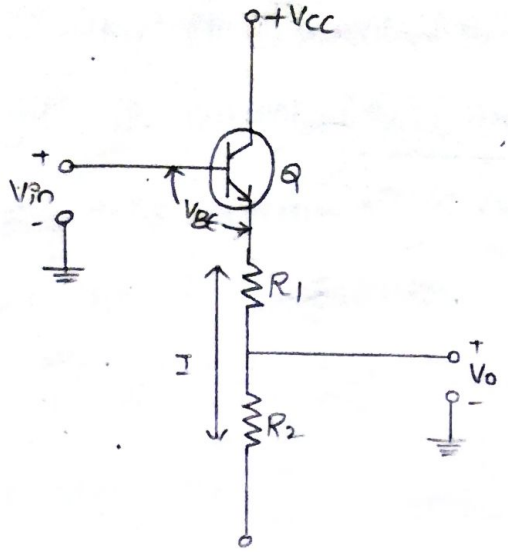
Using the particular fig. the basic emitter follower which can be used as a level translator. It can provide an amount of 0.7V shift from fig. the amount of shift is equal to V_{BE} i.e,

$$V_o = V_{in} - V_{BE} \quad \text{---------- (1)}$$

This ckt is useful if the shift is 0.7V (or) less than 0.7V

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(2) Modified Emitter follower circuit :-



In this circuit, this is useful other than 0.7V shift is applied. Thus, the circuit is modified by the network replacing $\frac{R}{R_1+R_2}$ from previous circuit. Using this fig. we can control the o/p voltage V_o.

From the fig. by applying KVL around i/p loop is given by

$$V_{in} - V_{BE} - I(R_1+R_2) = 0$$

$$I(R_1+R_2) = -V_{BE} + V_{in}$$

$$I = \frac{V_{in} - V_{BE}}{R_1+R_2} \quad \text{——— (1)}$$

Now applying KVL around o/p loop

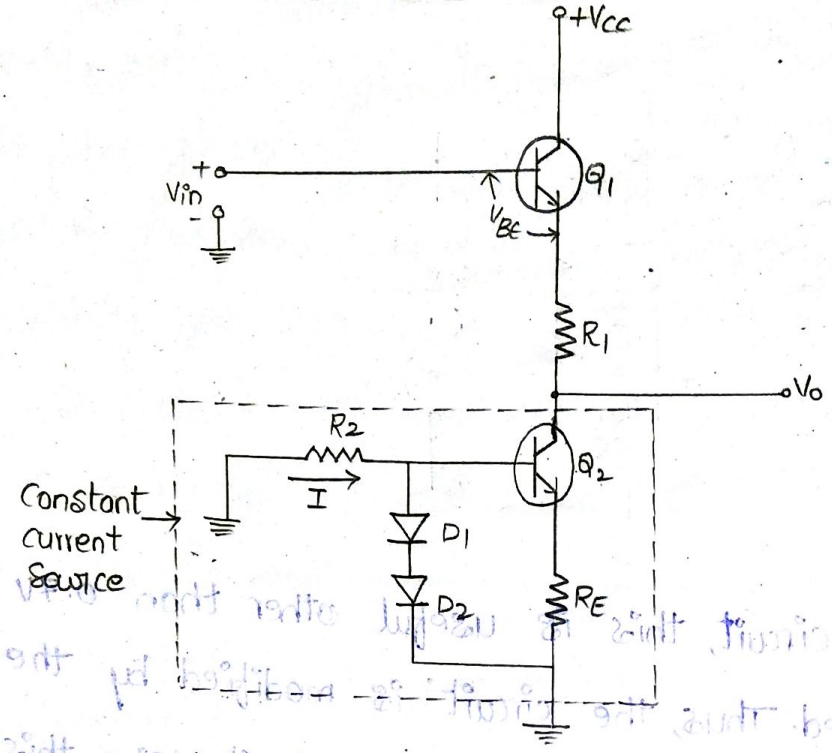
$$V_o = IR_2 \quad \text{——— (2)}.$$

Sub. eq (1) in (2)

$$\boxed{V_o = \left(\frac{V_{in} - V_{BE}}{R_1+R_2}\right) \cdot R_2}$$

From this eqn, by selecting the proper values of R_1 and R_2 we can take control the o/p voltage V_o.

(3) Constant current source ckt:-



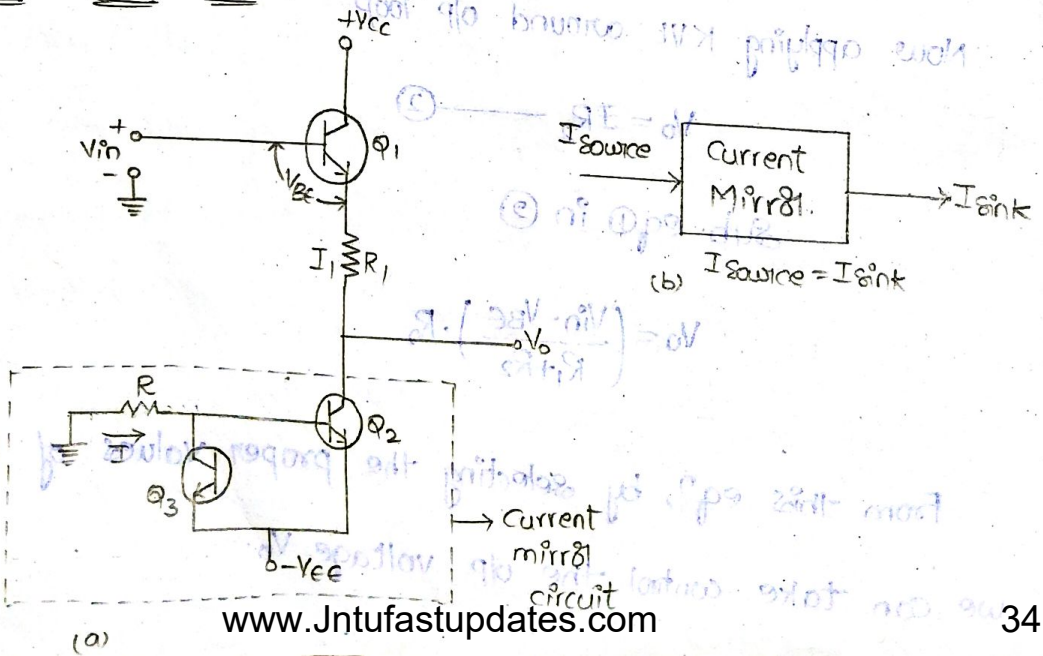
The constant current source circuit is also used as improving the levels of transistor. Here from the constant current source is provided by the transistor Q_2 whose ckt current is constant i.e; I = constant.

Then, from the fig. the o/p voltage V_o is written as

$$V_o = V_{in} - V_{BE} - I_1 R_1$$

By selecting the proper values of R_1 and I, we can contol the o/p voltage V_o.

(4) Current Mirror ckt:-



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Current mirror is defined as the o/p current is forced to equal the i/p current i.e; o/p current is the mirror image of i/p current i.e; $I_{source} = I_{sink}$.

By using this current mirror ckt the level translator is also control the o/p voltage V_o.

From the fig(a) because of current mirror $I_1 = I$.

i.e; then from the ckt $I = \frac{V_{EE} - V_{BE}}{R_2}$

$$\therefore I_1 = I = \frac{V_{EE} - V_{BE}}{R_2} \quad \text{——— (1)}$$

Then the o/p voltage $V_o = V_{in} - V_{BE} - I_1 R_1$

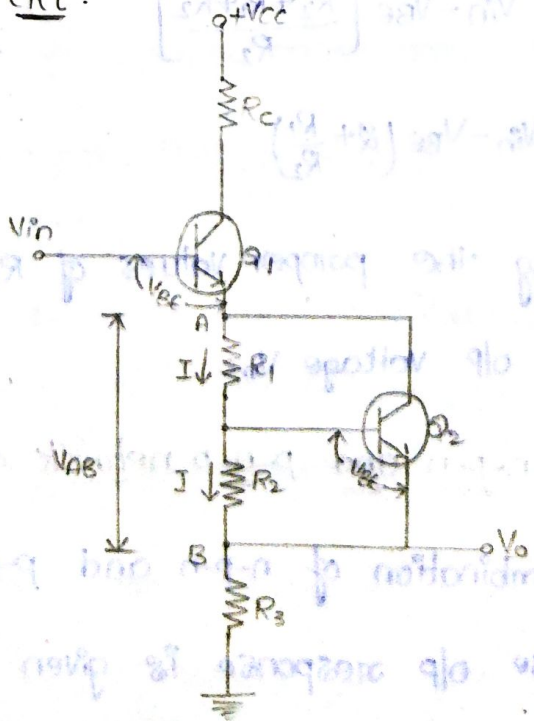
$$V_o = V_{in} - V_{BE} - I R_1 \quad \text{——— (2)}$$

Sub eq(1) in (2)

$$\boxed{V_o = V_{in} - V_{BE} - \left(\frac{V_{EE} - V_{BE}}{R_2}\right) R_1}$$

By selecting the proper values of R_1 and R_2, we can take the control of the o/p voltage.

(5) V_{BE} multiplier ckt :-



From the fig. the voltage b/w nodes A and B is

$$V_{AB} = I(R_1+R_2) \quad \text{---- (1)}$$

By applying KVL to the base to emitter loop of Q_2 transistor is written as

$$V_{BE} = IR_2 \quad \text{---- (a)}$$

$$I = \frac{V_{BE}}{R_2} \quad \text{---- (2)}$$

Sub. eq^n (2) in (1).

$$V_{AB} = \frac{V_{BE}(R_1+R_2)}{R_2} \quad \text{---- (3)}$$

Now, the o/p voltage V_o can be written as

$$V_o = V_{in} - V_{BE} - V_{AB} \quad \text{---- (4)}$$

Sub. eq (3) in eq (4).

$$V_o = V_{in} - V_{BE} - \frac{V_{BE}(R_1+R_2)}{R_2}$$

$$V_o = V_{in} - V_{BE}\left[1 + \left(\frac{R_1+R_2}{R_2}\right)\right]$$

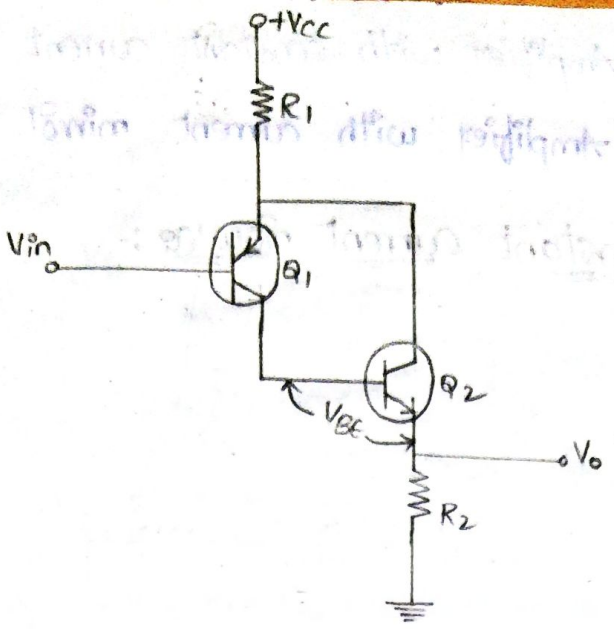
$$= V_{in} - V_{BE}\left[\frac{R_2+R_1+R_2}{R_2}\right]$$

$$\boxed{V_o = V_{in} - V_{BE}\left(2 + \frac{R_1}{R_2}\right)}$$

By selecting the proper values of R_1 and R_2 we can take control of o/p voltage V_o.

(6) Combination of n-p-n and p-n-p network circuits:

The combination of n-p-n and p-n-p network transistor whose o/p response is given as



$$V_o = \frac{R_2}{R_1}\left[V_{cc} - V_{in} - V_{BE}\right].$$

By selecting the proper values of R_1 and R_2 we can take control of o/p voltage V_o.

Methods of IMPROVING CMRR:-

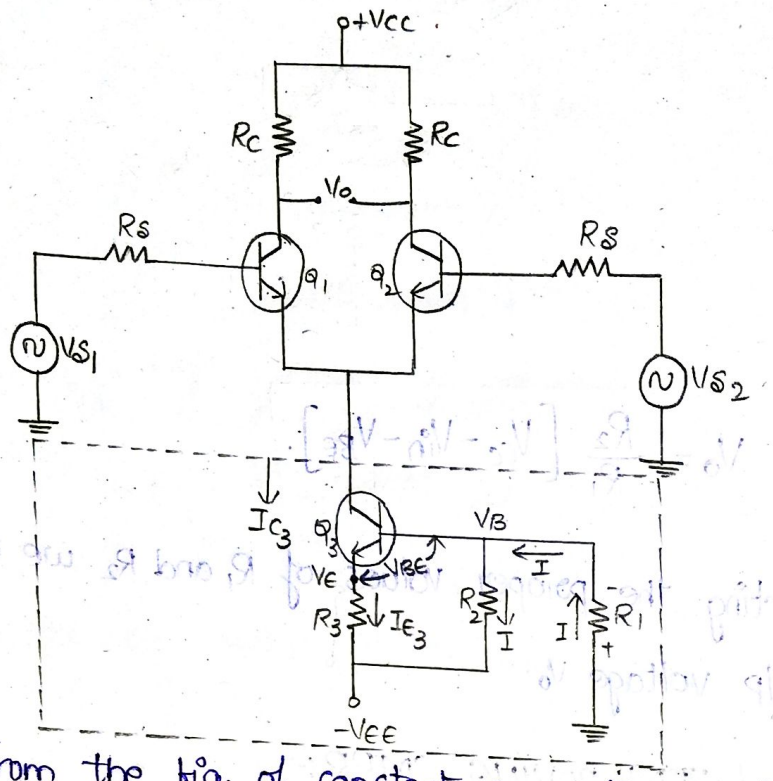
To increase the value of CMRR, the common mode gain (A_c) must be reduced. The common mode gain approaches to zero then effective Emitting resistance (R_E) tends to infinity (or) higher value. This is because of R_E introduced a -ve feed back in Common mode gain operation.

Thus higher value of R_E, lesser value of A_c and higher is the value of CMRR. But practically (R_E) cannot be selected very high due to the following limitations such as (i) larger R_E needs higher biasing voltage to set the operating point values.

(ii) This increases the overall chip area hence practically in place of R_E we can replace the following two methods.

1) Differential Amplifier with constant current source.
2) Differential Amplifier with current mirror circuit.

(1) D.A with constant current source :-



From the fig. of constant current source ckt, applying KVL to the i/p loop, then eqn is

$$IR_1 + IR_2 - V_{EE} = 0.$$

$$I(R_1+R_2) = V_{EE}$$

$$\boxed{I = \frac{V_{EE}}{R_1+R_2}} \quad \text{---- (1)}$$

Practically, the voltage at base (V_B) is $V_B = -IR_1$ ---- (2)

Sub. eq (1) in (2).

$$\boxed{V_B = \frac{-V_{EE}}{R_1+R_2} \cdot R_1} \quad \text{---- (3)}$$

The emitter voltage (V_E) can be written as

$$V_E = V_B - V_{BE} \quad \text{---- (4)}$$

Then the emitter current across Q_3 transistor is

$$I_{E_3} = \frac{V_E - (-V_{EE})}{R_3}$$

$$I_3 = \frac{V_E + V_{EE}}{R_3} \quad \text{——⑤}$$

Sub. eq ④ in ⑤

$$I_3 = \frac{V_B - V_{BE} + V_{EE}}{R_3}$$

$$I_{E_3} = \frac{\frac{-V_{EE} \cdot R_1}{R_1+R_2} - V_{BE} + V_{EE}}{R_3} \quad [\because \text{eq}③].$$

$$I_{E_3} = \frac{-V_{EE} \cdot R_1 - V_{BE}(R_1+R_2) + V_{EE}(R_1+R_2)}{R_3 (R_1+R_2)}$$

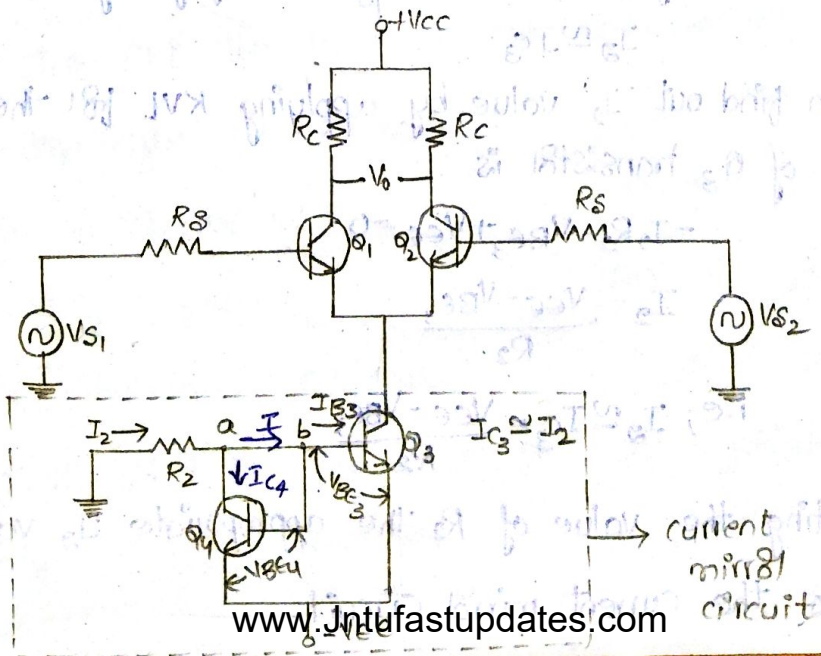
$$= \frac{V_{EE}\left(\frac{R_2}{R_1+R_2}\right) - V_{BE}}{R_3}$$

W.K.T the collector current I_{C_3} is approximately equal to I_{E_3}.

$$I_{C_3} \cong I_{E_3} = \frac{V_{EE}\left(\frac{R_2}{R_1+R_2}\right) - V_{BE}}{R_3}$$

By selecting the values of V_{EE}, R_1, R_2, R_3 and V_{BE} as constants Then the current I_{C_3} is almost equal to emitter current I_{E_3} and also constant.

(2) D.A with current mirror CKT :-



From the current mirror circuit, the two matched transistors Q_3 and Q_4 whose base to emitter voltages, Base currents and collector currents are same. i.e;

$$V_{BE_3} = V_{BE_4}$$

$$I_{B_3} = I_{B_4}$$

$$I_{C_3} = I_{C_4}$$

Now applying KCL at node 'a'

$$I_2 = I + I_{C_4} \quad \text{——— ①}$$

Similarly at node b, by applying KCL

$$I = I_{B_3} + I_{B_4}$$

$$I = I_{B_4} + I_{B_4} \quad (\because I_{B_3} = I_{B_4})$$

$$I = 2I_{B_4} \quad \text{——— ②}$$

from eq ①,

$$I_2 = 2I_{B_4} + I_{C_4}$$

$$I_2 = 2I_{B_3} + I_{C_4} \quad \text{——— ③}$$

W.K.T $I_{B_3} = \frac{I_{C_3}}{\beta}$, then from eq ③

$$\therefore I_2 = \frac{2I_{C_3}}{\beta} + I_{C_4}$$

$$= I_{C_3} + \frac{2I_{C_3}}{\beta} \quad (\because I_{C_3} = I_{C_4})$$

$$I_2 = I_{C_3}\left(1 + \frac{2}{\beta}\right)$$

Practically, β is very large hence $\frac{2}{\beta}$ is negligibly small then

$$I_2 \simeq I_{C_3}$$

Now, we can find out 'I_2' value by applying KVL for the base to emitter loop of Q_3 transistor is

$$-I_2R_2 - V_{BE_3} + V_{EE} = 0$$

$$I_2 = \frac{V_{EE} - V_{BE_3}}{R_2}$$

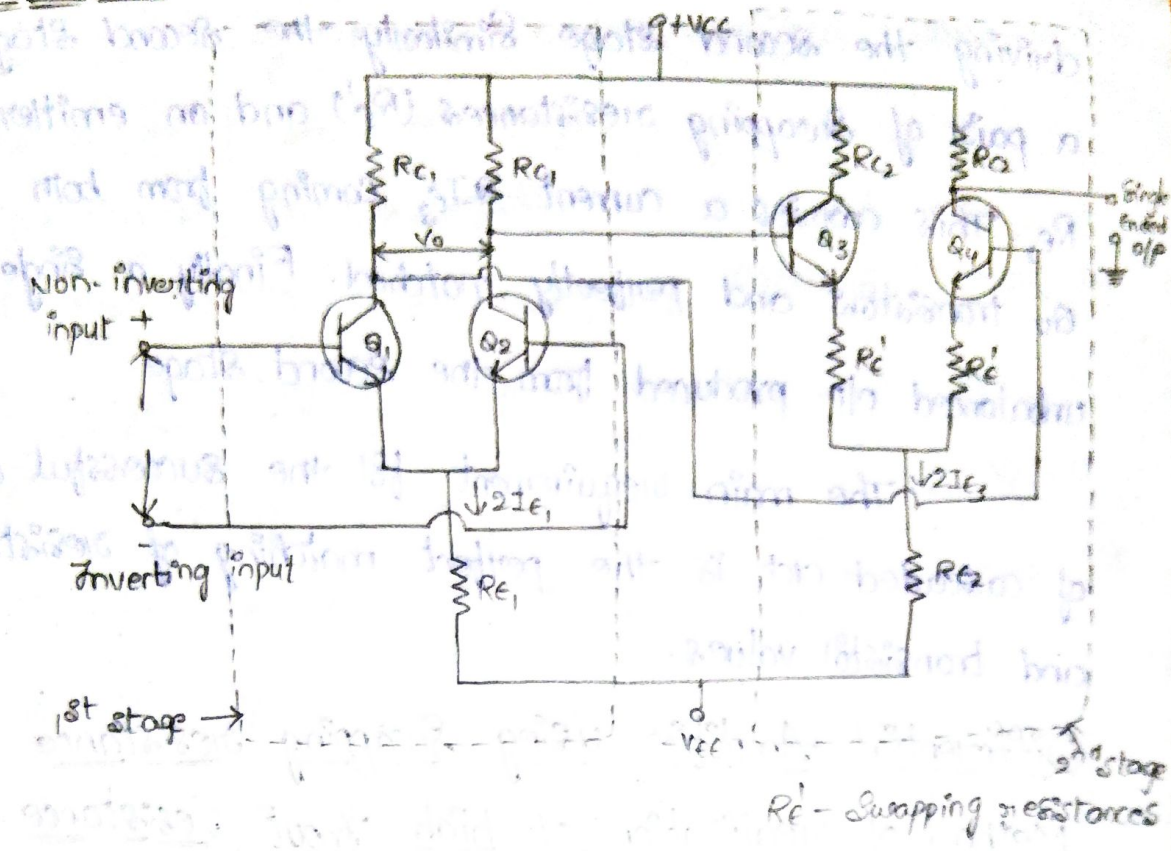
i.e; $I_2 \simeq I_{C_3} = \frac{V_{EE} - V_{BE_3}}{R_2}$

By selecting the value of R_2 the appropriate I_2 value can be set for the current mirror circuit.

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23/7/18

Cascaded Differential Amplifier:-



Cascaded differential Amplifiers is defined as the series of two or more differential amplifiers which is called as cascaded differential amplifiers and the output produces single ended o/p.

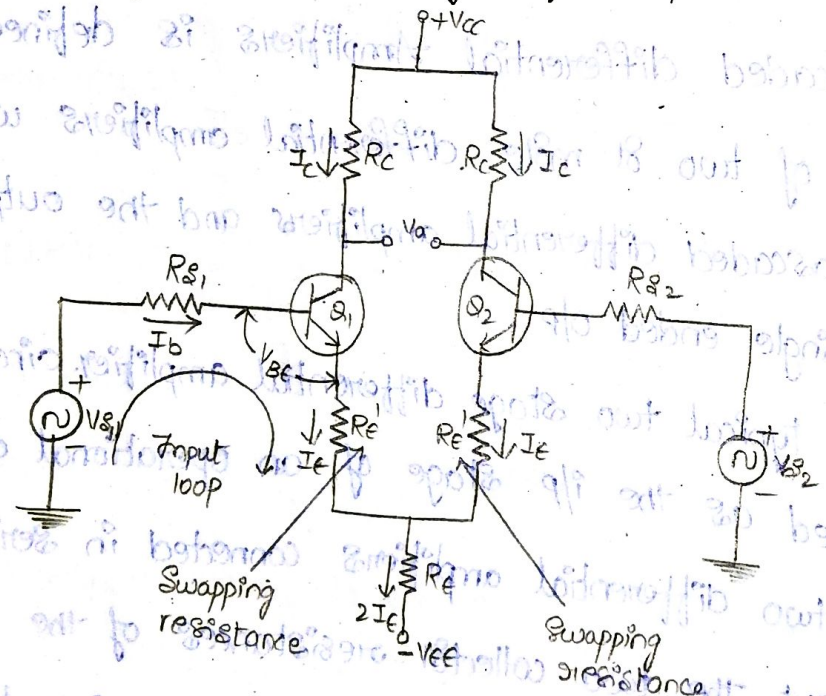
The typical two stage differential amplifier circuit is commonly used as the i/p stage of an operational amplifier and those two differential amplifiers connected in series. From the ckt the two collector resistances of the first stage are equal as shown as R_{C_1} while the second stage collector resistances are also equal shown as R_{C_2}.

The first stage is a DIBO D.A which uses the emitter resistance R_{E_1} causes current $2I_{E_1}$ from the Q_1 transistor which is same as from Q_2 transistor, both are perfectly matched transistors. The o/p of the first stage

act as i/p to the second stage that means first stage driving the second stage. Similarly the second stage uses a pair of swapping resistances (R_E') and an emitter resistance R_{E_2}. This carries a current $2I_{E_3}$ coming from both Q_3 and Q_4 transistors and perfectly matched. Finally a single ended unbalanced o/p produced from the second stage.

The main requirement for the successful operation of cascaded ckt is the perfect matching of resistances and transistor values.

Differential Amplifier using Swapping resistance (or) Method of realization of high Input resistance :-



The use of swapping resistances is to achieve the high i/p resistances, external resistances R_E' is connected in series with each emitter of each transistor of a D.A. Such resistances are called Swapping resistances. The various effects of swapping resistances on the performance of D.A's are

(i) Increases the i/p resistances.

(ii) Minimization of changes in the transistor parameters due to the factors like temp

(iii) Reduction in differential gain.

(iv) Increase in the linearity range of differential amplifier.

(a) DC analysis:- Using swapping resistances R_E' for dc analysis AC voltage sources are grounded i.e; $V_{s_1} = V_{s_2} = 0$ and $R_{s_1} = R_{s_2} = R_s$. From the fig. by applying KVL around i/p loop is given by

$$-R_{s_1} I_b - V_{BE} - I_E R_E' - 2I_E R_E + V_{EE} = 0 \quad \text{——— (1)}$$

W.K.T the values of I_B, I_C and I_E of Q_1 and Q_2 transistors are perfectly matched then

$$I_B = \frac{I_C}{\beta} \simeq \frac{I_E}{\beta} = \frac{I_E}{h_{fe}} \quad \text{——— (2)}$$

Sub. eq (2) in eq (1)

$$-R_{s_1} \frac{I_E}{h_{fe}} - V_{BE} - I_E R_E' - 2I_E R_E + V_{EE} = 0$$

$$I_E = \frac{V_{EE} - V_{BE}}{\left(\frac{R_s}{h_{fe}}\right) + R_E' + 2R_E} \quad \text{——— (3)}$$

from the above eq^n $\frac{R_s}{h_{fe}}$ is too small then neglecting that and the eq^n can be written as

$$I_E = \frac{V_{EE} - V_{BE}}{R_E' + 2R_E} \simeq I_{CQ}$$

While the eq^n for collector to emitter loop voltage remains same as before which is $V_{CEQ} = V_{CC} + V_{BE} - I_C R_C$

(b) AC analysis:-

AC analysis of a differential amplifier using swap resistance is same as AC analysis of D.A. but include the swapping resistance R_E' then the diff. voltage gain for DIBO is

$$A_d = \frac{h_{fe} R_C}{R_S + h_{ie} + R_E'(1+h_{fe})}$$

for dual i/p unbalanced o/p is

$$A_d = \frac{h_{fe} R_C}{2\left[R_S + h_{ie} + R_E'(1+h_{fe})\right]}$$

Similarly the common mode gain expression for all configurations is

$$A_C = \frac{-h_{fe} R_C}{R_S + h_{ie} + (2R_E + R_E')(1+h_{fe})}$$

while the i/p resistance of differential amplifier is

$$R_i = 2\left[R_S + h_{ie} + (1+h_{fe}) R_E'\right]$$

while the o/p resistance is equal to the collector resistance i.e;

$$R_o = R_C$$

Using r-parameters:-

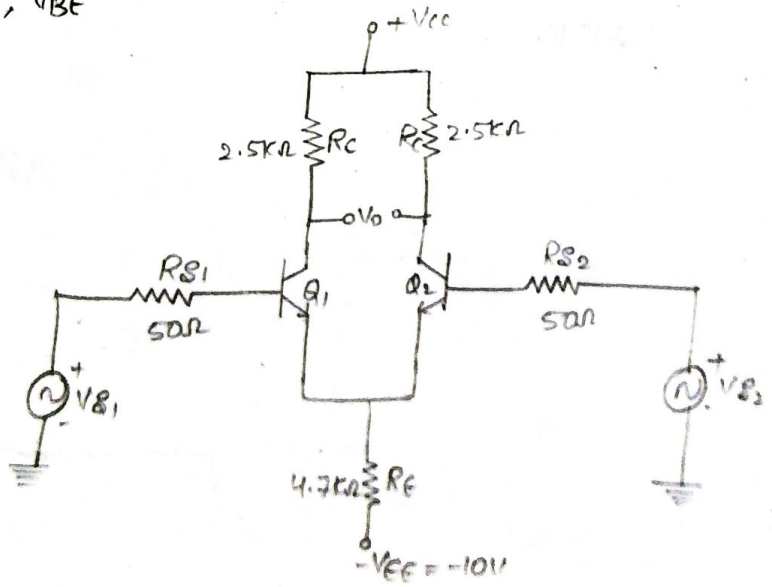
Using r-parameter analysis D.A is considered by replacing r_e with $r_e + R_E'$

S.NO	Type of Configuration	A_d	R_i	R_o
1.	DIBO	$A_d = \frac{R_c}{r_e + R_E'}$	$R_i = 2(r_e + R_E')\beta$	$R_o = R_c$
2.	DIUBO	$A_d = \frac{R_c}{2(r_e + R_E')}$	$R_i = 2(r_e + R_E')\beta$	$R_o = R_c$
3.	SIBO	$A_d = \frac{R_c}{r_e + R_E'}$	$R_i = 2(r_e + R_E')\beta$	$R_o = R_c$
4.	SIUBO	$A_d = \frac{R_c}{2(r_e + R_E')}$	$R_i = 2(r_e + R_E')\beta$	$R_o = R_c$

Problem :-

① For a D.A following fig. shows DIBO. (i) Determine the operating point values (ii) Determine the voltage gain (iii) i/p & o/p resistances (iv) the o/p voltage V_o if $V_{s_1} = 50mV_{p-p}$ and $V_{s_2} = 20mV_{p-p}$ (v) What is the max. o/p voltage without clipping? (vii) sketch the i/p and o/p waveforms and assume $h_{fe} = 100$, $V_{BE} = 0.7V$, $h_{ie} = 2.5K\Omega$

Sol:-



Given data is

$V_{cc} = 10V$

$V_{EE} = -10V$

(i) $I_E = \frac{V_{EE} - V_{BE}}{2R_E}$

$= \frac{10 - 0.7}{2(4.7 \times 10^3)} = 0.9873mA$

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$$I_c = \frac{h_{fe}}{1+h_{fe}} I_c$$

$$= \frac{100}{101} \times 0.984 = 0.9774 \text{ mA}$$

$$V_{CE} = V_{CC} + V_{BE} - I_C R_C$$

$$= 10 + 0.7 - 0.9774 \times 10^{-3} \times 2.2 \times 10^3$$

$$= 8.57 \text{ V}$$

(ii) $$A_d = \frac{h_{fe} R_C}{R_S + h_{ie}} = \frac{100 \times 2.2 \times 10^3}{50 + 2.5 \times 10^3} = 86.27$$

(iii) $$R_{in} = 2(R_S + h_{ie})$$

$$= 2(50 + 2.5 \times 10^3)$$

$$= 5.1 \text{ K}\Omega$$

$$R_o = R_C = 2.2 \text{ K}\Omega$$

(iv) $$V_o = A_d (V_{S_1} - V_{S_2})$$

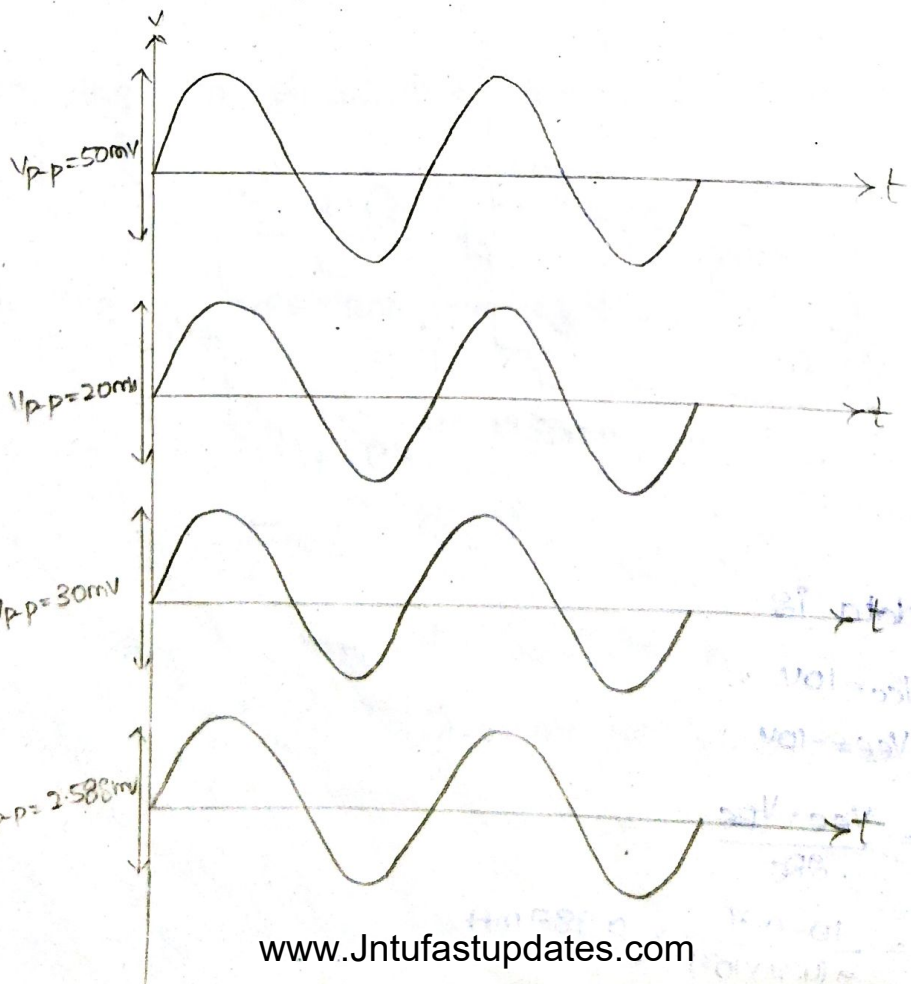
$$= 86.27 (50 - 20)$$

$$= 2.588 \text{ V}_{p-p}$$

(v) Max. voltage $= I_C R_C$

$$= 0.977 \times 10^{-3} \times 2.2 \times 10^3$$

$$= 2.15 \text{ V}.$$



* DC Analysis of Dual i/p unbalanced o/p D·A

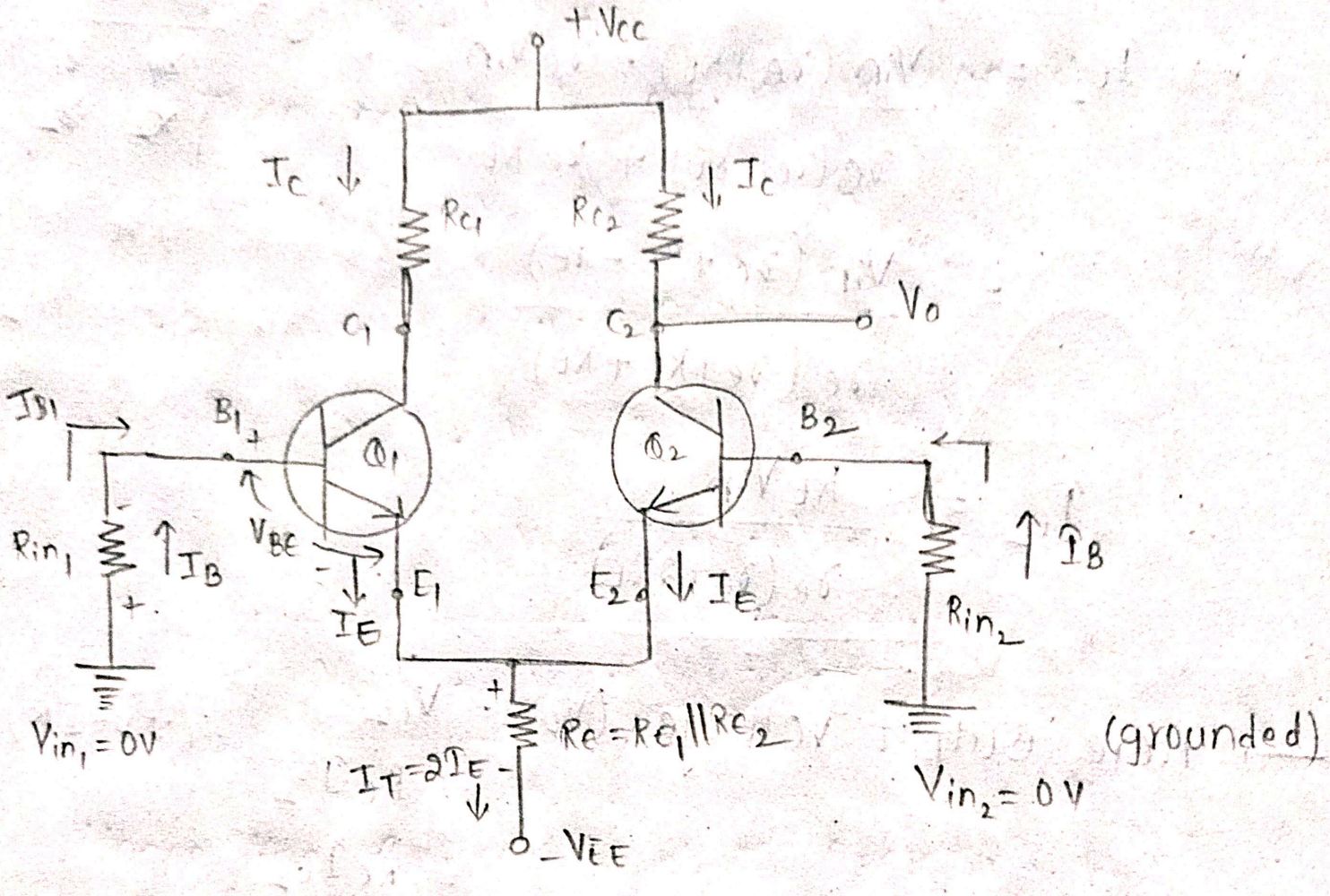


fig: Dual input unbalanced output Differential Amplifier

Here, $I_C \simeq I_E$, $I_B = \frac{I_E}{\beta_{dc}}$ ——— ①

We should determine operating point values (I_{CQ} & V_{CEQ})

Here, $R_{E_1} || R_{E_2} = R_E$

$R_{C_1} = R_{C_2} = R_C$

The magnitude of $V_{CC} = V_{EE}$

from the ckt, applying KVL loop to base to emitter voltage of Q_1 transistor then the eqn is

$$-R_{in} I_B - V_{BE} - R_E(2I_E) + V_{EE} = 0$$

$$\Rightarrow -R_{in} I_B - V_{BE} - 2R_E I_E + V_{EE} = 0$$

$$\rightarrow V_{EE} - V_{BE} = R_{in} I_B + 2R_E I_E$$

$$= R_{in} \frac{I_E}{\beta_{dc}} + 2R_E I_E \quad (\because \text{from } ①)$$

$$= I_E \left\{ \frac{R_{in}}{\beta_{dc}} + 2R_E \right\}$$

$$\therefore I_E = \frac{V_{EE} - V_{BE}}{2R_E + \frac{R_{in}}{\beta_{dc}}} \quad \text{——— } ②$$

$V_{BE} = 0.6\ V$ for silicon transistor

$= 0.2V$ for germanium transistor

In ②; $\frac{R_{in}}{\beta_{dc}} << 2R_E$, so neglect $\frac{R_{in}}{\beta_{dc}}$

$$\Rightarrow I_E = \frac{V_{EE} - V_{BE}}{2R_E} \quad (\because I_C \simeq I_E)$$

$$\therefore \boxed{I_{CQ} = I_E = \frac{V_{EE} - V_{BE}}{2R_E}}$$

Now, let us determine the V_{CE} value as I_C value is known and $I_E \simeq I_C$, then we can determine the collector current voltage (V_C) of Q_1 transistor.

$$V_C = V_{CC} - I_C R_C \quad \text{—— (3)}$$

Neglecting the drop voltage across the source resistance R_{in} we can say that voltage at the emitter of Q_1 is i.e

$$V_E = -V_{BE} \quad \text{—— (4)}$$

Then collector to emitter voltage is

$$V_{CE} = V_C - V_E \quad \text{—— (5)}$$

Sub (3) and (4) in Eq^n (6)

$$\Rightarrow V_{CE} = [V_{CC} - I_C R_C] - (-V_{BE})$$

$$= V_{CC} - I_C R_C + V_{BE}$$

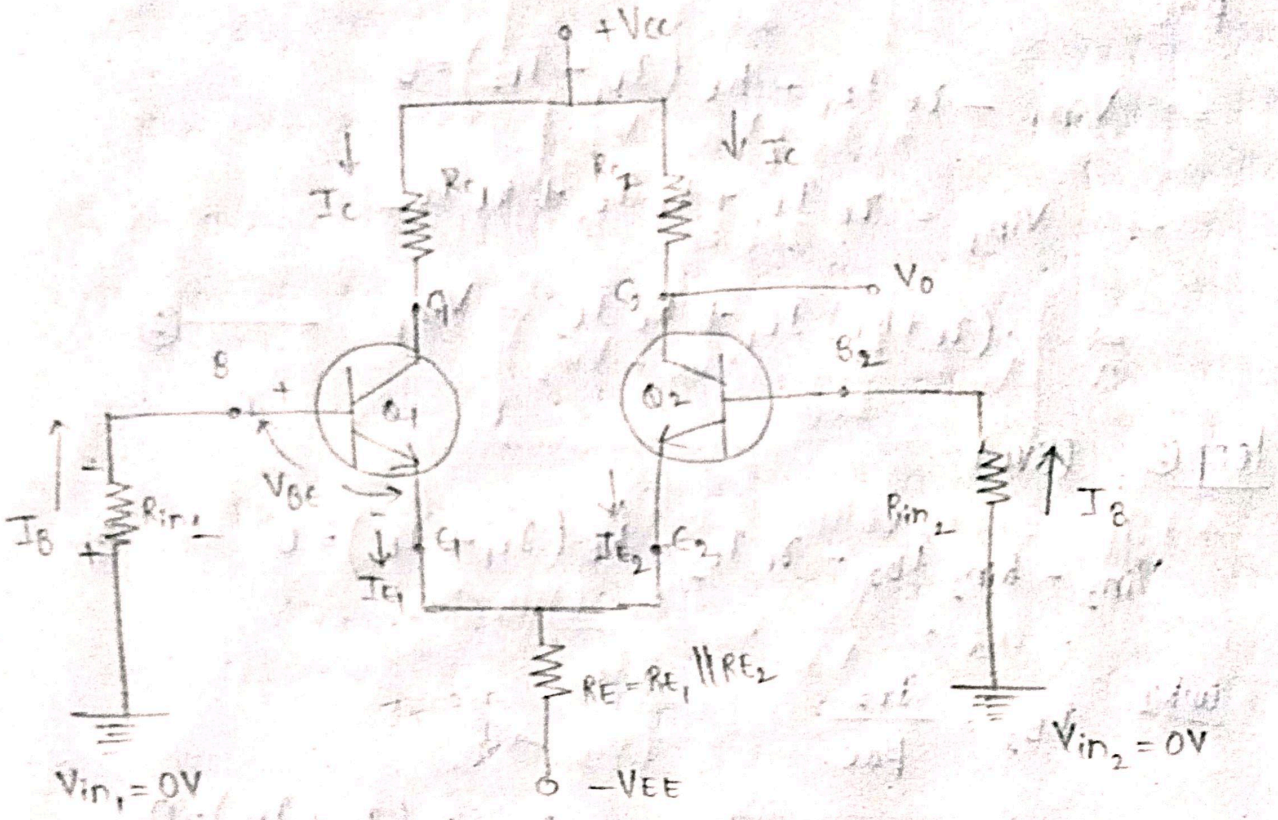
$$\therefore \boxed{V_{CEQ} = V_{CC} + V_{BE} - I_C R_C}$$

Hence the Quiscent point (or) Operating point values of a Dual input unbalanced output differential Amplifier, DC Analysis values are

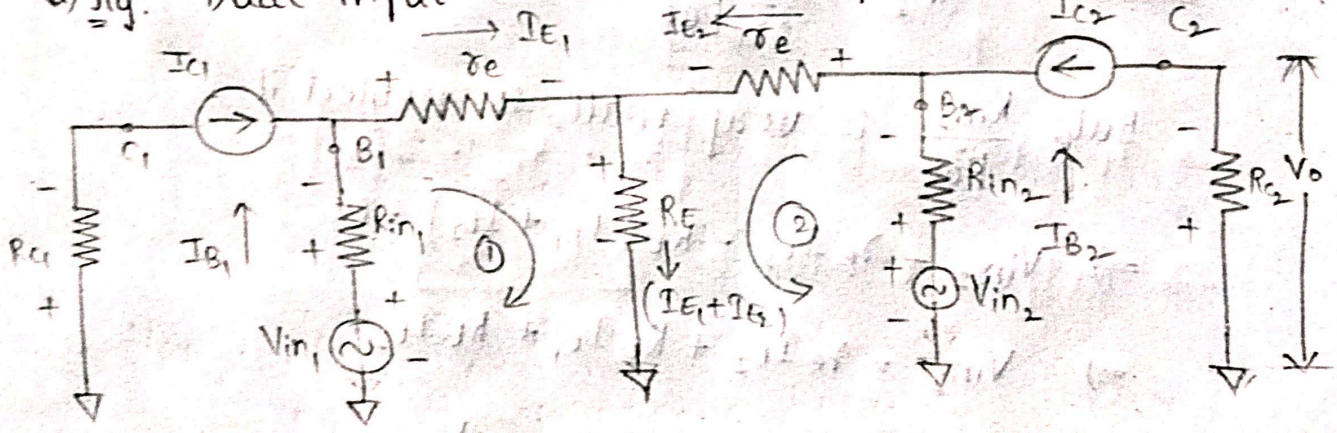
$$I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E}$$

$$V_{CEQ} = V_{CC} + V_{BE} - I_C R_C$$

* AC Analysis of Dual i/p unbalanced o/p D·A :-



(a) fig: Dual input unbalanced output D·A



(b) fig:- r-parameter equivalent to fig(a)

Apply KVL for loop ① and loop ②

loop ①:-

$$V_{in_1} - R_{in_1} I_{B_1} - r_e I_{E_1} - R_E (I_{E_1} + I_{E_2}) = 0 \quad \text{——} ①$$

w.k.t $\quad I_{B_1} = \dfrac{I_{E_1}}{\beta_{ac}} \quad (\because \text{ac-analysis})$

Then; $\quad V_{in_1} - R_{in_1} \dfrac{I_{E_1}}{\beta_{ac}} - r_e I_{E_1} - R_E (I_{E_1} + I_{E_2}) = 0$

①

$\frac{R_{in_1}}{\beta_{ac}}$ is very small, so neglect it

$\Rightarrow V_{in_1} - r_e I_{E_1} - R_E (I_{E_1} + I_{E_2}) = 0$

$\rightarrow V_{in_1} = r_e I_{E_1} + R_E I_{E_1} + R_E I_{E_2}$

$\Rightarrow (r_e + R_E) I_{E_1} + R_E I_{E_2} = V_{in_1}$ ——— (2)

Loop (2) :- (KVL)

$V_{in_2} - R_{in_2} I_{B_2} - r_e I_{E_2} - R_E (I_{E_1} + I_{E_2}) = 0$ ——— (3)

W.K.T $I_{B_2} = \frac{I_{E_2}}{\beta_{ac}}$

Then (3) :- $V_{in_2} - R_{in_2} \frac{I_{E_2}}{\beta_{ac}} - r_e I_{E_2} - R_E (I_{E_1} + I_{E_2}) = 0$

But, $\frac{R_{in_2}}{\beta_{ac}}$ is very small, so neglect it

$\Rightarrow V_{in_2} - r_e I_{E_2} - R_E (I_{E_1} + I_{E_2}) = 0$

$\rightarrow V_{in_2} = r_e I_{E_2} + R_E I_{E_1} + R_E I_{E_2}$

$\rightarrow (r_e + R_E) I_{E_2} + R_E I_{E_1} = V_{in_2}$

$\Rightarrow R_E I_{E_1} + (r_e + R_E) I_{E_2} = V_{in_2}$ ——— (4)

Consider:

(2) $\rightarrow$ $(r_e + R_E) I_{E_1} + R_E I_{E_2} = V_{in_1}$

(4) $\rightarrow$ $\because R_E I_{E_1} + (r_e + R_E) I_{E_2} = V_{in_2}$

X Y Z

Apply cramer's rule to above eqn's (2) & (4); we get

then:

$$I_{E_1} = \frac{\begin{vmatrix} V_{in_1} & -R_E \\ V_{in_2} & r_e + R_E \end{vmatrix}}{\begin{vmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{vmatrix}}$$

$$\rightarrow I_{E_1} = \frac{V_{in_1}(r_e + R_E) - R_E V_{in_2}}{(r_e + R_E)^2 - (R_E)^2} \quad \text{---------- (5)}$$

and:

$$I_{E_2} = \frac{\begin{vmatrix} r_e + R_E & V_{in_1} \\ R_E & V_{in_2} \end{vmatrix}}{\begin{vmatrix} r_e + R_E & R_E \\ R_E & r_e + R_E \end{vmatrix}}$$

$$\Rightarrow I_{E_2} = \frac{(r_e + R_E)V_{in_2} - R_E V_{in_1}}{(r_e + R_E)^2 - (R_E)^2} \quad \text{---------- (6)}$$

Here the output voltage, $V_O = V_{C_2}$

Since $V_{C_2} = -R_C I_{C_2} = -R_C I_{E_2}$ $(\because I_C \simeq I_E)$

$$\Rightarrow V_O = -R_C I_{E_2}$$

$$= -R_C \left[\frac{(r_e + R_E)V_{in_2} - R_E V_{in_1}}{(r_e + R_E)^2 - (R_E)^2} \right]$$

$$= R_C \left[\frac{R_E V_{in_1} - (r_e + R_E)V_{in_2}}{r_e^2 + R_E^2 + 2 r_e R_E - R_E^2} \right]$$

$$= R_C \left[\frac{R_E V_{in_1} - r_e V_{in_2} - R_E V_{in_2}}{r_e^2 + 2 R_E r_e} \right]$$

Here, $R_E >> r_e$, so neglect "r_e"

$$\rightarrow V_o = R_C\left[\frac{R_E V_{in_1} - R_E V_{in_2}}{2R_E r_e}\right]$$

$$= \frac{R_C R_E \left[V_{in_1} - V_{in_2}\right]}{2R_E r_e}$$

$$\therefore \boxed{V_o = \frac{R_C}{2r_e}\left(V_{in_1} - V_{in_2}\right)}$$

$\rightarrow$ Differential voltage Gain,

$$A_d = \frac{V_o}{V_d} = \frac{\frac{R_C}{2r_e}(V_{in_1} - V_{in_2})}{(V_{in_1} - V_{in_2})}$$

$$\therefore \boxed{A_d = \frac{R_C}{2r_e}}$$

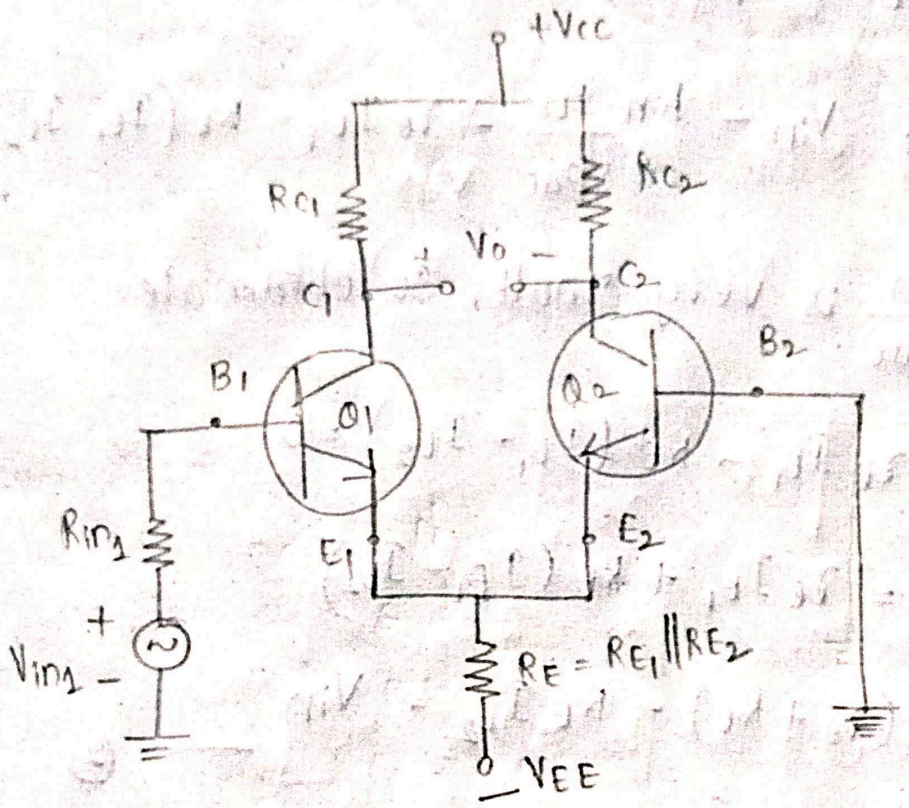
$\rightarrow$ Input resistance $\boxed{R_{i_1} = R_{i_2} = 2\beta_{ac} r_e}$

$\rightarrow$ Output resistance $\boxed{R_o = R_C}$

24/8/2020 mon

* Single input differential Amplifier - AC Analysis

Balanced output



ⓐ fig: single input balanced o/p Differential Amplifier

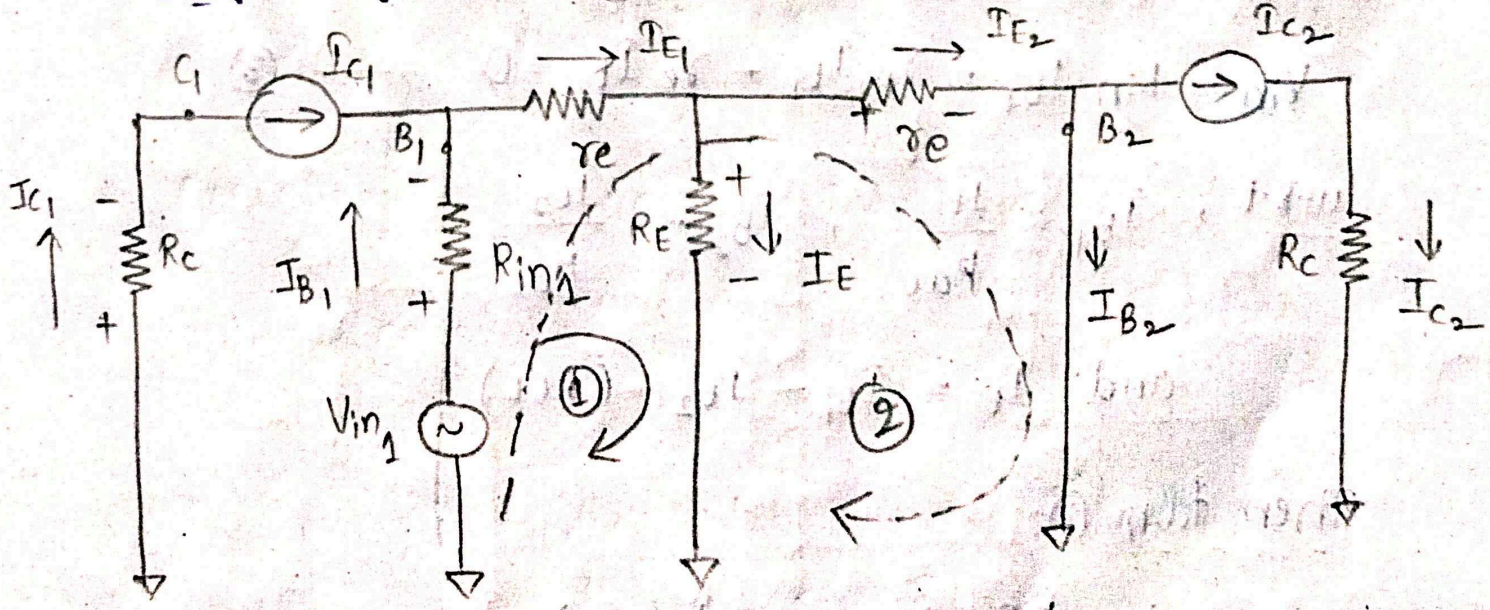


fig: (b) ÷ Equivalent to fig(a)

let $V_{in_1} \simeq V_{in}$, $R_{in_1} = R_{in}$

Applying KVL for loop ① and loop ② in fig (b)

loop ①:

$$V_{in} - R_{in} I_{B_1} - r_e I_{E_1} - R_E I_E = 0 \quad \text{——} ①$$

we know that;

$$I_{B_1} = \frac{I_{E_1}}{\beta_{ac}} \quad (\because \text{Ac analysis})$$

and $I_E = I_{E_1} - I_{E_2}$ (KCL)

now from ① ; $V_{in} - R_{in} \frac{I_{E_1}}{\beta_{ac}} - r_e I_{E_1} - R_E (I_{E_1} - I_{E_2}) = 0$

Here, $\frac{R_{in}}{\beta_{ac}}$ is very small, so eliminate.

$$\Rightarrow V_{in} - r_e I_{E_1} - R_E (I_{E_1} - I_{E_2}) = 0$$

$$\Rightarrow V_{in} = r_e I_{E_1} + R_E (I_{E_1} - I_{E_2})$$

$$\Rightarrow I_{E_1} (r_e + R_E) - R_E I_{E_2} = V_{in} \quad \text{——} ②$$

loop ②:

$$V_{in} - R_{in} I_{B_1} - r_e I_{E_1} - r_e I_{E_2} = 0 \quad \text{——} ③$$

w.k.t , $I_{B_1} = \frac{I_{E_1}}{\beta_{ac}}$, $I_{B_2} = \frac{I_{E_2}}{\beta_{ac}}$

and $I_E = I_{E_1} - I_{E_2}$ (KCL)

Then from ③:

$$V_{in} - \frac{R_{in}}{\beta_{ac}} I_{E_1} - r_e I_{E_1} - r_e I_{E_2} = 0$$

R_{in} is very small, so eliminate.

P_{ac}

$\rightarrow V_{in} - r_e I_{E_1} - r_e I_{E_2} = 0$

$\rightarrow r_e I_{E_1} + r_e I_{E_2} = V_{in}$ ——— (3)

Consider: (3) $\rightarrow (r_e + R_E) I_{E_1} - R_E I_{E_2} = V_{in}$

(4) $\rightarrow r_e I_{E_1} + r_e I_{E_2} = V_{in}$

By applying Cramer's rule:-

$$I_{E_1} = \frac{\begin{vmatrix} V_{in} & -R_E \\ V_{in} & r_e \end{vmatrix}}{\begin{vmatrix} r_e + R_E & -R_E \\ r_e & r_e \end{vmatrix}} \quad ; \quad I_{E_2} = \frac{\begin{vmatrix} r_e + R_E & V_{in} \\ r_e & V_{in} \end{vmatrix}}{\begin{vmatrix} r_e + R_E & -R_E \\ r_e & r_e \end{vmatrix}}$$

$$\rightarrow I_{E_1} = \frac{r_e V_{in} + R_E V_{in}}{r_e (r_e + R_E) + R_E r_e} \qquad I_{E_2} = \frac{V_{in}(r_e + R_E) - r_e V_{in}}{r_e (r_e + R_E) + R_E r_e}$$

$$= \frac{V_{in} (r_e + R_E)}{r_e (r_e + R_E + R_E)} \qquad = \frac{V_{in} (r_e + R_E - r_e)}{r_e (r_e + R_E + R_E)}$$

$$\therefore \boxed{I_{E_1} = \frac{V_{in} (r_e + R_E)}{r_e (r_e + 2R_E)}} \qquad \boxed{I_{E_2} = \frac{R_E V_{in}}{r_e (r_e + 2R_E)}}$$

$\rightarrow$ Output voltage $(V_o) = V_{C_2} - V_{C_1}$

$\Rightarrow V_o = R_C I_{C_2} - [-R_C I_{C_1}]$ $(\because V = IR)$

$R_{C_1} = R_{C_2} = R_C$

$= R_C I_{C_2} + R_C I_{C_1}$

$= R_C [I_{C_1} + I_{C_2}]$

$$\therefore \boxed{V_o = R_C [I_{C_1} + I_{E_2}]} \qquad (\because I_C \simeq I_E)$$

$$\rightarrow V_o = R_c \left[\frac{(r_e + R_e) V_{in}}{r_e (r_e + 2R_e)} + \frac{R_e V_{in}}{r_e (r_e + 2R_e)} \right]$$

$$= R_c \left[\frac{(r_e + R_e) V_{in} + R_e V_{in}}{r_e (r_e + 2R_e)} \right]$$

$$= R_c \left[\frac{(r_e + 2R_e) V_{in}}{r_e (r_e + 2R_e)} \right]$$

$$\therefore \boxed{V_o = \frac{R_c V_{in}}{r_e}}$$

$\rightarrow$ Differential Gain $(A_d) = \frac{V_o}{V_{in}}$

$$= \frac{R_c V_{in} / r_e}{V_{in}}$$

$$\therefore \boxed{A_d = \frac{R_c}{r_e}}$$

$\rightarrow$ Input resistance $\boxed{R_i = 2 \beta_{ac} r_e}$

$\rightarrow$ Output resistance $\boxed{R_{o_1} = R_{o_2} = R_c}$

* single i/p unbalanced output differential Amplifier - Ac Analysis

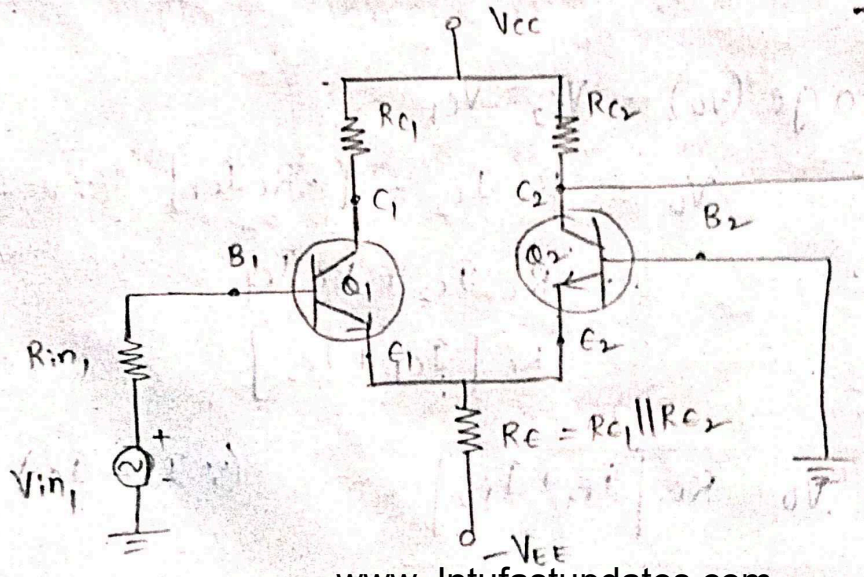
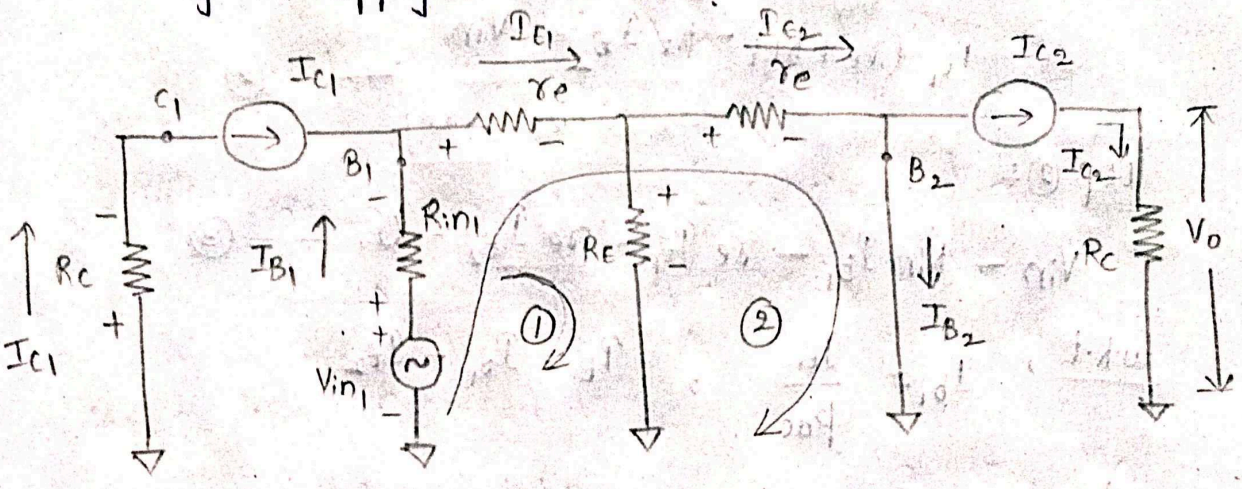
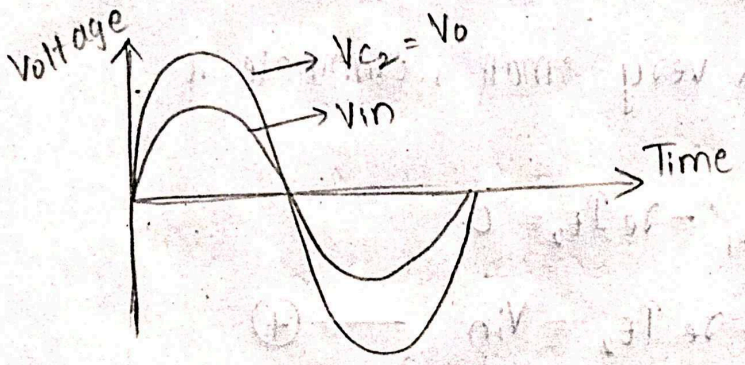


fig (a) - single i/p unbalanced o/p D.A

- It has less voltage gain
  There exist DC o/p voltage without any i/p signal apply



fig(b): equivalent r-parameter (π) to fig(a)



o/p voltage, $V_o = V_C$

$V_o = R_C I_{C_2} = R_C I_{E_2}$

$(\because I_C \simeq I_E)$

let $V_{in_1} \simeq V_{in}$, $R_{in_1} = R_{in}$

Applying KVL for loop ① and loop ② in fig(b):

loop ①:

$$V_{in} - R_{in} I_{B_1} - r_e I_{E_1} - R_E I_E = 0 \quad \text{——①}$$

w.k.t, $I_{B_1} = \frac{I_{E_1}}{\beta_{ac}}$ & $I_E = I_{E_1} - I_{E_2}$ (KCL)

now from ①: $V_{in} - R_{in} \frac{I_{E_1}}{\beta_{ac}} - r_e I_{E_1} - R_E (I_{E_1} - I_{E_2}) = 0$

Here, $\frac{R_{in}}{\beta_{ac}}$ is very small, so eliminate.

$\Rightarrow V_{in} - r_e I_{E_1} - R_E (I_{E_1} - I_{E_2}) = 0$

$\Rightarrow V_{in} = r_e I_{E_1} + R_E (I_{E_1} - I_{E_2})$

$\Rightarrow I_{E_1} (r_e + R_E) - R_E I_{E_2} = V_{in}$ ——— ②

loop ②:-

$V_{in} - R_{in} I_{B_1} - r_e I_{E_1} - r_e I_{E_2} = 0.$ ——— ③

w.k.t, $I_{B_1} = \frac{I_{E_1}}{\beta_{ac}}$, $I_E = I_{E_1} - I_{E_2}$

from ③:-

$V_{in} - \frac{R_{in}}{\beta_{ac}} I_{E_1} - r_e I_{E_1} - r_e I_{E_2} = 0.$

Since, $\frac{R_{in}}{\beta_{ac}}$ is very small, eliminate it.

$\Rightarrow V_{in} - r_e I_{E_1} - r_e I_{E_2} = 0.$

$\Rightarrow r_e I_{E_1} + r_e I_{E_2} = V_{in}$ ——— ④

Consider ② $\longrightarrow$ $I_{E_1} (r_e + R_E) - R_E I_{E_2} = V_{in}$

④ $\longrightarrow$ $I_{E_1} \cdot r_e + r_e I_{E_2} = V_{in}$

$\quad\quad\quad

$$\rightarrow I_{E_1} = \frac{V_{in}(r_e + R_E)}{r_e\left[r_e + R_E + R_E\right]}$$

$$\therefore \boxed{I_{E_1} = \frac{V_{in}(r_e + R_E)}{r_e(r_e + 2R_E)}}$$

and $$I_{E_2} = \frac{\begin{vmatrix} r_e + R_E & V_{in} \\ r_e & V_{in} \end{vmatrix}}{\begin{vmatrix} r_e + R_E & -R_E \\ r_e & r_e \end{vmatrix}}$$

$$\rightarrow I_{E_2} = \frac{V_{in}(r_e + R_E) - r_e V_{in}}{r_e(r_e + R_E) + r_e R_E}$$

$$= \frac{V_{in}(\cancel{r_e} + R_E - \cancel{r_e})}{r_e(r_e + R_E + R_E)}$$

$$\therefore \boxed{I_{E_2} = \frac{R_E V_{in}}{r_e(r_e + 2R_E)}}$$

$\rightarrow$ Here Output voltage $(V_o) = V_{C_2}$ $(\because V = IR)$

$$= R_C I_{C_2}$$

$$= R_C I_{E_2}$$

$$\Rightarrow V_o = R_C\left[\frac{R_E V_{in}}{r_e(r_e + 2R_E)}\right]$$

$$\Rightarrow V_o = R_C\left[\frac{\cancel{R_E} V_{in}}{r_e(2\cancel{R_E})}\right] \quad (\because R_E >> r_e ;\ \text{neglect } r_e)$$

$$\therefore \boxed{V_o = \frac{R_C V_{in}}{2r_e}}$$

(2 x 2) cramer's rule

$a_1x + b_1y = z_1$

$c_2x + d_1y = v$

$$x = \frac{\begin{vmatrix} z & b \\ v & d \end{vmatrix}}{\begin{vmatrix} a & b \\ c & d \end{vmatrix}}$$

$$y = \frac{\begin{vmatrix} a & z \\ c & v \end{vmatrix}}{\begin{vmatrix} a & b \\ c & d \end{vmatrix}}$$

→ Differential voltage gain,

$$A_d = \frac{V_o}{V_{in}} = \frac{R_c}{2 r_e}$$

→ Input resistance $R_i = 2\beta_{ac} r_e$

→ output resistance $R_o = R_c$