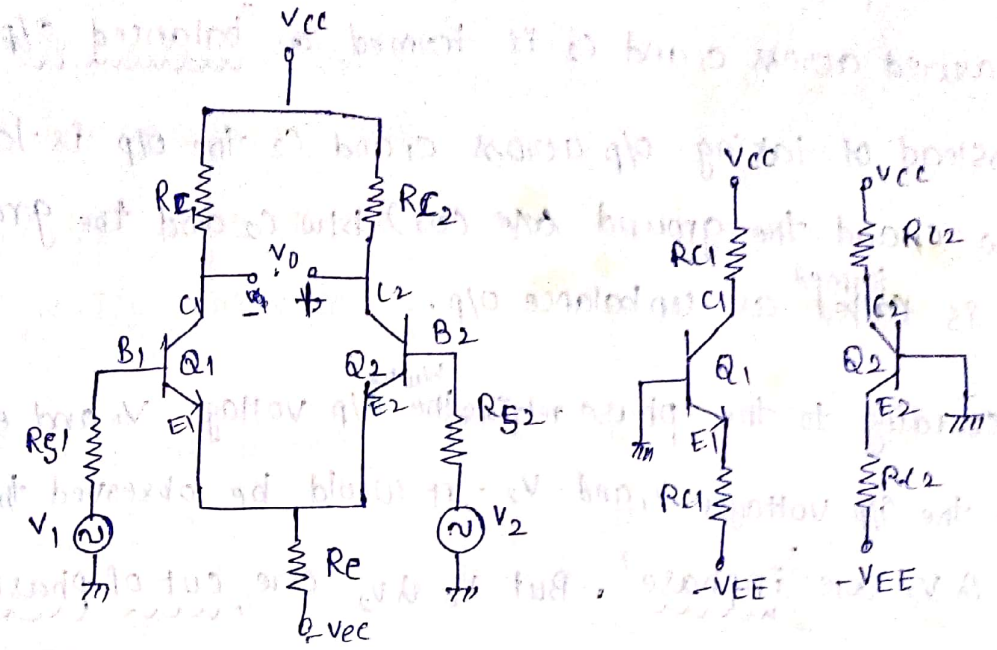
1. Integrated circuits

Differential amplifiers:-



→ The differential amplifier is i/p stage of operational amp. It is also called difference amplifier.

→ It amplifies the difference of 2 i/p signals.

→ The differential amplifier mainly consists of two identical transistor - either BJT (or) FET. whose emitters are directly connected as shown in fig.

→ The DC power supplies V_{CC} & V_{EE} are common to both transistors.

→ The collector ckt resistances are equal and the emitter resistance of the two transistors are replaced by single resistance.

→ From the fig V_1 & V_2 are the i/p voltages and the difference b/w them differential i/p voltages is the's differential voltages get amplified and appears as the o/p voltage V_o across the collector terminal C_1 and C_2.

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→ Since the collector resistors are equal and V_{cc} is common to both transistor.

∴ The DC potentials of C_1 and C_2 are equal. Hence the O/p measured across C_1 and C_2 is termed as "balanced O/p".

↔ Instead of taking O/p across C_1 and C_2 the O/p is taken b/w C_1 and the ground or b/w C_2 and the ground it is termed as unbalance O/p.

→ According to the phase relationship between the O/p voltage V_o and each of the i/p voltages V_1 and V_2. It would be observed the V_o & V_1 are 'inphase'. But V_o & V_2 are out of phase by 180°. Hence B_1 at which the i/p signal V_1 is applied is termed as "noninverting i/p terminal" and B_2 at which the i/p signal V_2 is applied is termed as inverting i/p terminal.

∴ We have $V_o = A(V_1 - V_2)$

Where A is the gain of the differential amp.

if V_1 is grounded then $V_1 = 0$.

∴ $\boxed{V_o = -AV_2}$.

if V_2 is grounded then $V_2 = 0$

∴ $\boxed{V_o = AV_1}$

from this relation it is cleared that V_o is inphase with V_1 But outof phase w.r.to V_2 by 180°.

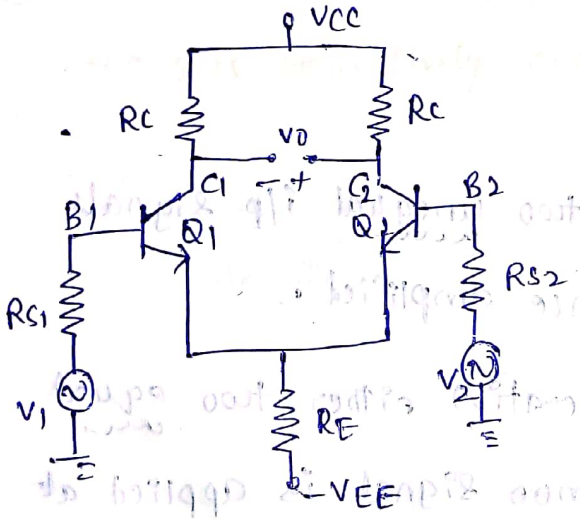
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Circuit configurations:

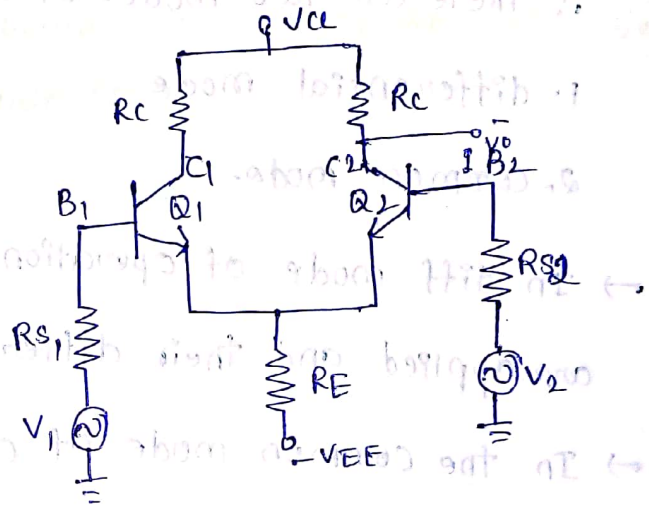
→ Depending upon how the i/p signals are applied and o/p is taken the practical diff amp may be classified as

1. Dual i/p Balanced o/p
2. Dual i/p unbalanced o/p
3. Single i/p Balanced o/p
4. Single i/p, unbalance o/p.

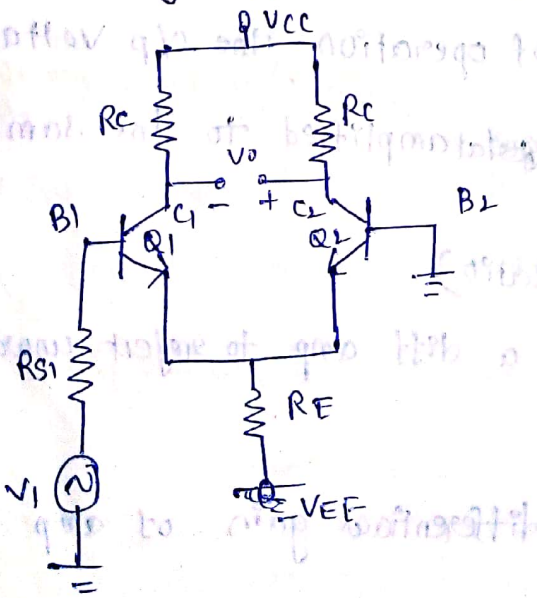
1. Dual i/p Balanced o/p.



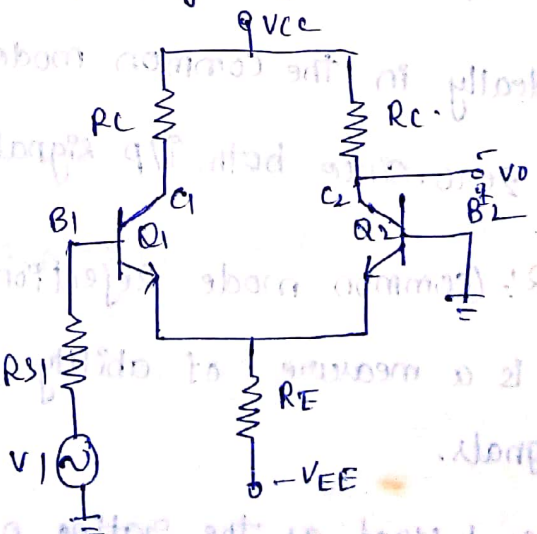
2. Dual i/p unbalanced o/p



3. Single i/p, Balanced o/p.



4. single i/p unbalanced o/p



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→ Depending upon the applications we have used any one of the configurations are adopted

modes of operation:-

→ The differential amp has two i/p terminals during the normal operations two signals may be applied at both terminals either two different signal may be applied (or) a common signal may be applied at both terminals.

∴ There are two modes of operation.

1. differential mode
2. common mode.

→ In diff mode of operation two unequal i/p signals are applied and their difference amplified.

→ In the common mode of operation either two equal signals are applied (or) a common signal is applied at both i/p terminals.

→ Ideally in the common mode of operation the o/p voltage is zero. Since both i/p signals are amplified to the same.

CMRR:- (Common mode Rejection Ratio)

It is a measure of ability of a diff amp to reject unwanted i/p signals.

→ It is defined as the ration of differential gain of amp to the common mode gain.

$$CMRR = \frac{Ad}{Ac}$$

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where Ad is the differential mode gain
Ac is the common mode gain.

→ Ideally Ac = 0, but Ad has the finite value hence CMRR is infinite value being a ratio of two gains CMRR is purely a number having no dimensions.

→ The CMRR is also be expressed in decibles i.e,

$$CMRR = 20\log_{10}\left(\frac{Ad}{Ac}\right)$$

PJ Let in practical case the calculated values of Ad & Ac will be 6000 & 15 respectively. Calculate CMRR

Gi.T

$Ad = 6000$

$Ac = 15$

$CMRR = \frac{6000}{15} = 400$

$CMRR = 20\log_{10}(400)$

$= 52.04$ dB

Analysis of diff amp:-

→ The analysis of diff amp consists in the evaluation of ckt parameters like voltage gain, i/p resistance, o/p resistance

voltage gain:- It is also called diff voltage gain.

It is defined as

$$Ad = \frac{V_o}{V_{id}}$$

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where v_{i1} and v_{i2} are the i/p voltages apply at the inverting and noninverting i/p terminals

v_o is the o/p voltage & v_{id} is the differential i/p voltage

i/p resistance:- It is also called diff i/p resistance

→ It is defined as the equivalent resistance that would be measure at any one of the i/p terminals with other terminal grounded

→ It is denoted as R_{i1} (or) R_{i2}.

$$R_{i1} = \frac{v_{i1}}{i_{b1}} \quad \text{where } v_{i2} = 0.$$

$$R_{i2} = \frac{v_{i2}}{i_{b2}} \quad \text{where } v_{i1} = 0$$

o/p resistance:- The equalent resistance that to be measure at either of collector terminals w.r.to ground.

It is denoted as R_{o1} (or) R_{o2}.

⇒ The analysis of diff amp types can be devided into 2 types

1. Dc analysis
2. Ac analysis

1. Dc analysis:-

→ The DC analysis of the diff amp is used to obtain Q-point (or) Dc bias point.

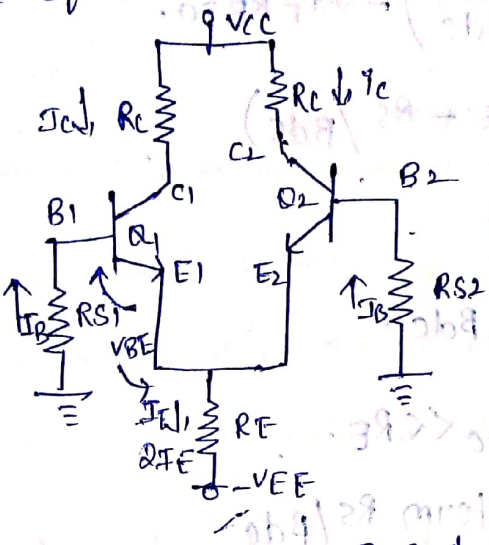
let I_{CQ} = Quecent collector current.

V_{CEQ} = Quecent collector to emitter voltage.

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→ The DC equivalent ckt can be obtained by setting the i/p voltages V_{i1} and V_{i2} is zero.

→ ∴ The equivalent ckt will be



→ Since the transistors Q_1 and Q_2 are identical, source resistance are equal.

$$R_{S1} = R_{S2} = R_S$$

→ In the ckt is symmetrical, the collector currents are equal, the emitter currents are also be equal and the collector to emitter voltages of both transistors are same. Hence in order to determine the Q-point values it is necessary to consider any one half of the ckt.

To find I_{CQ}:-

Considering the left portion of the ckt we have,

$$-R_S I_B - V_{BE} - 2I_E R_E = -V_{EE}$$

By applying KVL to the base to emitter,

$$\therefore V_{EE} - V_{BE} - R_S I_B - 2I_E R_E = 0$$

we have $I_B = \frac{I_C}{\beta_{dc}}$

where β_{dc} is current amplification factor.

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we have $I_C \simeq I_E$

when ever the transistor operates in CE mode.

$$\therefore V_{EE} - V_{BE} - R_S\left(\frac{I_E}{\beta dc}\right) - 2I_E R_E = 0.$$

$$V_{EE} - V_{BE} = I_E\left(2R_E + R_S/\beta dc\right)$$

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E + R_S/\beta dc}.$$

usually choosen $R_S/\beta dc << R_E$.

$\therefore$ We can neglect the term $R_S/\beta dc$

$$\boxed{I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E}}$$

→ To find V_{CEQ}:-

From the ckt $V_{CEQ} = V_C - V_E$

But $V_C = V_{CC} - I_C R_C$

$V_E \simeq -V_{BE}$ (We can neglect the source resistance of the transistor Q_1)

$$V_{CE} = V_{CC} - I_C R_C - (-V_{BE})$$

$$\boxed{V_{CEQ} = V_{CC} + V_{BE} - I_C R_C}$$

for both transistors Q_1 and Q_2 the Q-point values are

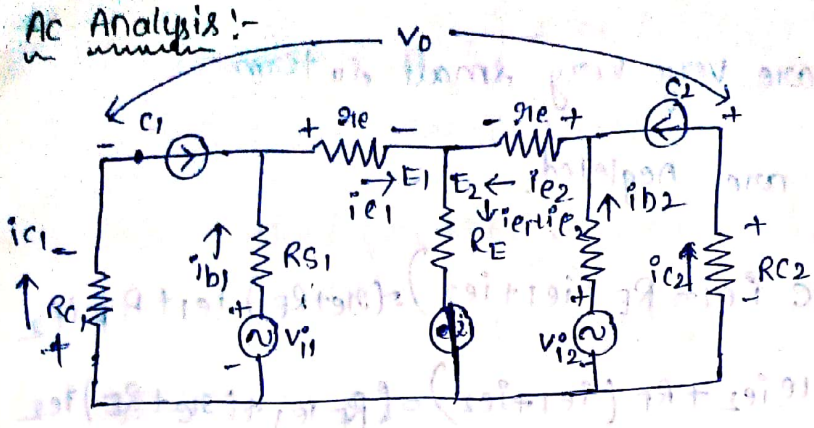
$$\boxed{I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E}}$$

$$\boxed{V_{CEQ} = V_{CC} + V_{BE} - I_C R_C}$$

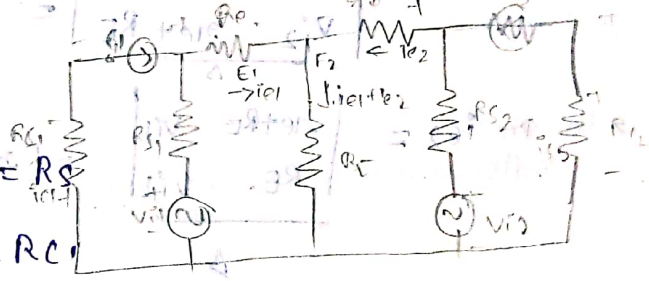
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Ac Analysis :-



→ We shall first consider the dual i/p balanced o/p configurat in order to obtained the Ac equivalent ckt the Dc voltages +vcc and -vcc are said to be zero and each of the transistors are replaced by its equivalent re model as shown in fig;



→ From the ckt $R_{S1} = R_{S2} = R_S$

$R_{C1} = R_{C2} = R_C$

differential voltage gain:-

→ Applying KVL to loops 1 and 2 we can get

$$V_{i1} - R_S i_{b1} - r_e i_{e1} - R_E (i_{e1} + i_{e2}) = 0 \quad \text{---(1)}$$

$$V_{i2} - R_S i_{b2} - r_e i_{e2} - R_E (i_{e1} + i_{e2}) = 0 \quad \text{---(2)}$$

→ we have $i_{b1} = \frac{i_{c1}}{\beta_{ac}} = \frac{i_{e1}}{\beta_{ac}}$ $\left[i_{c1} = i_{e1}\right]$

similarly $i_{b2} = \frac{i_{c2}}{\beta_{ac}} = \frac{i_{e2}}{\beta_{ac}}$ $\left[i_{c2} = i_{e2}\right]$

sub the values of i_{B1} and i_{B2} in the above eqns we get

$$V_{i1} - R_S \left(\frac{i_{e1}}{\beta_{ac}}\right) - r_e i_{e1} - R_E (i_{e1} + i_{e2}) = 0$$

$$V_{i2} - R_S \left(\frac{i_{e2}}{\beta_{ac}}\right) - r_e i_{e2} - R_E (i_{e1} + i_{e2}) = 0$$

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→ In practice $\frac{R_s}{\beta_{ac}}$ are very very small so term containing R_s/β_{ac} are neglected.

$$\therefore V_{i1} = r_e i_{e1} + R_E(i_{e1}+i_{e2}) = (r_e+R_E) i_{e1} + R_E i_{e2}$$

$$V_{i2} = r_e i_{e2} + R_E(i_{e1}+i_{e2}) = R_E i_{e1} + (r_e+R_E) i_{e2}$$

→ Applying crammers rule to evaluate i_{e1} and i_{e2}

$$\therefore \Delta = \begin{vmatrix} r_e+R_E & R_E \\ R_E & r_e+R_E \end{vmatrix}$$

$$i_{e1} = \frac{\begin{vmatrix} V_{i1} & R_E \\ V_{i2} & r_e+R_E \end{vmatrix}}{\Delta} = \frac{V_{i1}(R_E+r_e) - R_E V_{i2}}{(r_e+R_E)^2 - R_E^2} \quad \text{— (3)}$$

$$i_{e2} = \frac{\begin{vmatrix} r_e+R_E & V_{i1} \\ R_E & V_{i2} \end{vmatrix}}{\Delta} = \frac{(r_e+R_E)V_{i2} - V_{i1}R_E}{(r_e+R_E)^2 - R_E^2} \quad \text{— (4)}$$

we have the O/p voltage $V_o = V_{c1} - V_{c2}$

$$= i_{c1}R_{c1} - i_{c2}R_{c2} \quad \left(R_{c1} = R_{c2} = R_c,\ i_{c1} = i_{e1},\ i_{c2} = i_{e2} \right)$$

$$= R_c(i_{c1} - i_{c2})$$

$$= R_c(i_{e1} - i_{e2})$$

Sub the values of i_{e1} and i_{e2} in the above eqn get

$$V_o = R_c(i_{e1} - i_{e2})$$

$$= R_c\left[\frac{V_{i1}r_e + V_{i1}R_E - R_E V_{i2} - r_e V_{i2} - R_E V_{i2} + V_{i1}R_E}{(r_e+R_E)^2 - R_E^2}\right]$$

$$= R_c\left[\frac{V_{i1}r_e + 2V_{i1}R_E - 2R_E V_{i2} - r_e V_{i2}}{(r_e+R_E)^2 - R_E^2}\right]$$

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$$= R_C \left[\frac{r_e(v_{i1}-v_{i2}) + R_E(v_{i1}-v_{i2}) + R_E(v_{i1}-v_{i2})}{(r_e+R_E)^2 - R_E^2} \right]$$

$$= R_C \left[\frac{(r_e+2R_E)+(v_{i1}-v_{i2})}{r_e(r_e+2R_E)} \right] = \frac{R_C}{r_e}(v_{i1}-v_{i2})$$

$$v_o = \frac{R_C}{r_e} v_{id}$$

$$v_o/v_{id} = \frac{R_C}{r_e}$$

→ The diff voltage gain

$$A_d = \frac{R_C}{R_E}$$

differential i/p resistance:-

→ The equivalent resistance that can be measured at any one of the i/p terminal, i/p and other terminal must be grounded.

$$R_{i1} = \left| \frac{v_{i1}}{i_{b1}} \right|_{v_{i2}=0}$$

$$R_{i2} = \left| \frac{v_{i2}}{i_{b2}} \right|_{v_{i1}=0}$$

$$i_{b1} = \frac{i_{e1}}{\beta_{ac}} = \frac{i_{e1}}{\beta_{ac}}$$

sub i_{b1} value in R_{i1}

$$R_{i1} = \left| \frac{v_{i1}}{i_{e1}/\beta_{ac}} \right| \Rightarrow \frac{\beta_{ac} v_{i1} [r_e(r_e+2R_E)]}{v_{i1}(r_e+R_E) - v_{i2}R_E}$$

In practice $R_E >> r_e$.

$\therefore r_e + 2R_E \simeq 2R_E$

$r_e + R_E \simeq R_E$

$$R_{i1} = \frac{\beta_{ac} v_{i1} r_e [2R_E]}{v_{i1} R_E - v_{i2} R_E} = 2\beta_{ac} r_e$$

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similarly it can be shown that

~~2βac RE~~ 2 βac r_{ie}

hence diff i/p resistance at either of the i/p terminal is given as

$$R_{i1} = 2\beta_{ac} r_{ie}$$

where $r_e = \frac{26mV}{I_E}$

O/p resistance:-

→ It is eq resistance than can be measure at either of the collector terminal

∴ O/p resistance at C_1 = $R_{O1} = R_{C1}$

O/p resistance at C_2 = $R_{O2} = R_{C2}$.

But $R_{C1} = R_{C2} = R_C$.

$$\therefore R_{O1} = R_{O2} = R_C$$

→ In the Ac analysis the transistors are replaced by hybrid model instead of r_{ie} model. It can be described as

$$A_d = \frac{h_{fe} R_C}{R_S + h_{ie}}$$

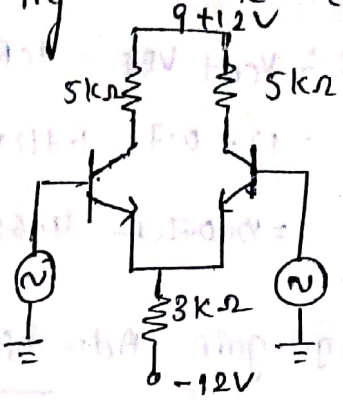
diff i/p impedence:-

$$R_i = 2(R_S + h_{ie})$$

O/p impedence:- $R_O = R_C$.

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P] For the diff amp as shown in fig determine I_{CQ} and V_{CEQ}. Assume silicon transistors.



$$I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E}$$

$$= \frac{12V - 0.7}{2(3)10^3}$$

$$= 1.88 \times 10^{-3}$$

$$= 1.88 \text{ mA}$$

$$V_{CEQ} = V_{CC} + V_{BE} - I_C R_C$$

$$= 12 + 0.7 - 1.88 \times 5 \times 10^3 .$$

$$= 12.07 - 1.88 \times 5 \times 10^{-3}$$

$$= 3.25 \text{ V}$$

→ For the dual i/p balanced o/p diff amp with $h_{fe} = 100$ for silicon transistors used. find the Q-point values and diff voltage gain, diff i/p impedence and o/p impedence.

Given $h_{fe} = 100$

$R_C = 4.7k\Omega$

$R_E = 3.3k\Omega$

$R_{S1} = R_{S2} = 100\Omega$.

$V_{CC} = 12V$, $h_{ie} = 1.4k\Omega$ $V_{EE} = 12$.

Soln

$$I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E}$$

$$= \frac{12 - 0.7}{2(3.3 \times 10^3)}$$

$$= 1.712 \text{ mA}$$

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$V_{CEQ} = V_{CC} + V_{BE} - I_C R_C$

$= 12 + 0.7 - 1.712 \times 10^{-3} \times (4.7 \times 10^3)$

$= 4.65\ V$

voltage gain $A_d = \dfrac{h_{fe} R_C}{R_s + h_{ie}}$

$= \dfrac{100 \times 4.7 \times 10^3}{\frac{4.7 \times 10^3}{100} + 1.4 \times 10^3}$

$= 313.33$

i/p impedence $R_i = 2(R_s + h_{ie})$

$= 2(100 + 1.4 \times 10^3)$

$= 1500 \times 2 = 3000 = 3K\Omega$

o/p impedence $R_o = R_C$

$R_o = 4.7\ K\Omega$

Other ckt configurations :-

→ We consides a dual i/p balanced o/p diff amp for obtaining the Q-point values like I_{CQ} V_{CEQ} these parameters are same in respect to other 3 ckt configuration since the biasing arrangement is the same for all ckt configuration

→ ∴ The Dc analysis follows the exactly the same Q-point values are obtained.

→ Hence for the single i/p unbalanced o/p diff amp, single i/p balanced o/p diff amp, the dual i/p unbalanced diff amp con-figuration we can get

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$$I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E}$$

$$V_{CEQ} = V_{CC} + V_{BE} - I_C R_C$$

→ The AC analysis for single i/p balanced o/p diff amp

$$A_d = \frac{R_C}{r_e} \qquad R_i = 2\beta_{ac} r_e \qquad R_o = R_C$$

→ for the single i/p unbalanced o/p diff amp.

$$A_d = \frac{R_C}{2r_e}, \quad R_i = 2\beta_{ac} r_e, \quad R_o = R_C$$

→ for the dual i/p unbalanced o/p diff amp

$$A_d = \frac{R_C}{2R_e} \qquad R_i = 2\beta_{ac} r_e \qquad R_o = R_C$$

→ the above results can be summerised as follows

configuration	voltage gain	i/p resistance	o/p resistance
1. single i/p balanced o/p	$A_d = R_C/R_E$	$R_i = 2\beta_{ac} r_e$	$R_o = R_C$
2. single i/p unbalance o/p	$A_d = \frac{R_C}{2r_e}$	$R_i = 2\beta_{ac} r_e$	R_C
3. dual i/p balanced o/p	R_C/r_e	$2\beta_{ac} r_e$	R_C
4. dual i/p unbalanced o/p	$\frac{R_C}{2r_e}$	$2\beta_{ac} r_e$	R_C

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→ The o/p voltage V_o for unbalanced configuration

$V_o = V_{c1}$ (or) V_{c2}

$V_o = V_{c1}$

$= I_{c1} R_{c1}$

$= I_{e1} R_{c1}$

$= R_c I_{e1}$

$= R_c \left[\frac{V_{i1}(r_e + R_E) - V_{i2} R_E}{r_e (r_e + 2R_E)} \right]$

In practice

$R_E >> r_e$

$r_e + R_E \simeq R_E$

$r_e + 2R_E \simeq 2R_E$

$= R_c \left[\frac{V_{i1} R_E - V_{i2} R_E}{r_e (2R_E)} \right]$

$= R_c \left[\frac{R_E (V_{i1} - V_{i2})}{r_e 2R_E} \right]$

$V_o = \frac{R_c}{2R_E} (V_{i1} - V_{i2})$

$$\frac{V_o}{V_{id}} = \frac{R_c}{2R_E}$$

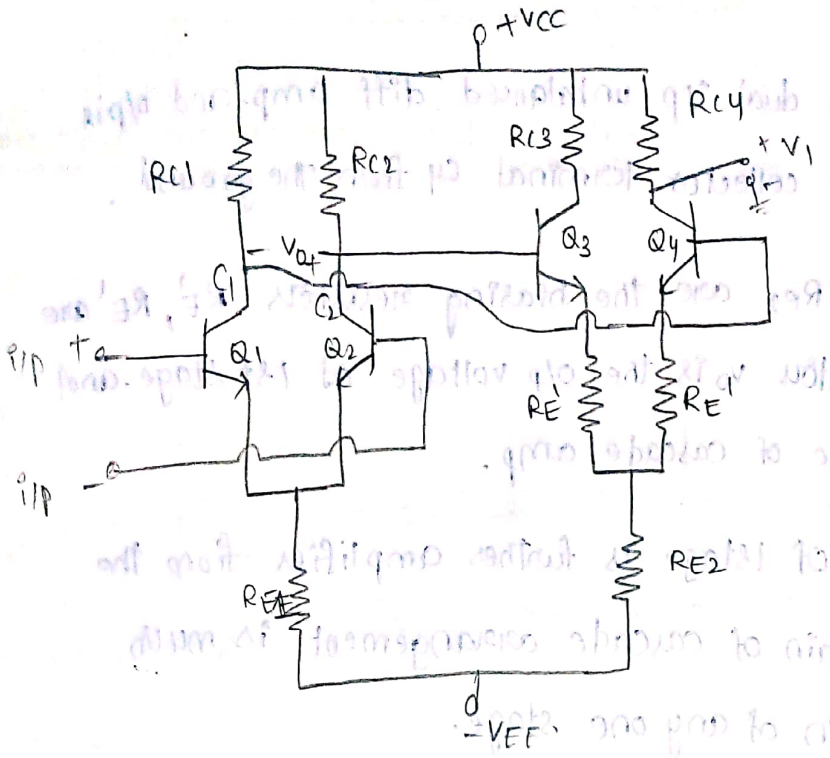
→ From the table reveals that for the diff i/p resistance is the same for all ckt configurations

→ The o/p resistance is the same for all ckt configurations.

→ The diff voltage gain of an unbalanced o/p ckt configuration is half of the voltage gain of a balanced o/p configuration.

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Cascading of diff amp:-



→ In the differential mode of operation the difference of the i/p signals at the noninverting and inverting terminals as amplified o/p and

→ The amplified o/p is taken across the collector terminals with a single stage the voltage gain is limited when larges voltage gains are needed. It is common practice to arrange several stages in cascade. such that the o/p of one stage forms the i/p to the next stage.

→ The overall voltage gain of several stages in cascade is given by the product of the individual stage gains.

→ Let us consider a two stage cascaded diff amp is shown in fig.

→ From the fig it is seen that the 1st stage is a dual i/p

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is the amplified o/p and it is applied to the 2nd stage transistors.

→ The 2nd stage is a dual i/p unbalanced diff amp. and o/p is taken across the collector terminal cy from the ground.

→ From the ckt R_{e1}, R_{e2} are the biasing resistors R_E', R_E' are the sampling resistors v_0 is the o/p voltage of 1st stage. and V_1 is the o/p voltage of cascade amp.

→ The amplified o/p of 1stage is further amplifies from the overall voltage gain of cascade arrangement is much larger than the gain of any one stage.

→ Depending on the total gain needed several stages may be cascaded it is essential that for proper functioning of cascading the transistors used in differential stages are properly matched and DC biasing of the transistors is provided.

→ &

Swamping resistors :-

→ The dependency of voltage gain R_E can be minimized by using additional resistors R_{e1}. In the emitter ckts of transistor Q_1 and Q_2 these resistors are termed as swamping resistors

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