

UNIT-III

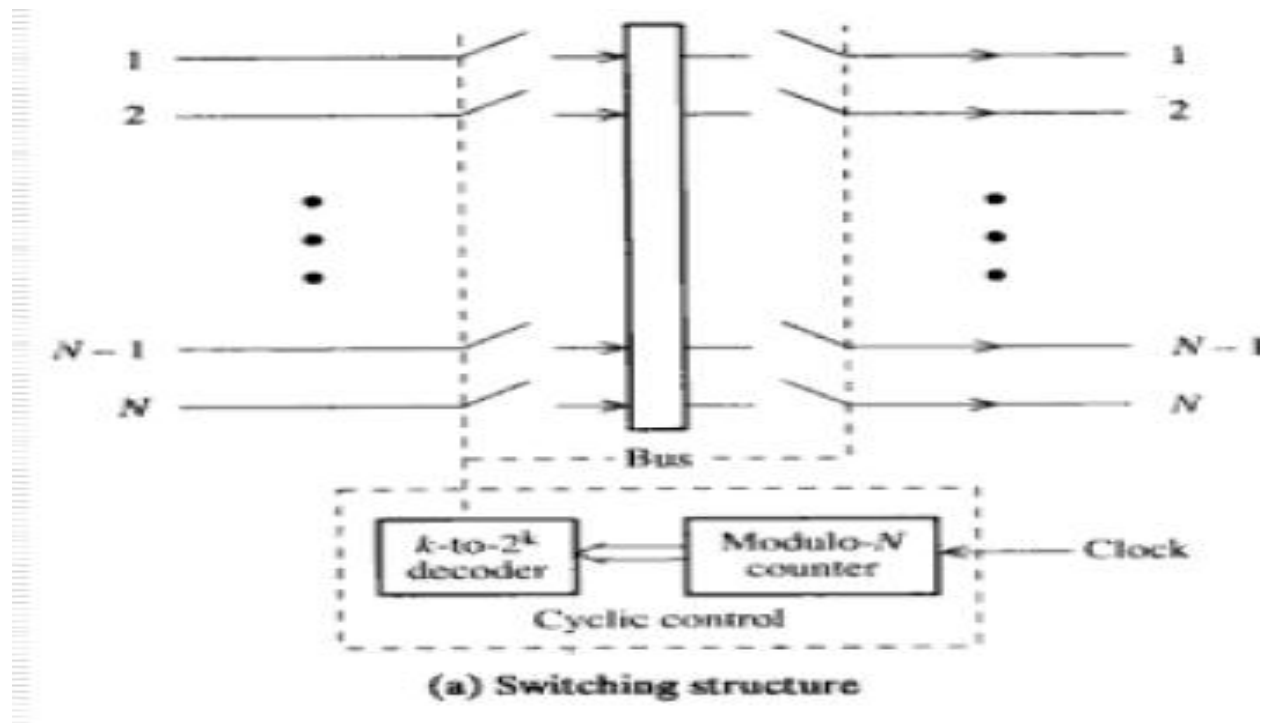
Time Division Switching

3.1 Introduction

- The switching scheme used by the electronic switching systems may be either Space Division Switching or Time Division Switching
- **Space Division Switching**
 - **Single-stage:** a crosspoint switching element is used to establish a specific connection between two subscribers.
 - **Multi-stage:** A conversation could be established via any one of the many alternative paths. A crosspoint is usable for establishing more than one connection. It is sharable among many subscribers.
- **Time Division Switching**
 - In digital transmission, sampled values of speech are sent as pulse amplitude modulated (PAM) values or pulse code modulated (PCM) binary words.
 - Features of PAM/PCM signal
 - Discrete in time domain
 - Transmission of PAM/PCM signal
 - Multiplexing
 - Periodical time slots

3.2 Basic Time Division Space Switching

- A sample $N \times N$ time division space switch is shown in below figure.



- The time division space switch can be represented in an equivalent form as a two stage network with $N \times 1$ and $1 \times N$ switching matrices for the first and second stages respectively as shown in below figure.

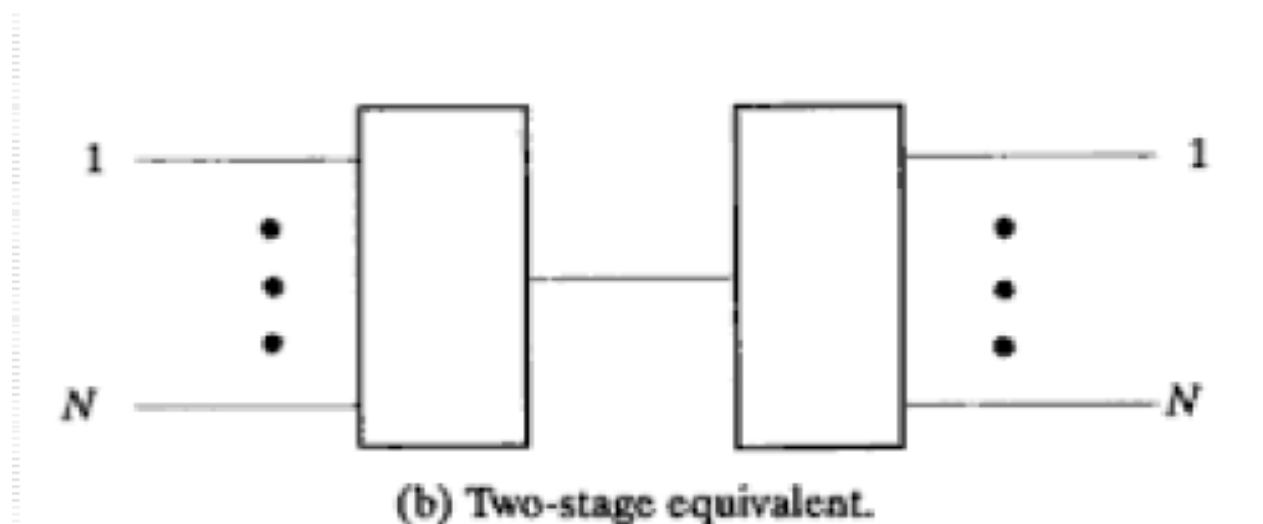


Fig. 6.1 Simple PAM time division switching.

- The network has one link interconnecting the two stages.
- Each inlet/outlet is a single speech circuit corresponding to a subscriber line. The speech is carried as PAM analog samples or PCM digital samples.
- When PAM samples are switched in a time division manner, the switching is known as analog time division switching
- If PCM binary samples are switched, then the switching is known as digital time division switching.
- In figure, the interconnecting link is shown as a bus to which a chosen inlet-outlet pair can be connected by a suitable control mechanism and the speech sample transferred from the inlet to the outlet.
- When PAM samples are switched, the bus is analog in nature and if the binary samples are switched, a digital bus is used.
- The number of simultaneous conversations, SC can be supported on a network of this kind is inversely proportional to the time required to select and connect an inlet-outlet pair and transfer the speech sample from the inlet to the outlet and is given by

$$SC = 125/t_s$$

➤ **Control mechanisms:**

- Cyclic control in synchronism
 - Input-controlled / Input-driven
 - Output-controlled / Output-driven
- **Cyclic control in synchronism**
- The selection of inlet/outlet is controlled dynamically. The simplest form of control is to select the inlets and outlets in a cyclic manner in synchronism.
- In this case, there is a fixed one to one correspondence between the inlets and the outlets.
- Suppose a cycle starts at inlet/outlet 1 and proceeds as 2, 3, 4, ...N, the next cycle as 1, 2, 3, ...N and so on, then inlet i is always connected to outlet i. in effect there is no switching in the true sense except that a single switching element is being shared by all the connections.
- The cyclic control is organised using a modulo-N counter and a k-to- 2^k decoder as shown in above figure.

- N and k are related by the equation

$$\lceil \log_2 N \rceil = k$$

- Where the symbol $\lceil \quad \rceil$ is a ceiling function that gives the lowest integer equal to or higher than the quantity inside the symbol.
- All the inlets/outlets are scanned within the 125 μ s, the switching capacity (SC) of the network is the same as the number of inlets or outlets in the system and the switch is called nonblocking. But it lacks full availability as it is not possible to connect any inlet to any outlet.
- **Input-controlled / Input-driven:**

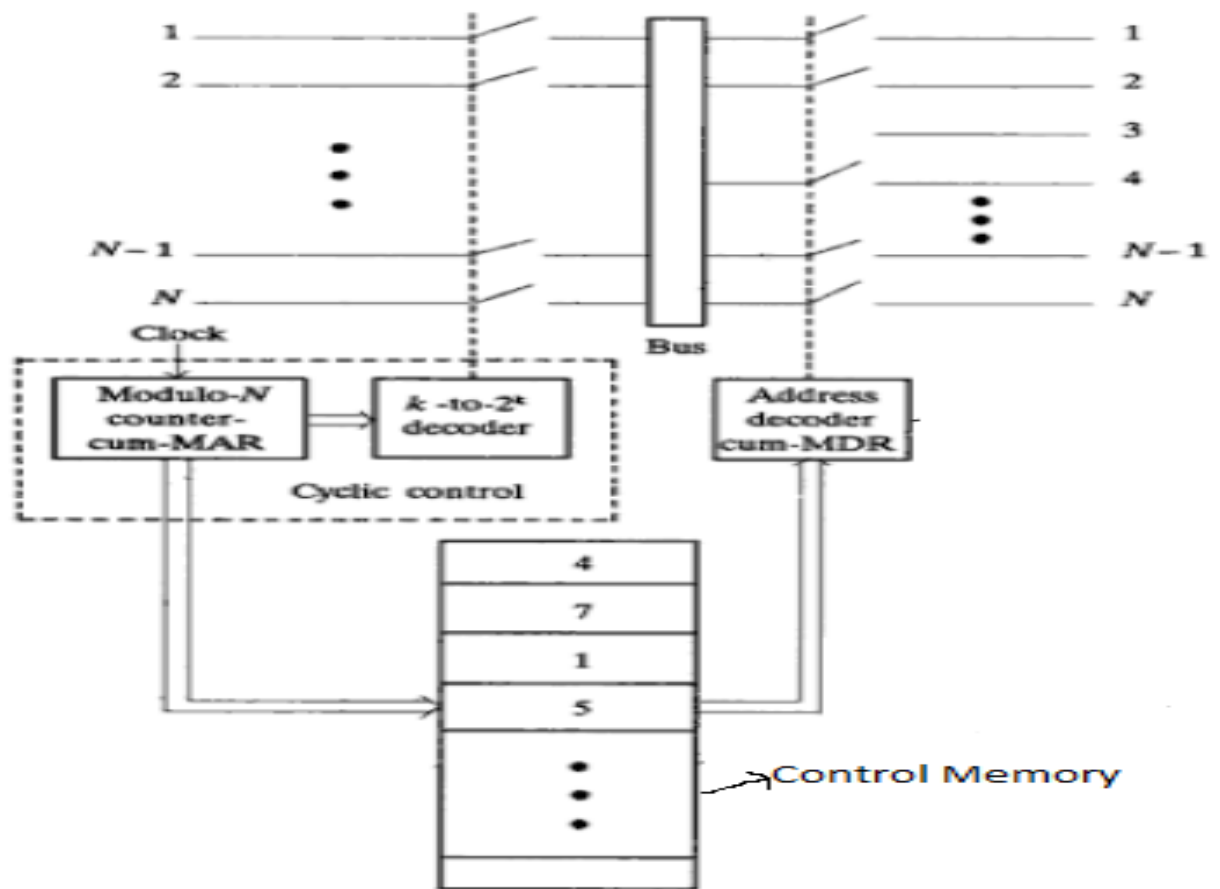


Fig. 6.2 Input-controlled time division space switch.

- The control on the input side works in a cyclic manner.
- The control on output side is memory based and changes synchronously with the input side.
- Full availability is obtained by using the programmable feature of the memory.

- There is a control memory on the output side which contains the address of the outlets stored in contiguous locations in the order in which they are to be connected to the inlets.
 - For example, an address sequence 4-7-1-5 stored in locations 1, 2, 3 and 4 of the control memory implies that inlet 1 is connected to outlet 4, inlet 2 to outlet 7, inlet 3 to outlet 1 and so on in that order. This switch is said to be input controlled or input driven.
 - The modulo-N counter of the cyclic control also acts as the memory address register (MAR) of the control memory.
 - Control memory has N words corresponding to N inlets and has a width of $\lceil \log_2 N \rceil$ bits which are used to address the N outlets.
 - Cyclic control at the input implies that all the subscriber lines are scanned irrespective of whether they are active or not.
 - For an active inlet i, the corresponding outlet address is contained in the i-th location of the control memory.
 - It is read out and passed to the address decoder which also acts as the memory data register of the control memory.
 - The decoder output enables the proper outlet to be connected to the bus. The sample value is then transferred from the inlet to the outlet.
 - In case an inlet is not active, the corresponding location in the control memory contains a null value which forbids the address decoder from enabling any of the output lines.
 - **Output-controlled**
 - A dual scheme of the input-controlled
 - The control on the output side works in a cyclic manner.
 - The control on input side is memory based and changes synchronously with the output side.
 - Full availability is obtained by using the programmable feature of the memory.
 - Broadcast is supported.
 - The switching capacity is equal to the number of inlets or outlets N.
- $$N=SC=125/(t_i+t_m+t_d+t_l)$$
- t_i : time to increment the modulo-N counter

- t_m : time to read the control memory
- t_d : time to decode address and select inlet/outlet
- t_t : time to transfer the sample value from inlet to outlet
- Clock rate of the counter

Clock rate = $8N$ kHz

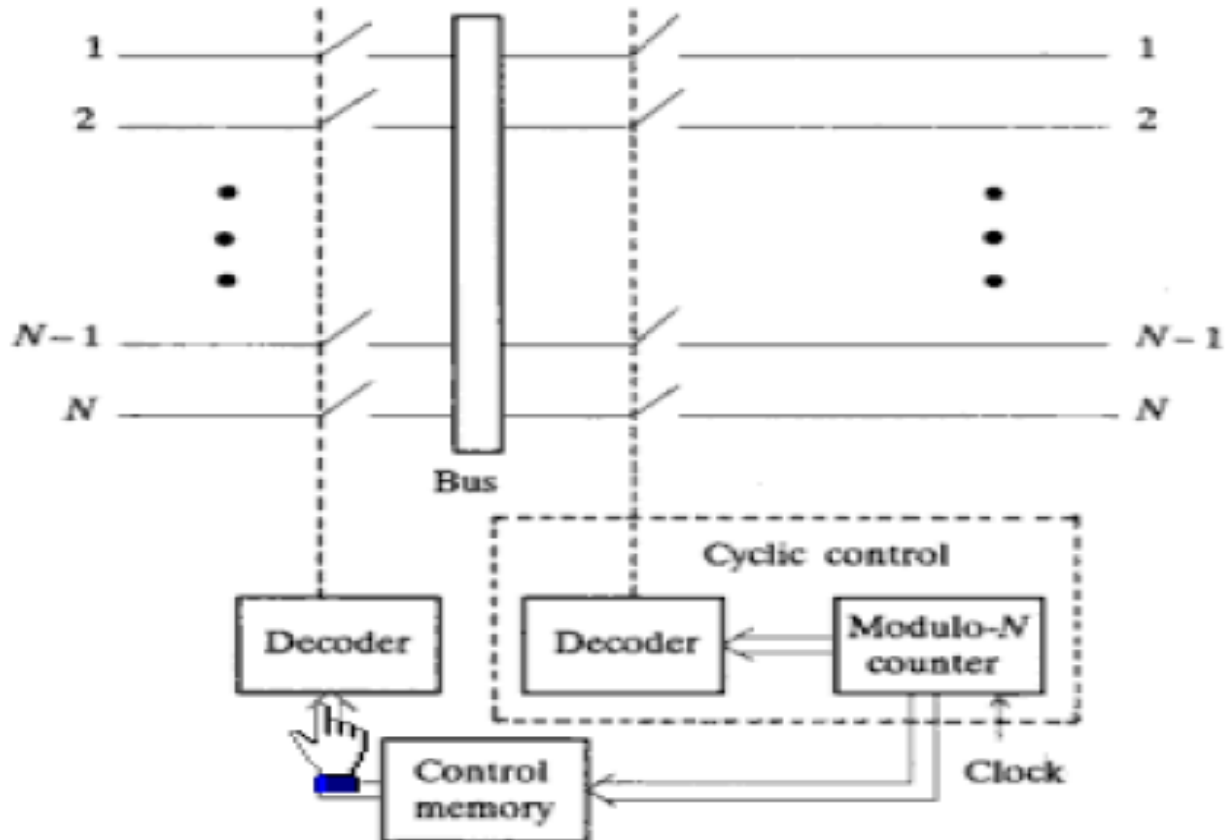


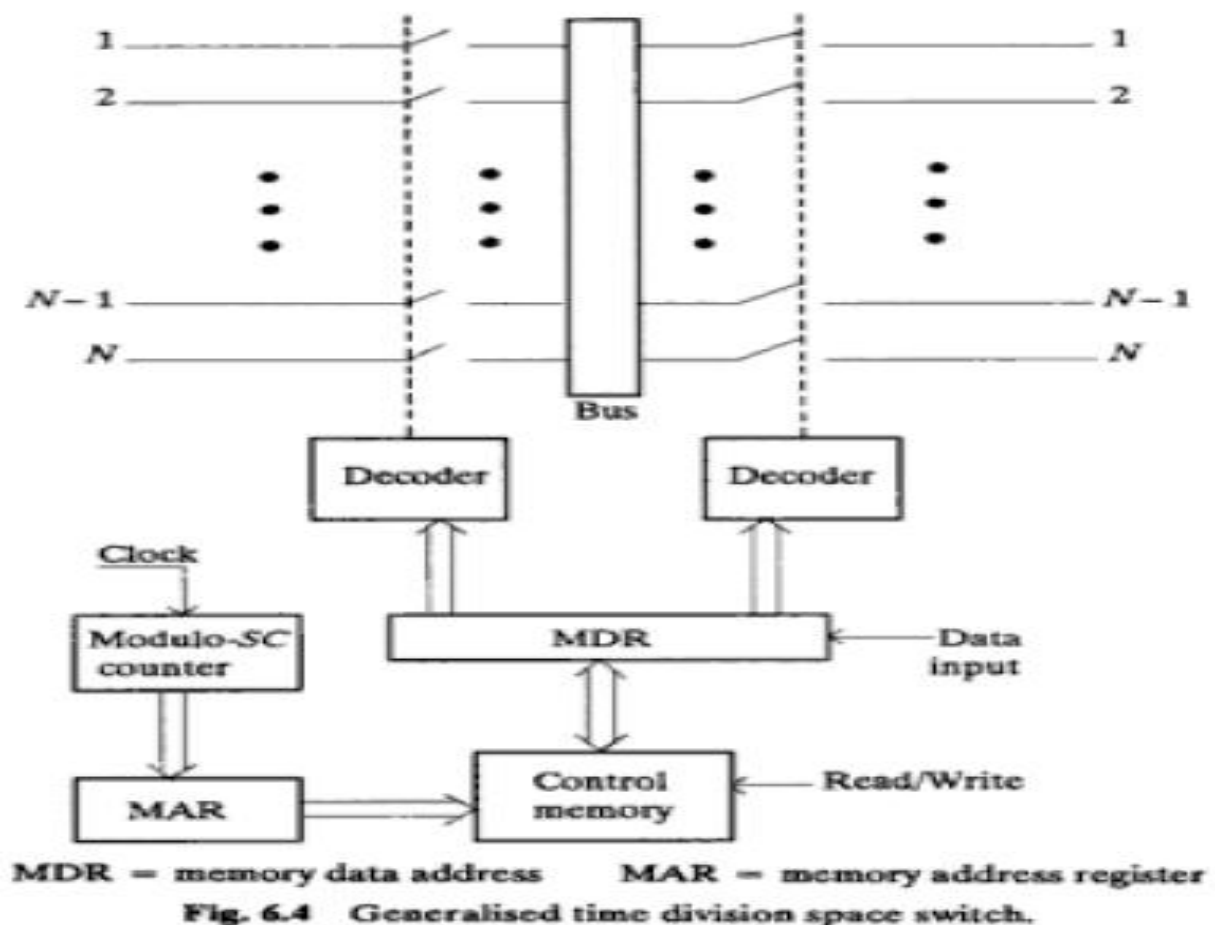
Fig. 6.3 Output-controlled time division space switch.

Parameters of time division space switching network (vs. Space division)

- For nonfolded networks, we have
- Number of switching elements:
 - On the input side = N
 - On the output side = N
 - total $S = N + N = 2N$

- Switching capacity, $SC=N$
- Traffic handling capacity, $TC=N/N=1$
- Cost of the switching network, $C=\text{cost of switching elements} + \text{cost of control memory}$
- $C=2N+N=3N$
- Cost capacity index, $CCI=SC/(C/N)=N/3$
- If we use space division switching on the same network, $C=2N$, SC reduces to one and CCI works out to be 0.5 irrespective of the number of subscribers ($CCI=1/(2N/N)=0.5$).

3.3 Generalized time division space switching



- The use of cyclic control in input or output controlled switches restricts the number of subscribers on the system rather than the switching capacity.

- A switch configuration based on the use of control memory for controlling both inlets and outlets would permit a much larger number of subscribers than the switching capacity of the network and can be made to function either as a folded or a non folded network.
- The structure of the memory-controlled time division space switch is shown in below figure. Here, each word of the control memory has two addresses: an inlet address and an outlet address. The control memory width is $2 \lceil \log_2 N \rceil$.
- The operation of the switch proceeds as follows:
 - The module-SC counter is updated at the clock rate.
 - The control memory words are read out one after another.
 - The inlet address is used to connect the corresponding inlet to the bus and so also the outlet address to connect the outlet.
 - The sample is then transferred from the inlet to the outlet. Next, the clock updates the counter and the cycle of the operation repeated.

3.4 Basic Time Division Time Switching

- The time division switching is to use a memory block in place of the bus.
- The functional blocks of a memory based time division switch and its equivalent circuits are shown in below figures.
- In this organization, the data coming in through the inlets are written into the data memory and later read out to the appropriate outlets.
- The incoming and outgoing data are usually in serial form whereas the data are written into and read out of the memory in parallel form.
- It, therefore becomes necessary to perform serial to parallel conversion and parallel to serial conversion at the inlets and outlets respectively. For convenience the data in and data out parts of the MDR are shown separately for the data memory in below figure.
- Here, the information is not transferred in real time, it is first stored in the memory and later transferred to the outlet. There is a time delay between the acquisition of a sample from an inlet and its delivery to the corresponding outlet. Signifying these aspects, the data memory based scheme is known as time division time switching.

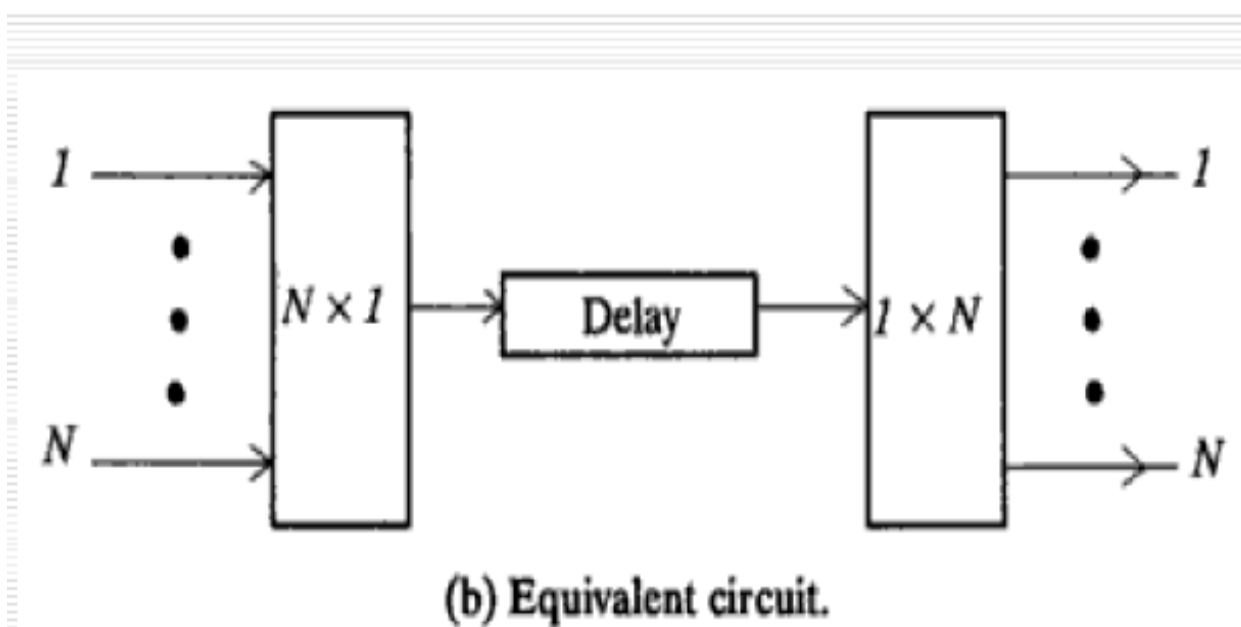
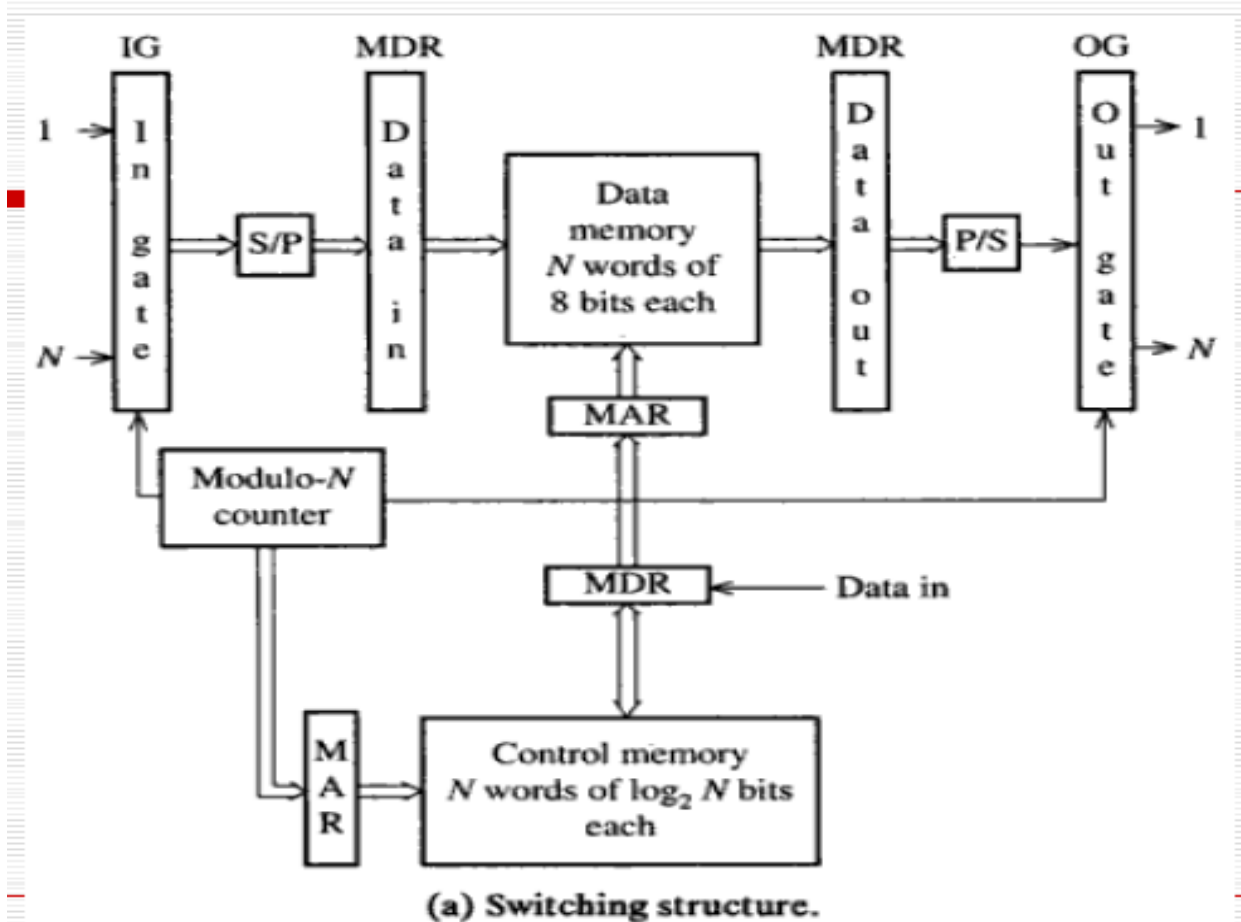


Fig. 6.5 Basic time division time switching.

- Time division time switching may be controlled in any of the following three ways:
 - Sequential write/Random read
 - Random write/Sequential read
 - Radom input/Random output
- **Sequential write/Random read**
 - The inlets and outlets are both scanned sequentially.
 - The samples from inlets are written into data memory sequentially.
 - The samples are read from data memory randomly and then delivered to outlets.
- **Random write/Sequential read**
 - The inlets and outlets are both scanned sequentially.
 - The samples from inlets are written into data memory randomly.
 - The samples are read from data memory sequentially and then delivered to outlets.
- **Radom input/Random output**
 - The inlets and outlets are both scanned randomly.
 - Both data writing and data reading operations on data memory are performed sequentially.

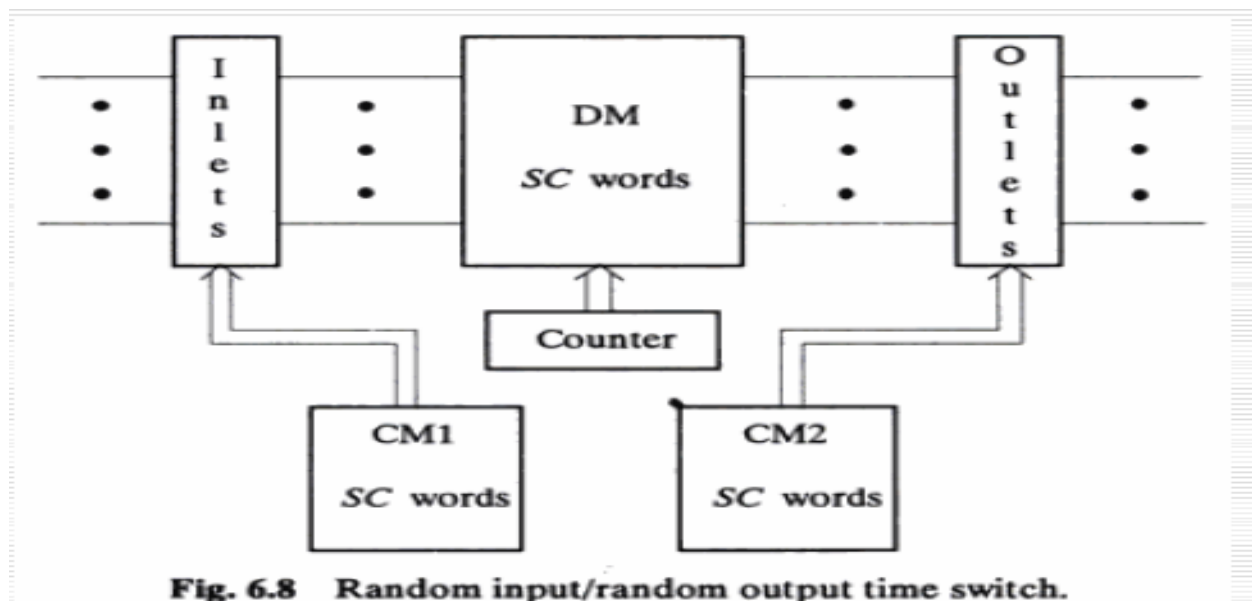


Fig. 6.8 Random input/random output time switch.

- There are two modes in which a time division time switch may be operated under any of the three forms of control. These modes are:

- Phased operation
- Slotted operation

➤ **Phased operation**

- The switching procedure is divided into two phases.
- Phase1: The data from inlets are stored in the data memory sequentially or randomly according to control method used.
- Phase2: The data are read from data memory and delivered to outlets sequentially or randomly according to the control method used.
- In the first phase, one memory write is involved per inlet whereas in the second phase two memory reads, one at the control memory and the other at the data memory are involved per outlet.
- The time taken for the two phase operation t_s is given by

$$t_s = Nt_d + N(t_d + t_c)$$

- Where t_d = read/write time for the data memory

t_c = read/write time for the control memory

If $t_d = t_c = t_m$, we have

$$t_s = 3N t_m$$

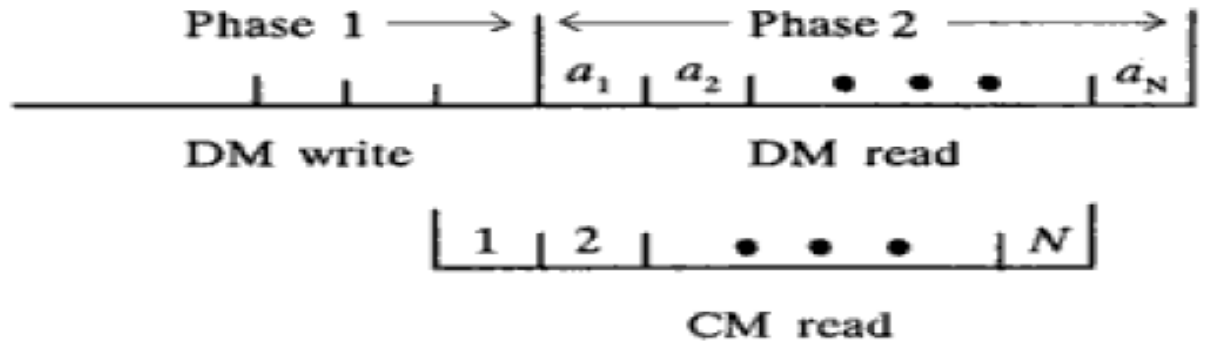
- Since the entire operation is to be completed within 125 μ s, we have the expression for the number of subscribers as

$$N = 125 / 3t_m$$

- The number of subscribers can be increased by overlapping the read cycles of the data memory and the control memory in the second phase of operation as shown in below figure.
- During last write cycle of phase-1, the first location of the control memory which contains an inlet address, say a_1 , is read.
- During the first cycle of the second phase, the location a_1 of the data memory and the second location of the control memory are read out simultaneously.

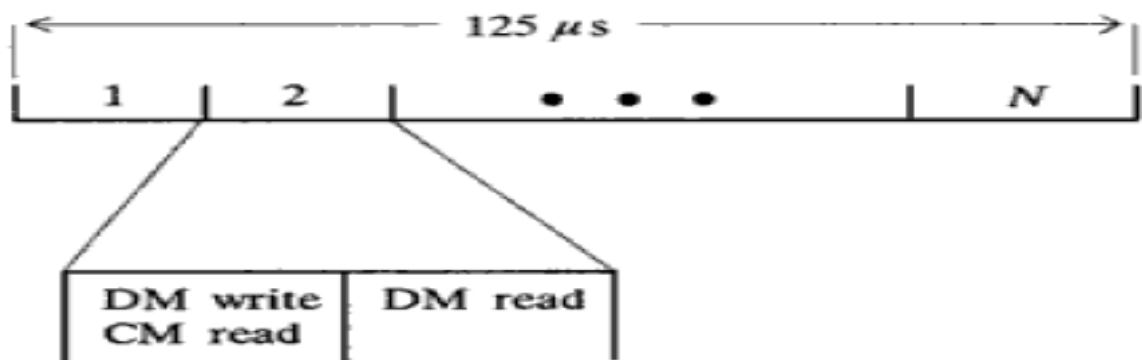
- The expression for the number of subscribers may be modified for overlapped operation as

$$N = 125 / 2t_m$$



(a) Overlapping of data and control memory reads

- **Slotted operation**
- In the Slotted operation the 125 μ s period is divided into N subperiods of duration 125/N. In each subperiod i, the following operations are performed:
 1. Read inlet i and store the data in data memory location i.
 2. Read the location i of the control memory which contains the value, say j.
 3. Read the data memory location j and transfer the data to outlet i.



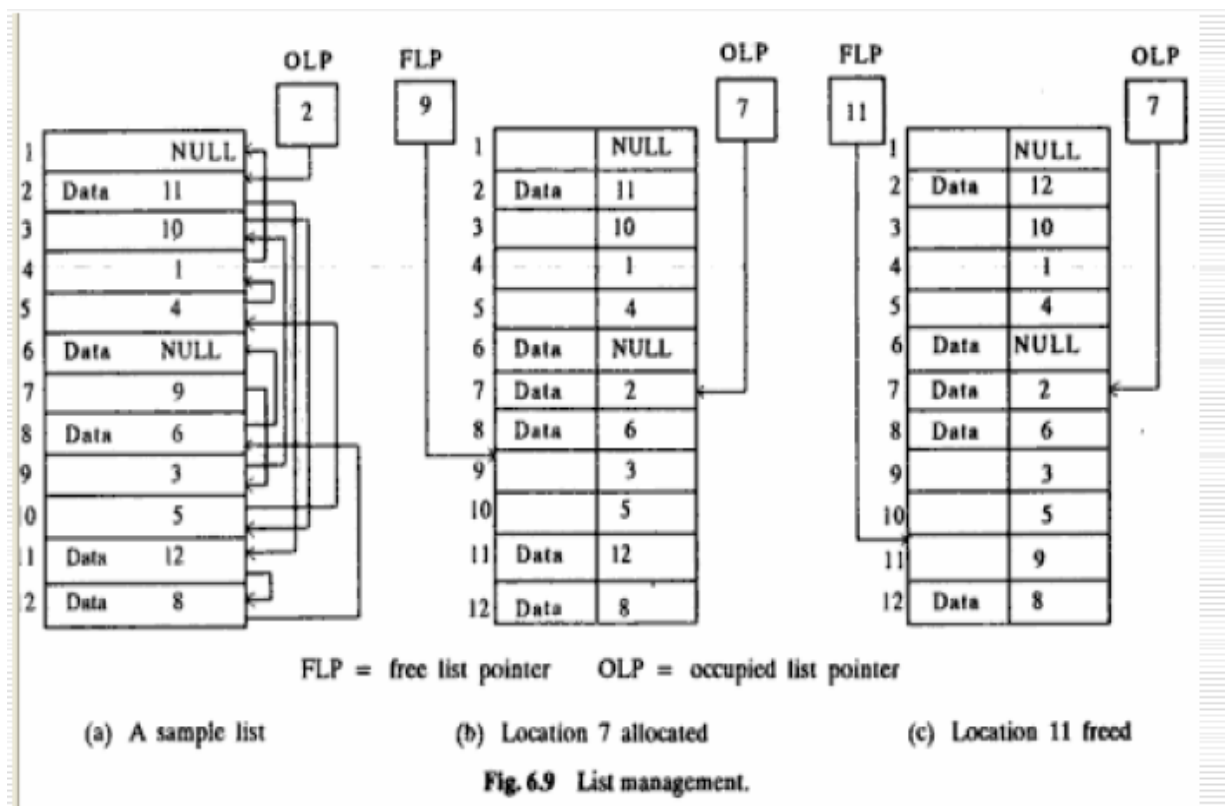
(b) Simultaneous DM write and CM read

Fig. 6.6 Two modes of operation of time switches.

Control memory management in random input/random output control:

- Random input/Random output control mode permits a large number of subscribers connected to the system, but it is blocking in nature.

- The entries in the control memory may be managed in any of the following three ways:
 - 1.By maintaining a free list
 - 2.By compacting the entries every time a call terminates
 - 3.By maintaining free and occupied lists.
- The free list is a linked list maintaining information about the free locations in the control memory. This list may be organized using a first come first served(queue) discipline or a last come first served (stack) discipline.
- The free list (or the occupied list) is usually managed by using pointers.
- Every entry in the list now consists of two parts: data and a pointer to the next entry in the list. For a free list, data value has no significance.
- The beginning of the list is identified by a variable which contains the address of the first free (or occupied) location which, in turn, points to the next free (or occupied) location.
- A link is thus established to all the free (or occupied) locations. The last (or occupied) location contains null pointer. This is illustrated in below figure.



3.5 Time multiplexed Space Switching

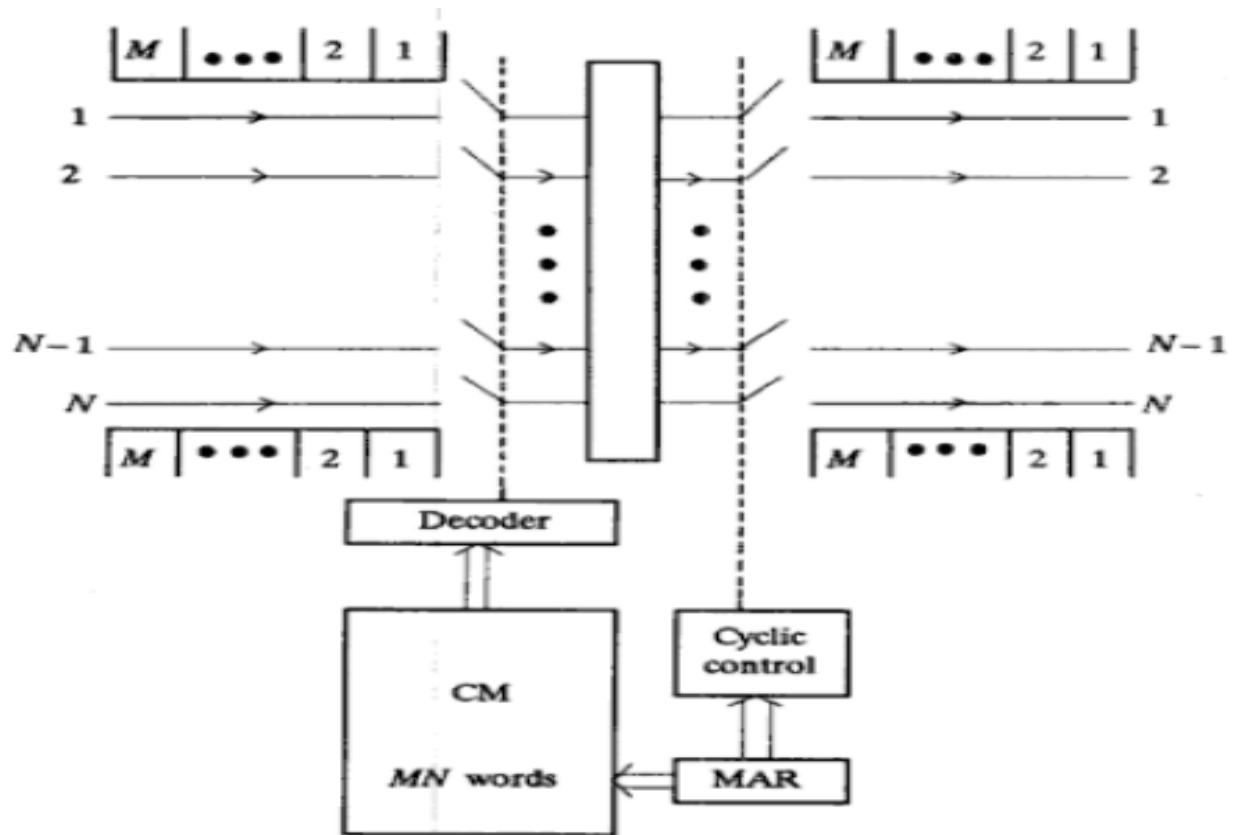


Fig. 6.10 Time multiplexed space switch.

- There are N incoming trunks and N outgoing trunks
- Each carrying a time division multiplexed stream of M samples per frame.
- Each frame is of 125 micro seconds time duration.
- In one frame time , total of MN speech samples have to be switched.
- One sample duration , $125/M$ micro seconds , is usually referred to as a time slot.
- In one time slot, N samples are switched.
- Figure shows output controlled switch. The output is cyclically scanned .
- There is a 1-to- M relationship between the outlets and the control memory locations i.e. there are M locations in the control memory corresponding to each outlet.

- The control memory has MN words
- If we view the control memory as M blocks of N word each, a location address may be specified in a two dimension form (i, j) .
- Where i is the block address and j is the word within the block.
- We have $1 \leq i \leq M$ and $1 \leq j \leq N$.
- The block address i corresponds to the time slot i and the word address j to the outlet j .
- The first N locations of the control memory correspond to the first time slot, the next N locations i.e. $N+1$ to $2N$ $(2,1)$ to $(2,N)$ when addressed correspond to the time slot 2 and so on.

Therefore if the location (i,j) contains an inlet address k , it implies that inlet k is connected to the outlet j during the time slot i . Number of trunks supported for this network is

$$N = 125/ Mt_s$$

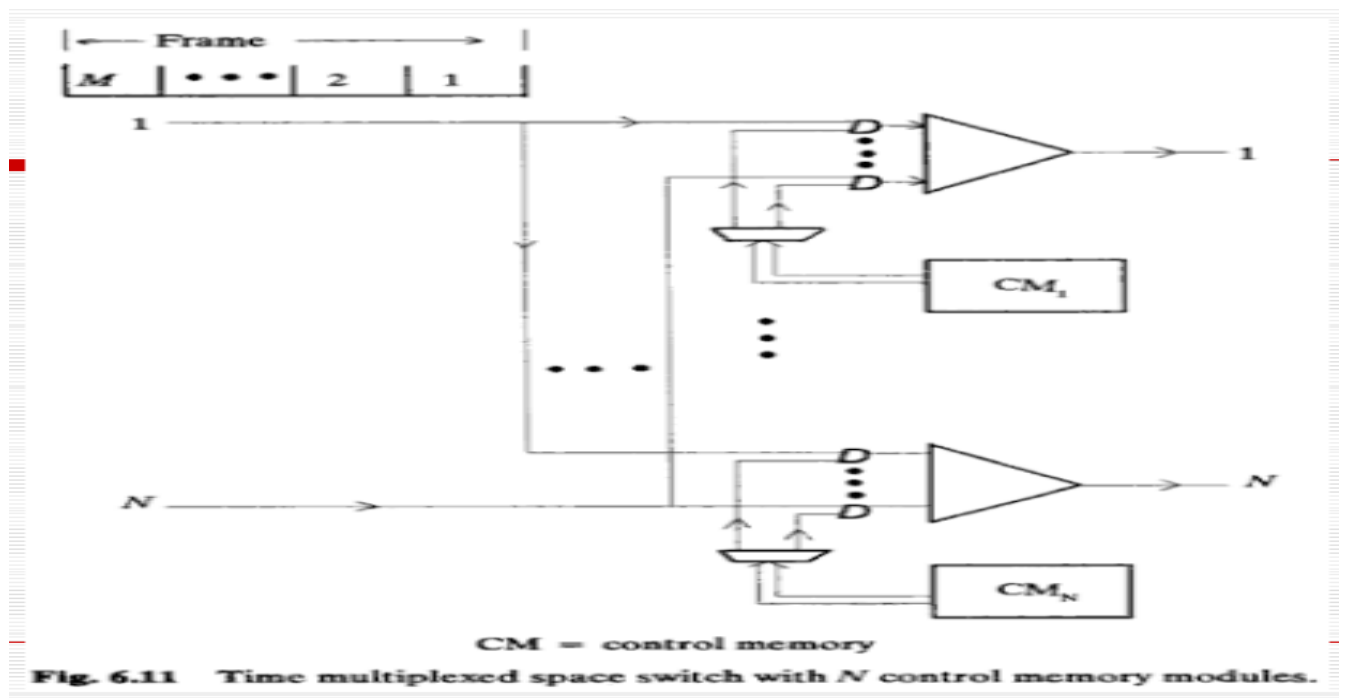
Cost of the switch is estimated as

$$\begin{aligned} C &= \text{No of switches} + \text{No. of memory words} \\ &= 2N + MN \end{aligned}$$

Cost of an equivalent Single-Stage space division network is $= (MN)^2$

- The number of trunks supported can be increased considerably by splitting the control memory into N independent modules of M words each and letting each module service one input or output line.
- If the control memory modules are arranged such that each one services one input line and switches the input data to the appropriate output during every time slot, the switch is input controlled.
- If the modules serve the output lines by switching the appropriate inputs, the switch is output controlled.
- An output controlled configuration is shown in below figure.
- There is one control memory module for each output line. The control memory modules contain the addresses of inlets that should be switched to the respective outputs in each of the M time slots.
- location-1 of every module corresponds to the time slot-1, location-2 to the time slot-2 and so on.
- All locations corresponding to a particular time slot are read out in parallel.
- To estimate the cost of the switch. The switch has N switching matrices of size $N \times 1$ each at inputs. There are NM memory words. Therefore, the cost is,

$$C = N(N \times 1) + NM = N^2 + NM$$



- Time multiplexed space switches do not provide full availability.
- Each incoming trunk carries multiplexed samples from M different voice sources and each stream on the outgoing trunk is demultiplexed to M different destinations as depicted in below figure.
- Sources, trunks and destinations have one to one time relationship as follows:
 1. Sources and incoming trunks time slots
 2. Outgoing trunk time slots and the destinations
 3. Time slots of incoming and outgoing trunks

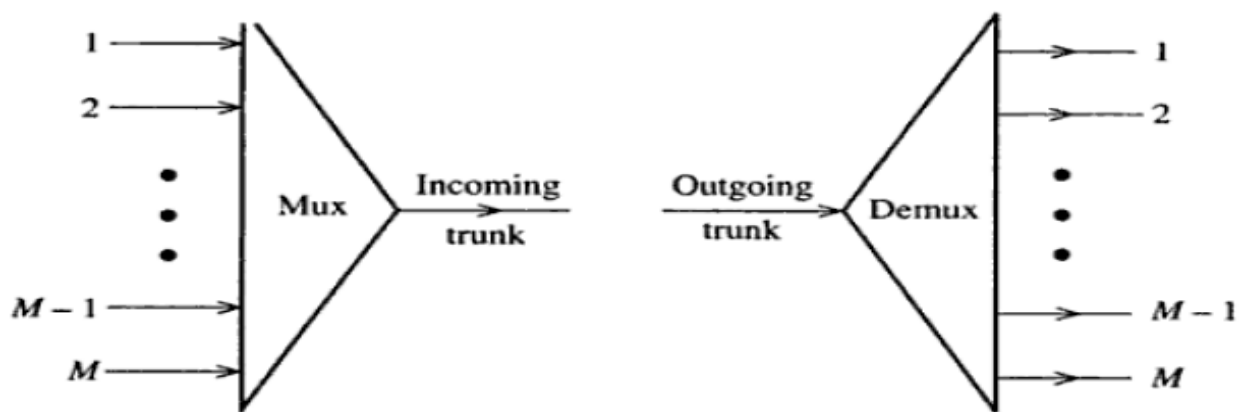
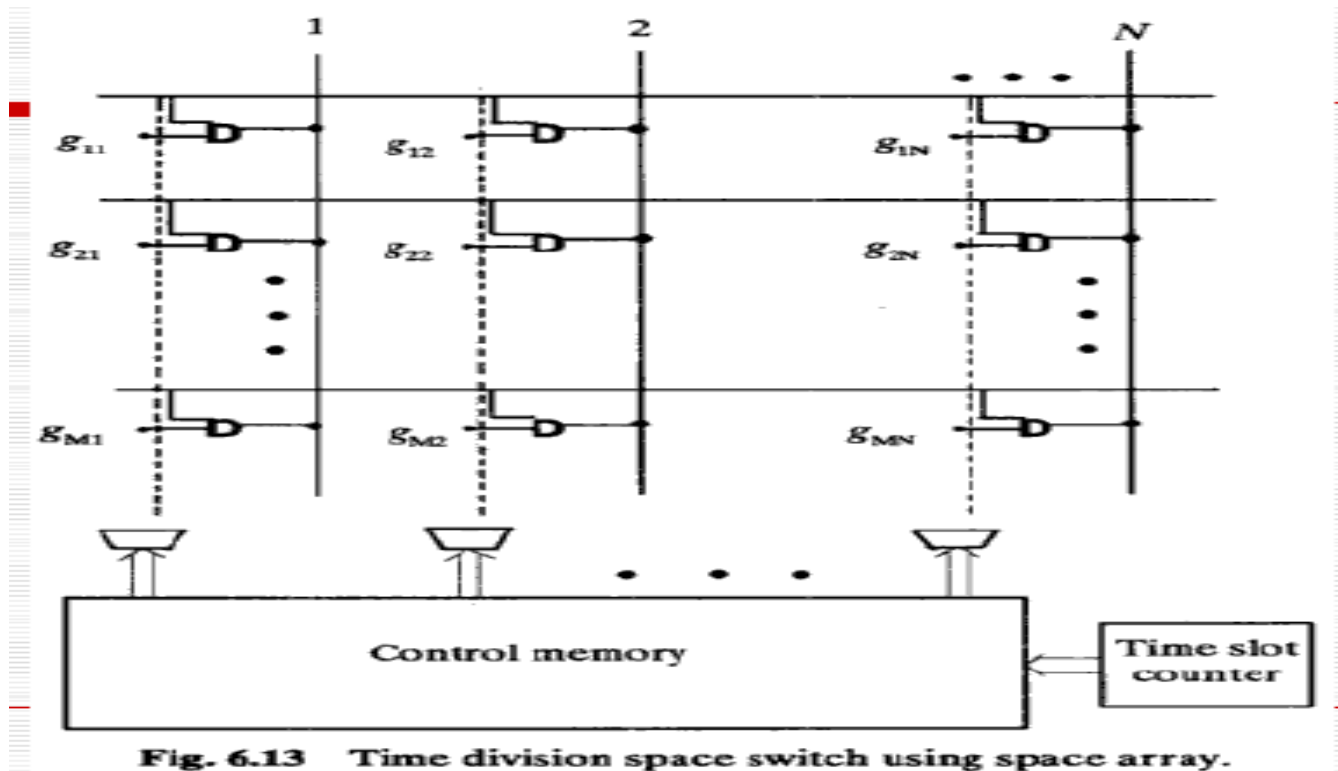


Fig. 6.12 Source multiplexing and destination demultiplexing.

Time division space switch using space array:

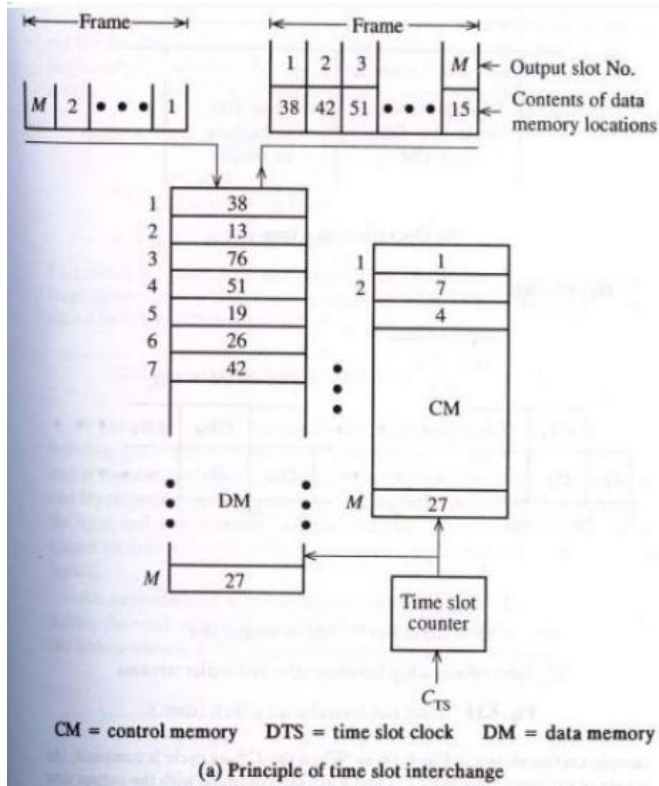
- With the advent of large scale integration in the semiconductor technology, integrated circuit space arrays that are suitable for digital space switching are becoming available.
- A digital space array of size $N \times N$ is similar to a $N \times N$ crossbar switching matrix, except the bulky expensive and power consuming electromagnets are replaced by digital gates.
- A time multiplexed time division space switch can be configured around a space array as shown in below figure.
- The array consists of M input horizontals and N output verticals. If $M=N$ the switch is non blocking. If $M > N$ the switch is concentrating and if $M < N$ the switch is expanding.
- In every time slot, one logic gate per vertical if $M > N$, or one logic gate per horizontal if $M < N$ is enabled for one to one connections.

- It may be observed that the space array is capable of establishing one to many and broadcast connections
- In any time slot only one gate for vertical and up to N gates per horizontal can be enabled for these connections.
- An enabled logic gate passes the input digital sample to the corresponding output vertical

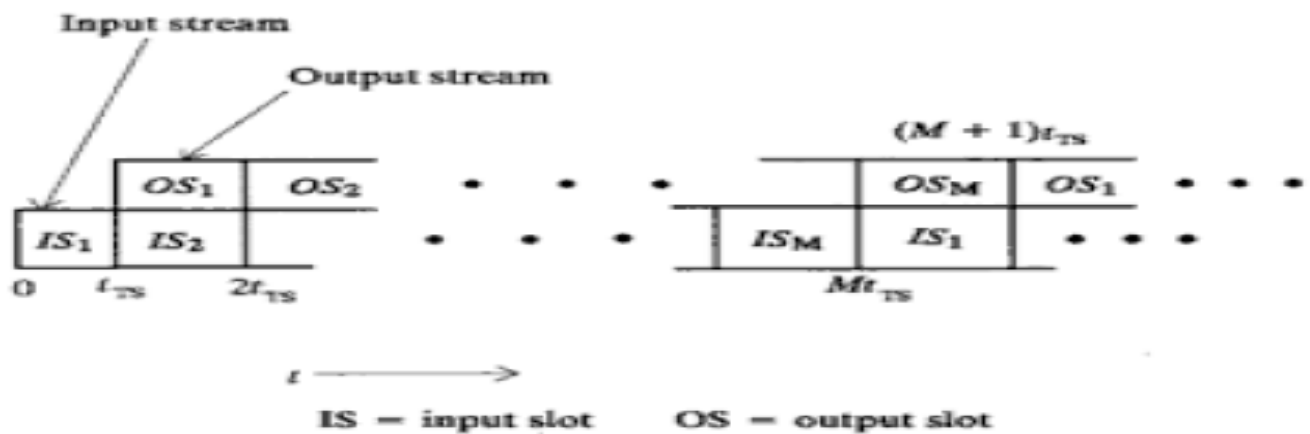
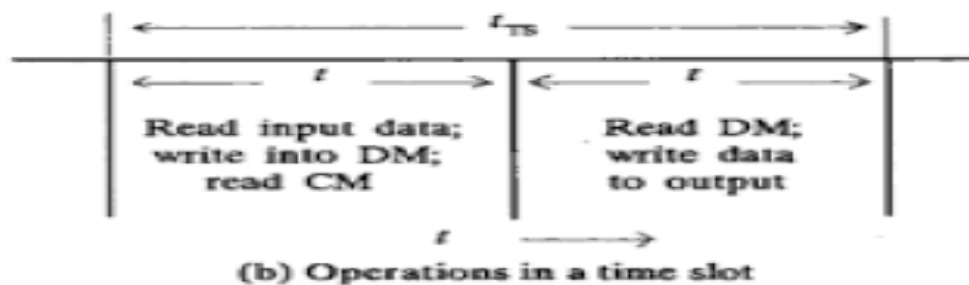


3.6 Time multiplexed time switching

- Unlike time multiplexed space switches, Time Multiplexed Time Switches permits time slot interchange (TSI) of sample values.
- In TSI, a speech sample input during one time slot can be sent to the output during a different time slot
- Such an operation necessarily implies a delay between the reception and the transmission of a sample. Below figure shows principle of TSI.



- M channels are multiplexed on each trunk
- The switch is organized in sequential write/ random read fashion
- Time slot duration, $t_{TS} = 125/M$
- Time slot clock runs at the time slot rate
- Time slot counter is incremented by 1 at the end of each time slot.



(c) Time relationship between inlet and outlet streams

Fig. 6.14 Time slot interchange switch (cont.).

- Contents of counter provides location addresses for the data memory and the control memory.
- Data memory and control memory access take place simultaneously at the starting of the time slot.
- Contents of the control memory are used as the address of the data memory and the data read out to the output trunk.
- Even if there is no time slot interchange, a sample is delayed by a minimum of one time slot in action.
- Depending on the output time slot, delay range is t_{TS} to Mt_{TS} microsec.
- In the example given in figure 1st location in CM contains value 1 which implies that the contents of input time slot 1 is switched to output time slot 1. Delay for this sample is t_{TS} microsec
- Location 2 contains 7. Therefore, input time slot 7 is switched to output time slot 2. Delay for this sample: $(M - (7-2) + 1) t_{TS} \mu s$

$$=(M - 4) t_{TS} \mu s$$
- Location 3 contains 4. Therefore, input time slot 4 is switched to output time slot 3. Delay for this sample: $(M - (4-3) + 1) t_{TS} \mu s$

$$=M t_{TS} \mu s = 125 \mu s$$
- There are two sequential memory access per time slot. So, time constraint may be stated as $t_{TS} = 2t_m$, $125 = 2Mt_m$
- As there are no switching elements the cost is equal to the number of memory locations
- There are M locations each in the control and data memory
- So, total cost is given by

Cost of switch = cost of switching element + cost of memory locations

$$C = (0+2M) \text{ units}$$

$$C=2M \text{ units}$$

- A TSI switch may be designed to be expanding or concentrating. In such switches, the number of time slots (samples) per frame in the input stream and in the output stream are different.

➤ **Expanding**

- The number of time slots per frame in the output stream M_2 is larger than that in the input stream M_1 , i.e. $M_2 > M_1$.

➤ **Concentrating**

- The number of time slots per frame in the input stream M_1 is larger than that in the output stream M_2 , i.e. $M_1 > M_2$.

➤ **Implementation:** Independent/asynchronous write and read.

- Time Constraint for the switch may be stated as in an expanding TSI switch:
 $125 = (M_1 + M_2) t_m$

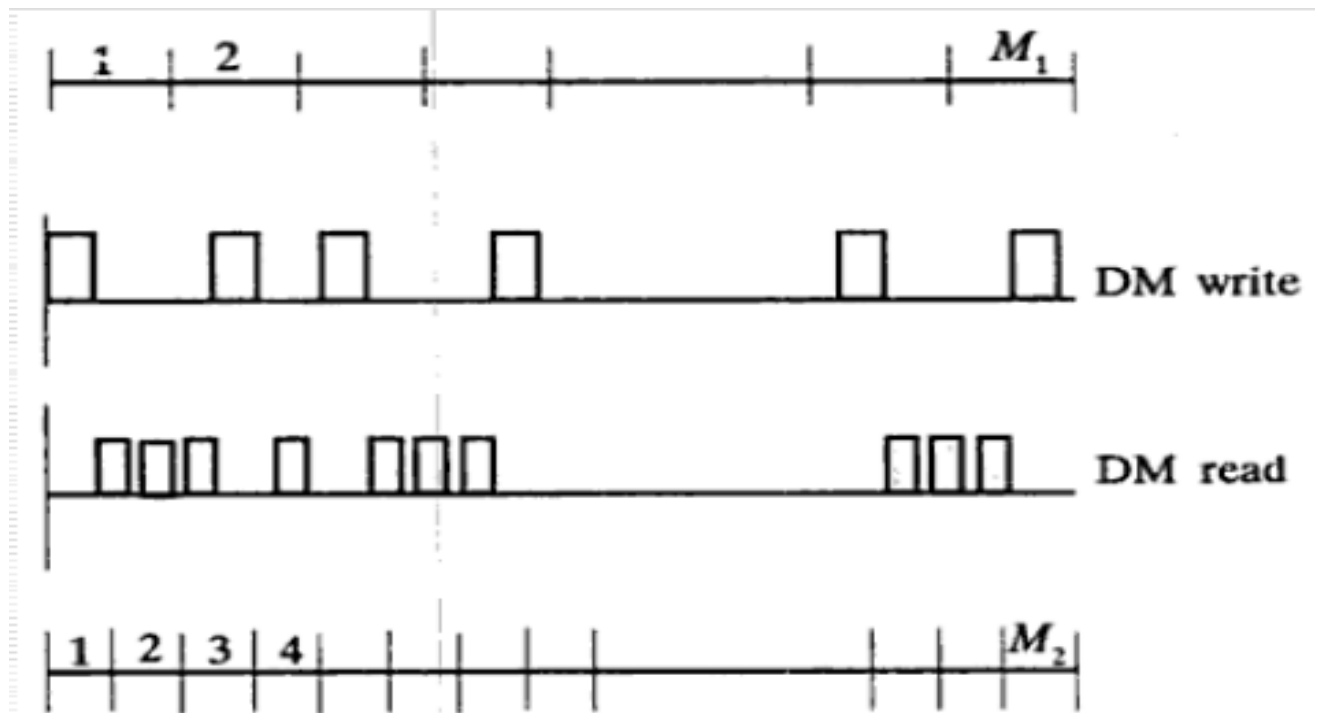


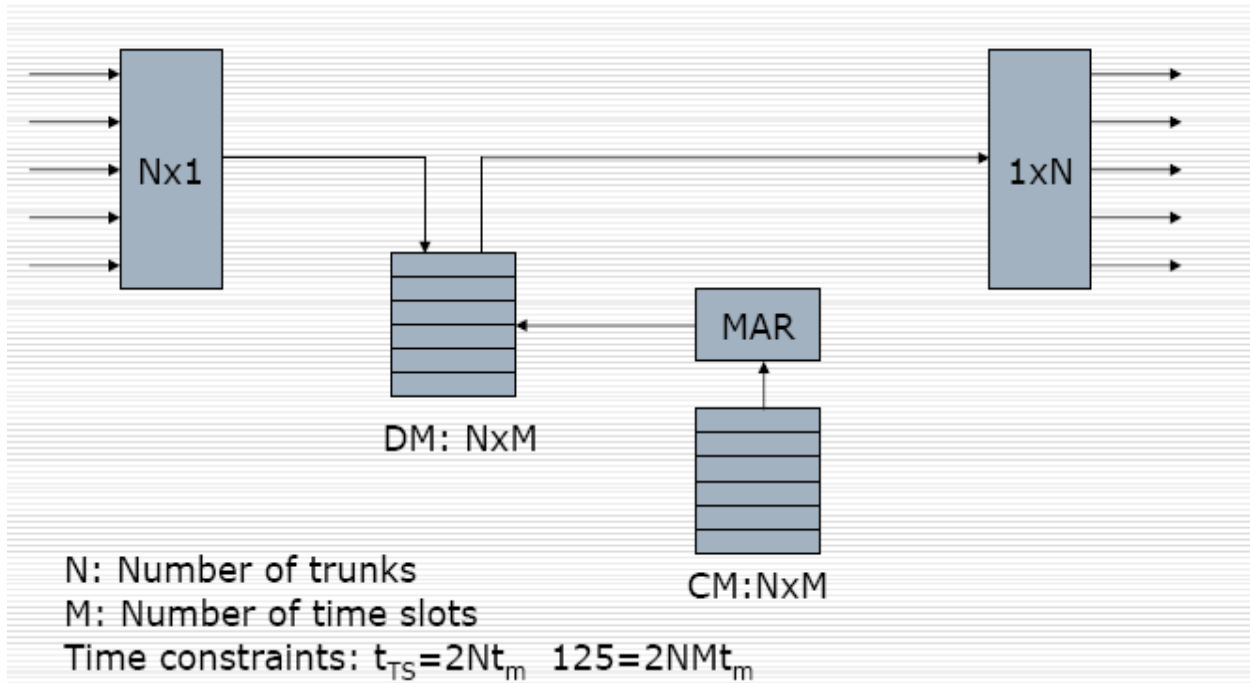
Fig. 6.15 Asynchronous read/write operations.

- Considering practical configuration of time multiplexed time switches, there are N time multiplexed input streams each multiplexing M subscribers and N time multiplexed output streams each carrying M subscribers.
- The task is to handle NM subscribers in time duration of $125 \mu s$. Such problem can be handled in four different configuration.

1. Serial-in / Serial-out (SISO) configuration

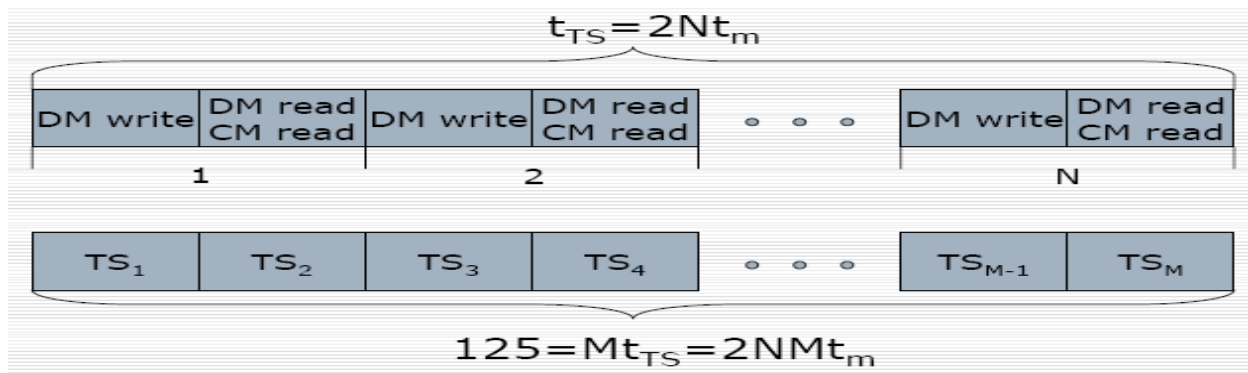
2. Parallel-in / Serial-out (PISO) configuration
3. Serial-in / Parallel-out (SIPO) configuration
4. Parallel-in / Parallel-out (PIPO) configuration

Serial-in/Serial-out (PISO) configuration:



- In each time slot, N data words are to be input and N data words to be output.
- During the first time slot, the first slot samples from all the input streams are read one after another and stored in the data memory.
- Within the same time duration, the data words corresponding to the first time slot of all the N output streams are read out of the data memory and sent to the respective output streams.
- The same operations are repeated for every one of the M time slots.
- The data memory write and the control memory read operations are carried out simultaneously followed by data memory read operation. The time constraints may be stated as

$$t_{TS} = 2Nt_m, 125 = 2NMt_m$$



Parallel-in / Serial-out (PISO) configuration:

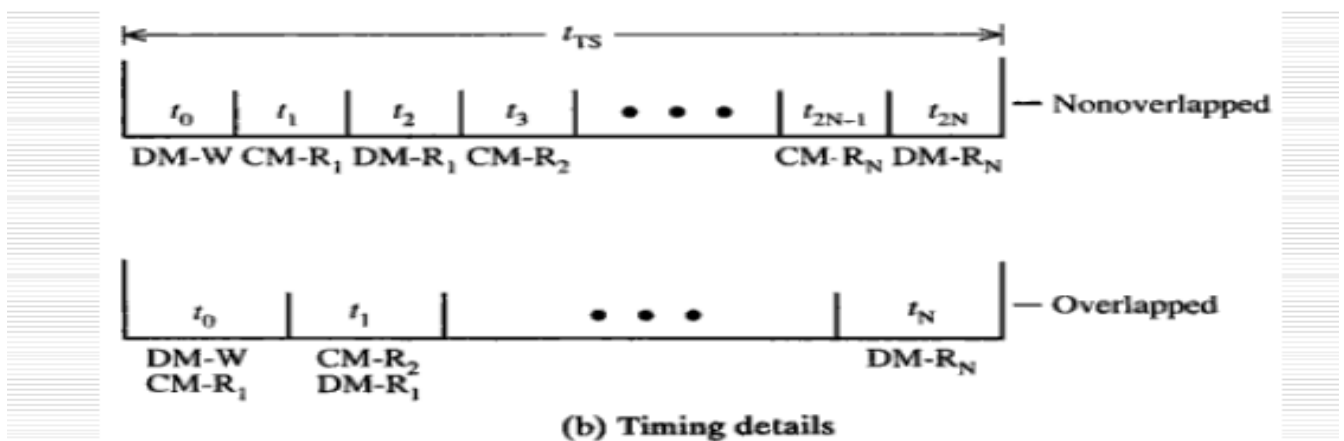
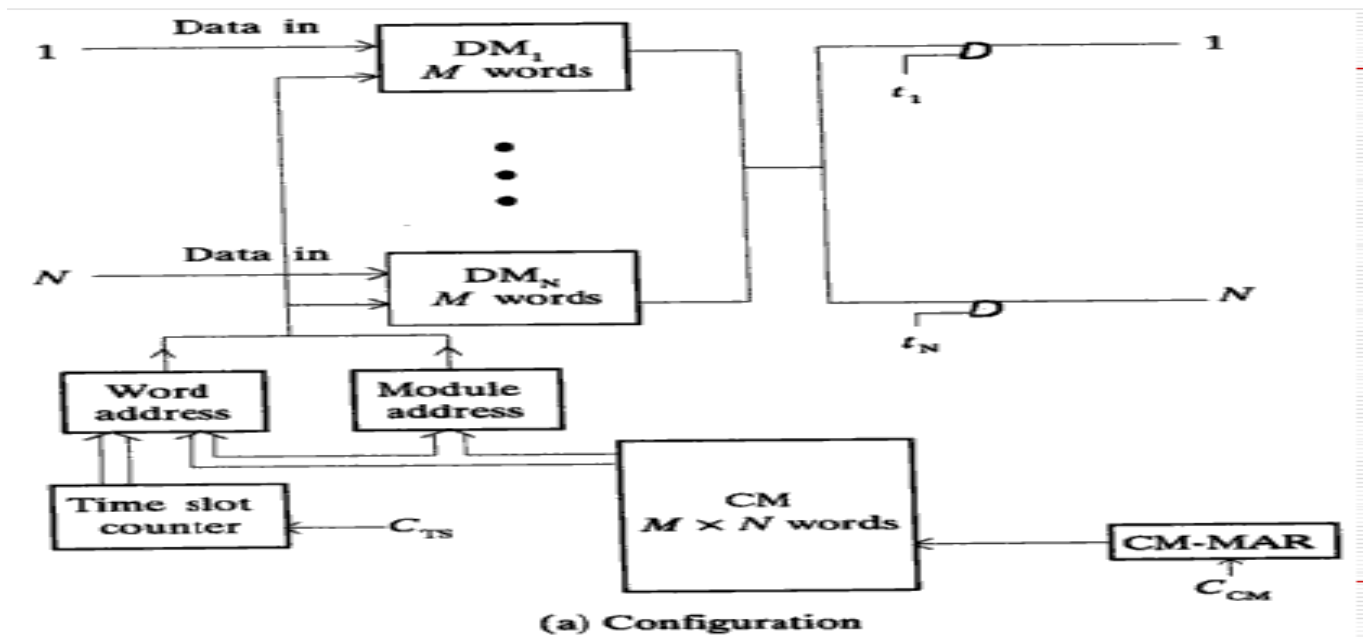


Fig. 6.16 Parallel-in/serial-out configuration.

Time constraints: $t_{TS} = (2N+1)t_m$ $125 = 2NMt_m$

- In Parallel-in / Serial-out (PISO) configuration, the data memory is organized as N modules of M words each as shown in above figure.
- Each module is associated with one input line. The time slot duration t_{TS} is divided into N+1 subslots $t_0, t_1, \dots, t_N$.
- During the subslot t_0 , data from all the input lines are read into the respective data memory modules simultaneously.
- A two dimensional addressing structure comprising module address and word address, is used to access the data memory words.
- The word address corresponds to the time slot number and the module address to the inlet number.
- The word address, word 1 corresponds to time slot 1, word 2 to time slot 2 and so on.
- A special control signal is used to enable all the data memory modules for write access during the subslot t_0 .
- During the subslots t_1 to t_N , the control memory locations are used to address the data memory for read access and the data words read out are transferred to the corresponding output lines.
- During the subslot t_1 of the time slot i, a data word read from the data memory is transferred to the outgoing trunk 1, for insertion in the time slot i of this stream
- Similar transfers take place during subslots t_2 to t_N to outgoing trunks 2 to N.
- The control memory locations contain the two part address of the data memory.
- The higher order address bits select the module and the lower order bits the word within a module.
- The width of the control memory word is $\lceil \log_2 N \rceil + \lceil \log_2 M \rceil$.
- The control memory clock C_{cm} , runs at the rate one pulse per $t_{TS} / (N+1)$ microseconds except that one pulse is inhibited during the subslot t_0 .
- The control memory read may be overlapped with data memory as indicated in the timing diagram in above figure.
- The time constraints may now be stated as:

For non overlapped operation

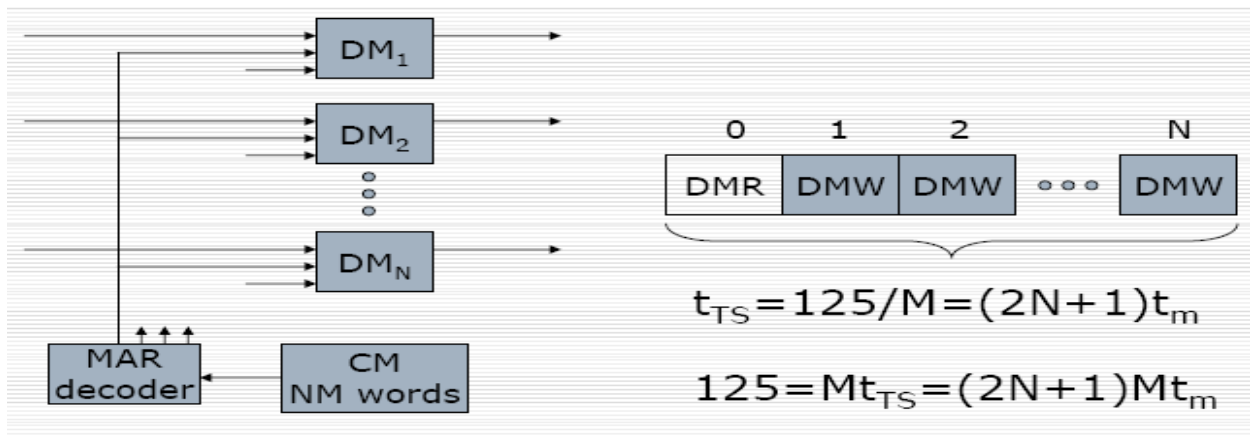
$$t_{TS} = (2N+1) t_m, \quad 125 = M(2N+1) t_m$$

For overlapped operation

$$t_{TS} = (N+1) t_m, \quad 125 = M(N+1) t_m$$

Serial-in / Parallel-out (SIPO) configuration:

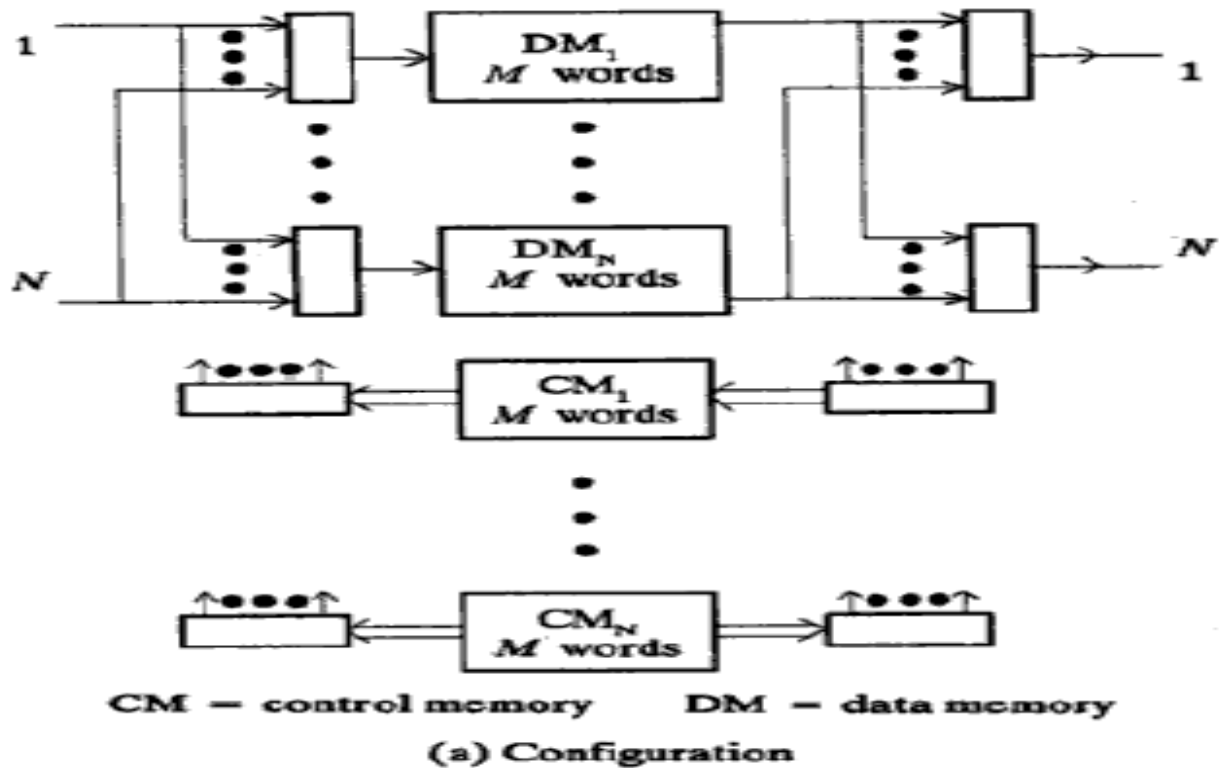
- Serial-in / Parallel-out switch is the dual of the parallel-in/serial-out switch. Here, the data memory modules are associated with the output lines instead of the input lines.
- The data input is serial and is carried out during the subslots t_1 to t_N .
- The subslot t_0 is used for parallel read out from all the data memory modules to the corresponding output lines.
- With this arrangement, it appears as though the output precedes input.
- Since the entire operation is cyclic, it is immaterial whether the output operation is carried out in subslot t_0 to t_N .



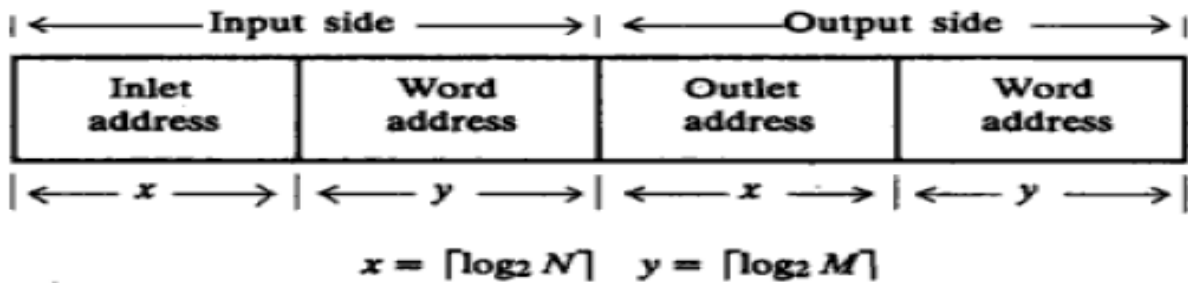
Parallel-in / Parallel-out (PIPO) configuration:

- Parallel-in/Parallel-out switch is the most complex of all the time multiplexed time switch configurations.
- It is also the configuration that can support the largest number of subscribers for a given technology option.
- The configuration shown in above figure(a), both the data memory and the control memory are organized as N independent modules of M words each.
- There is one to one correspondence between the data memory and control memory modules.

- Address outputs from the control memory module i are always used to access words in the data memory module i .



- Each location of the control memory module contains information about both the input side and the output side as shown in above figure (b).
- The input side contains an inlet address part and a word address part and the output side contains an outlet address part and a word address part.
- Inlet/outlet address selects one of the N inlet/outlet streams.
- Word address is used to access one of the M words in the data memory module corresponding to the control memory module from which the word address is read.
- The operation of the switch takes place in three phases in each time slot
 1. Control memory read
 2. Data memory write
 3. Data memory read



(b) Contents of control memory locations

Fig. 6.17 Parallel-in/parallel-out time switch.

3.7 Combination Switching

- Time multiplexed space switches do not provide full availability as they are not capable of performing time slot interchange (TSI).
- The TSI switches are not capable of switching sample values across the trunk without the help of some space switching matrices. Hence a combination of time and space switches leads to configurations that achieve both TSI and sample switching across trunks.
- A combination switch can be constructed by using number of stages of time and space switches.
- A two stage combination switch configurations are known as time-space (TS) or space time (ST) switches.
- The most common three stage configurations are space-time-space (STS) and time-space-time (TST) switches.

Time-Space (TS) switch:

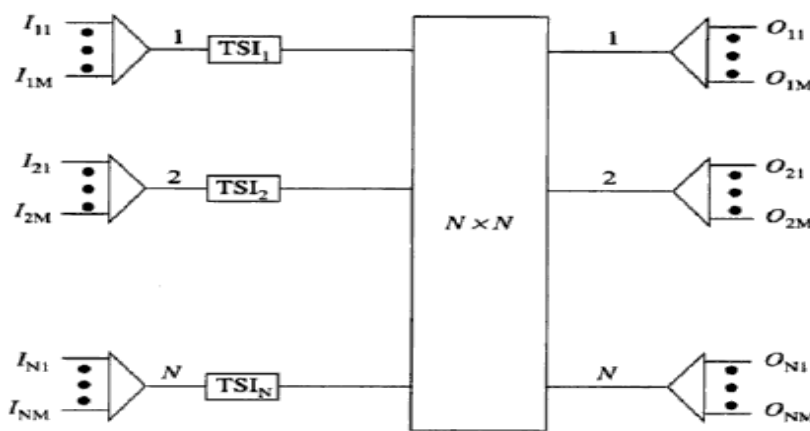


Fig. 6.18 Two-stage TS switch.

Example

Connection:

I47 → O56

Stage 1:

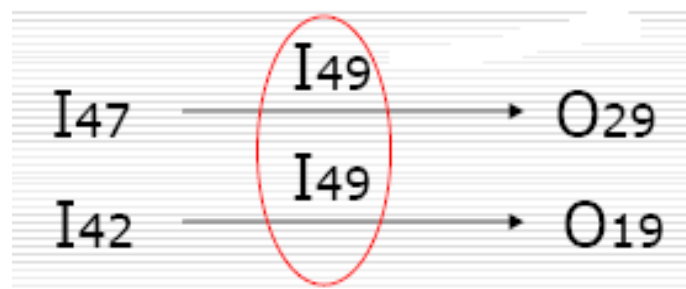
I47 → I46

Stage 2:

I46 → O56

- A Time-space (TS) switch is shown in below figure.

- the first stage is a time slot interchange (TSI) per inlet and second stage is a $N \times N$ space switch.
- Each time multiplexed inlet/outlet stream carries M channels.
- A subscriber on the input side is assigned to one of the inlets and a time slot in that inlet.
- An input subscriber assigned to line 4 at time slot 7 is identified by the label I_{47} .
- A subscriber connected to the outlet 5 and time slot 6 is identified by O_{56} .
- The corresponding time slots are identified as IS_{47} and OS_{56} . A communication is established between these two subscribers. The input sample from IS_{47} is first moved to IS_{46} at the output of TSI switch.
- During the time slot 6, a connection is established between the inlet 4 and the outlet 5 at the space switch. This switch configuration ensures full availability, it is not nonblocking.
- Consider the two connections to be established between I_{47} and O_{29} , and I_{42} & O_{19} .
- Both the samples originate from the same inlet and are destined to the same time slot in different outlets.
- Both input samples require to be switched to time slot 9, which is not possible. Only one of them can be switched to slot 9.
- In general blocking occurs if two inputs I_{ij} and I_{ik} are destined to outputs O_{pq} and O_{rq}



Let the traffic intensity in erlangs per inlet trunk $= \rho E$

Probability that a subscriber X is active $= \frac{\rho}{M}$

Probability that any other subscriber is active on the same inlet $= \frac{(M-1)}{M} \rho$

Probability that a particular outlet subscriber is chosen by X $= \frac{1}{MN}$

Probability that the same time slot on a different outlet is chosen by the other subscribers on the same inlet $= \frac{(M-1)\rho(N-1)}{M(MN-1)}$

Therefore, the blocking probability is given by

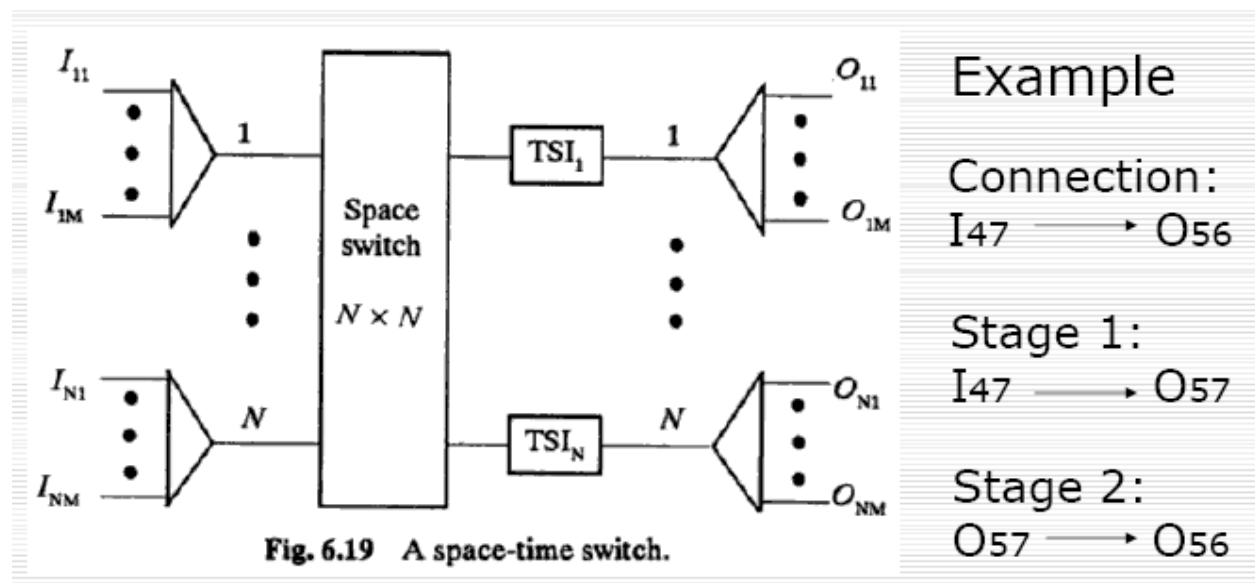
$$P_B = \frac{\rho}{M \times MN} \frac{(M-1)(N-1)}{M(MN-1)}$$

If $M \gg 1$ and $N \gg 1$, then Eq. (6.23) becomes

$$P_B = \frac{\rho}{M^3 N}$$

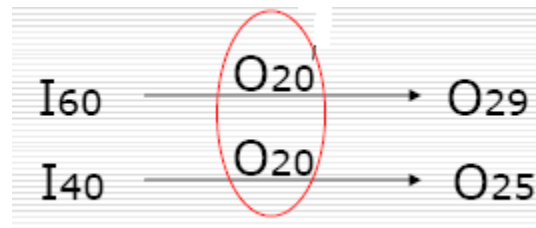
gunjinotes.com

Space-Time (ST) switch:



➤ A space time switch configuration is shown in below figure.

- This two-stage ST switch ensures full availability.
- Consider a connection between I_{47} and O_{57} .
- Similar to TS switch, this switch is also blocking.
- It is a blocking network. If two or more samples originating from different inlets during the same time slot are destined to the same outlet, blocking will occur.



- The performance of ST and TS switches are identical .
- Two switches are in series in these configurations, the time constraint is the sum of the two constraints and is given by

$$125 = 2 NMt_m + NM t_m = 3NM t_m$$

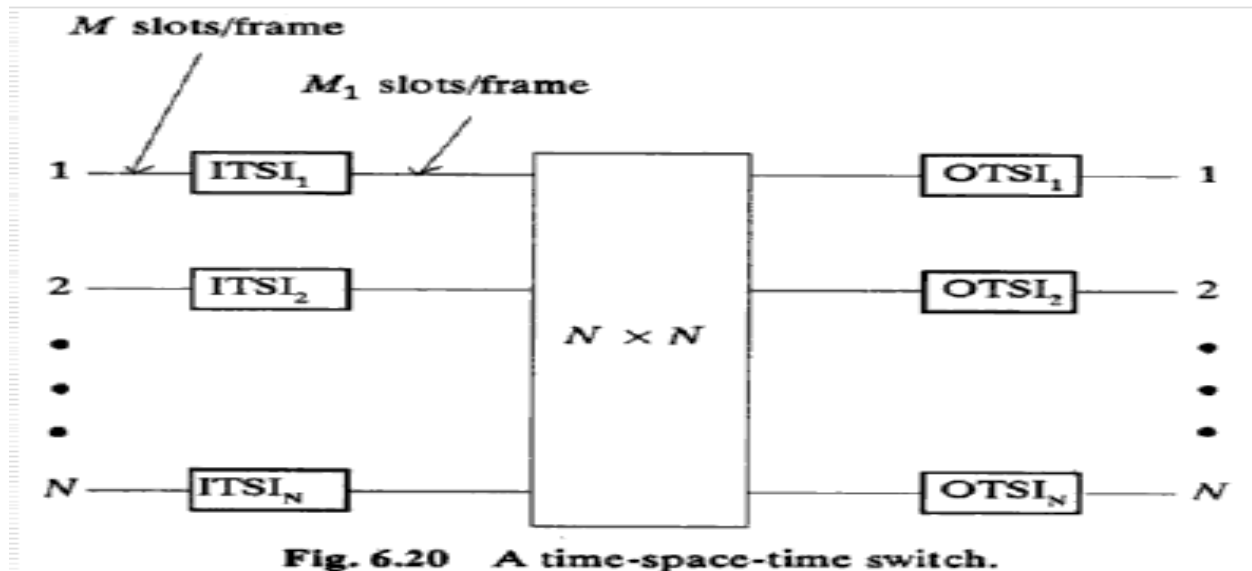
3.8 Three-Stage Combination Switching

- Three-stage Combination Switching provides better flexibility than two stage Combination Switching.
- The most common three stage configurations are:
 - **Time-space-time (TST) switches**
 - The first and third stages perform time switching
 - The second stage performs space switching.
 - **Space-time-space (STS) switches**
 - The first and third stages perform space switching;
 - The second stage performs time switching.
- Both TST and STS are blocking in general cases.

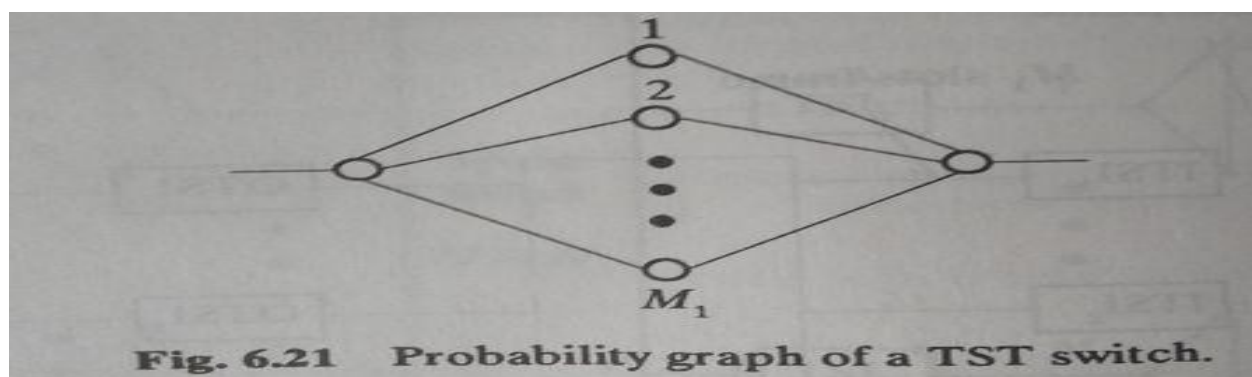
Time-Space-Time (TST) switches:

- The TST switch configuration is shown in below figure.

- In TST, two time stage at input and output side exchanges the information between external channels (i/p side) and the internal space array channels (o/p side). Hence there is no need to have a fixed space stage time slot for given input or output time slot.



- An incoming time slot may be connected to an outgoing channel time slot using any possible space array time slot.
- There exist multiple alternative paths between prescribed input and output unlike two stage switch has only one fixed path. Because of this, the value of blocking probability of three stage combination switch is reduced.
- Three stage combination switches are not perfectly non-blocking. To make it non-blocking, one slot in the intermediate space stage has to increase.
- **Lee's Probability graph of TST switch**



$$P_B = \left(1 - (1 - \alpha/L)^2\right)^{M_1} \quad (6)$$

where

M_1 = number of time slots on the output side of the TSI switch

L = expansion or concentration factor = M_1/M

α = traffic intensity on an inlet

Space-Time-Space (STS) switches:

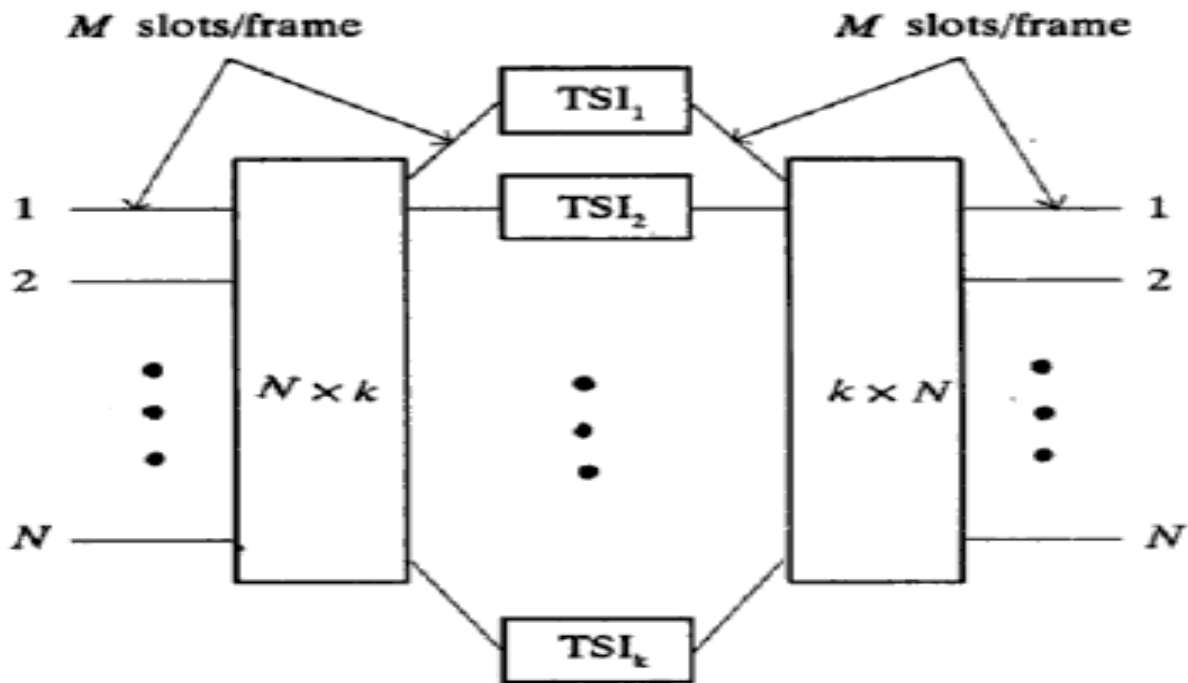


Fig. 6.22 A STS switch.

- A STS switch consists of $N \times k$ space matrix switch at input and an array of TST switches of middle with $k \times N$ space matrix.
- In STS switch the choice of input and output time slots is fixed for a given connection.
- But flexibility is provided by the ability to utilize any free TSI switch by space switching on input and output side. Many alternative paths exists as in TSI switch.
- The expansion and concentration takes place at the space switch level instead time slot level.
- The time slots are symmetrical
- STS switch is non-blocking, if $k=(2N-1)$. The blocking probability is same as TST switch.

- Costs of TST and STS
- **TST**
 - $C_{TST} = 5MN + N^2$
- **STS**
 - $C_{STS} = 2Nk + 4MN$
- The blocking probability is reduced by providing more feasible paths for any inlet-outlet pair.

3.9 n-Stage Combination Switching

- Very large time division switches, supporting 40,000 lines or more, can be economically designed by using more than three stages of time and space combination switching.
- We call this N-stage switching where N is greater than three, N-stage combination networks may also be designed to provide better flexibility and less blockage.
- Basically, two approaches are seen in designing N-stage switches:
 - Expanding a TST switch with additional space stages
 - Modular design using a number of time-space (TS) modules
- Typical configurations include TSST, TSSST and TSTSTSTS.

Table 6.1 Examples of Time-Space Combination Switches

System	Configuration	Traffic capacity (erlangs)	Maximum number of trunks
E10 B (France)	TST	1600	3600
No.4 ESS (USA)	TSSSST	47,000	107,520
C-DOT MAX-XL (India)	TST	16,000	40,000
DMS 100 (Folded) (Canada)	TSTS	39,000	61,000
System 12 (USA)	TSTSTSTSTSTSTS	25,000	60,000
NEAX 61 (Japan)	TSST	22,000	60,000

TIME DIVISION SWITCHING

In a single stage space division networks, a crosspoint switching element is used to establish a specific connection between two subscribers. In multistage space division network

⊛ " If we can establish a dynamic control mechanism whereby a switching element can be assigned to a number of input-outlet pairs for two microseconds each, a single switching element can be used to transmit speech samples from a no of inputs to the corresponding outlets "

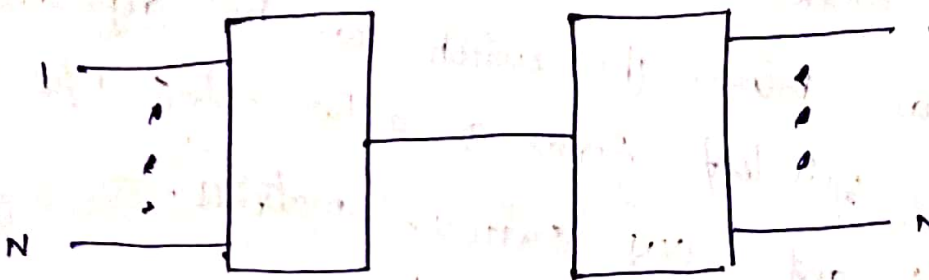
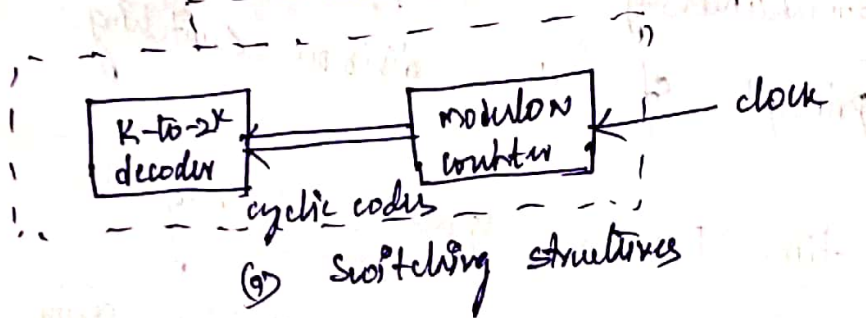
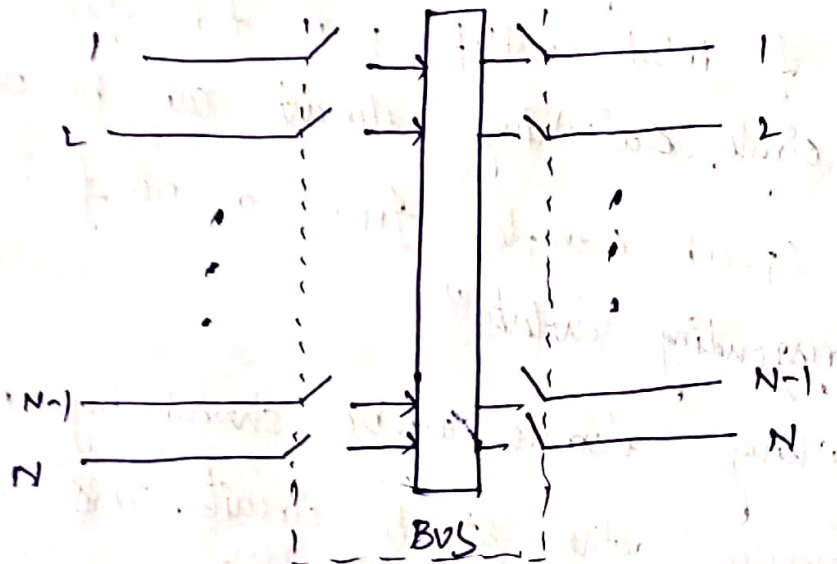
→ A switching element can be shared by number of simultaneously active speech circuits. This is the principle of time division switching.

⇒ Basic time division space switching:

→ A single $N \times N$ time division space switch is shown below. The switch can be represented in an equivalent form as a two-stage n/w with $N \times 1$ and $1 \times N$ switching matrices.

→ The network has one link to interconnecting two stages, Each input/output is single speech ch corresponding to a subscriber line.

→ The speech is carried as PAM analog samples or PCM digital samples, occurring $125\mu s$ intervals, when PAM samples are switched in a time division manner, that is known as 'Analog time division'. If PCM binary samples are switched, then the switching is known as 'digital time division switching'.



(b) Two stage equivalent

→ The interconnecting link is shown as bus to which a chosen inlet-outlet pair can be connected by a suitable control mechanism and speech sample transferred from the inlet to the outlet.

→ the no. of simultaneous calls 'Sc' can be supported on a r/w of this type is inversely proportional to the time required to select and connect an inlet outlet pair and transfer the speech samples from inlet to the outlet and is given by

$$Sc = \frac{125}{t_s}$$

where t_s = time in microseconds to set up a connection and transfer the sample value.

→ The selection of inlet/outlet controlled dynamically, the simplest form of control is to select the inlets and outlets in a cyclic manner in synchronism.

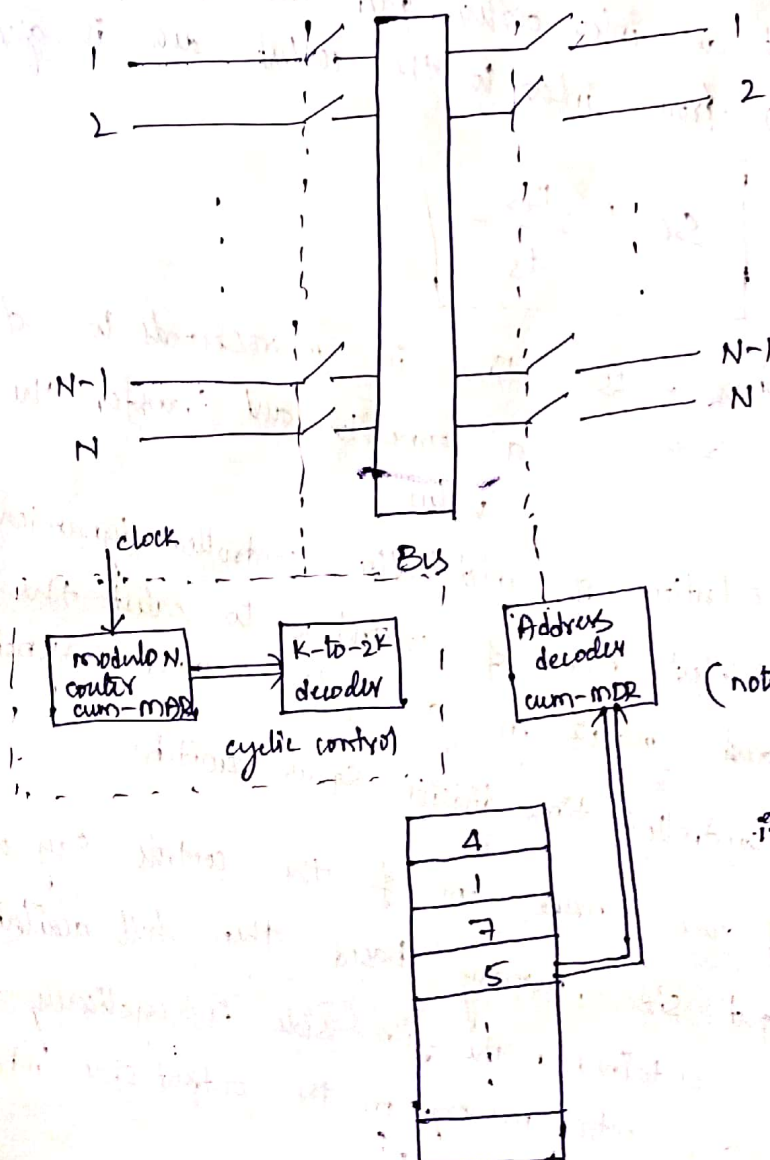
→ Input controlled time division space switch!

If we make one of the controls say on the output side, memory based then full availability can be obtained. The i/p side is cyclically switched there is a control memory on the output side which

contains the address of the outlets stored in continuous locations in order to connect.

→ This switch is said to be "input controlled" as the outlet is chosen depending on the input that is being scanned at any instant.

→ The modulo N -counter of cyclic control acts as the memory address register (MAR) of the control memory.



input control time division space switch.

(3)

→ Since a single switching element, the bus is being time shared by N connections, all of which can be active simultaneously and a physical connection is established between the inlet and outlet for the duration of sample transfer the switching technique is called as "time division space switching".

→ cyclic control for inlets and control memory selection is based on outlets is known as input controlled

→ cyclic control for the outlets and control memory based selection for the inlets is known as output controlled

→ The number of inlets and outlets N , which is equal to the switching capacity is given by

$$N = SC = \frac{125}{t_i + t_m + t_d + t_t}$$

t_i : time to increment the modulo N -counter

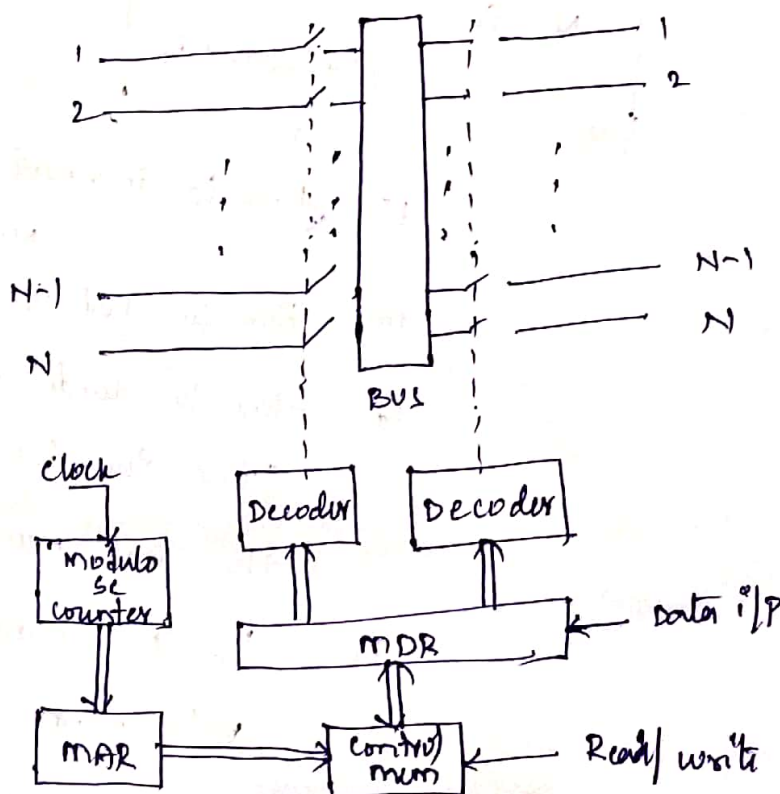
t_m : time to read the control memory

t_d : time to decode address and select the inlet/outlet as

the case may be

t_t : time to transfer the sample value from inlet - outlet.

- The use of cyclic control in input/output controlled switches restricts the number of subscribers on the system rather than the switching capacity.
- cyclic control demands that all the lines be scanned irrespective of whether they are active or not
- A switch configuration based on the use of control memory for controlling both inlets and outlets would permit a much larger number of subscribers than the switching capacity of network either as folded or non folded network and we will call this as 'memory-controlled time division space switch'
- This structure is more general and versatile than the i/p and o/p control structures.
- In this structure the busy inlet and outlets addresses load in a location and load of null value when they will free, the busy/free information will be maintained by bit vectors.



(4)

Basic time Division time Switch:

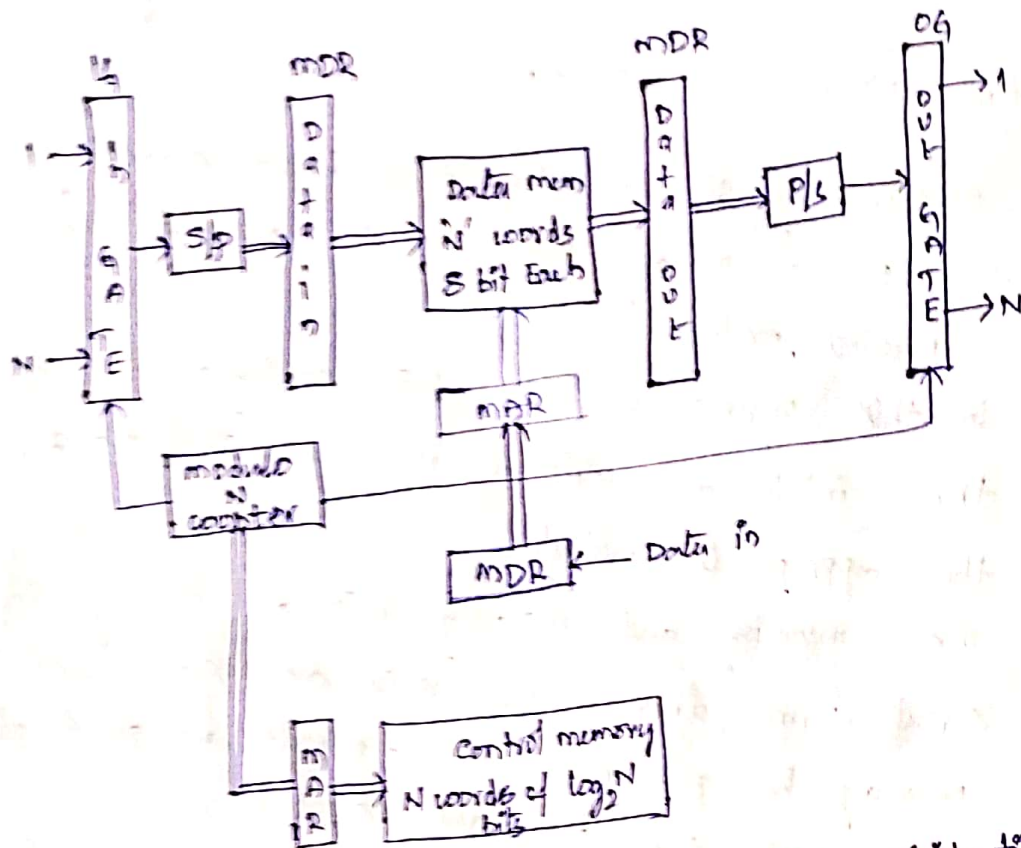
Another way of organising time division switching is to use a memory block in the place of box like previous model.

- In this organisation the data coming in through the inlets are written into and read out of the appropriate outlets.
- The incoming and outgoing data are usually in serial form, whereas the data ~~are~~ (are) become necessary to perform serial-parallel and parallel-to-serial at the inlets and outlets.
- Separate MDR (memory data Register) for inlets and outlets, to do this operations gates are provided in the structure.
- There is a time delay between the acquisition of a sample from an inlet and its delivery to the corresponding outlet. Signifying these aspects the data memory based scheme is known as

'Time division time Switching'

- Time division time switching may be controlled in any of the following ways.

- 1) Sequential write / Random read
- 2) Random write / sequential read
- 3) Random i/p / Random o/p



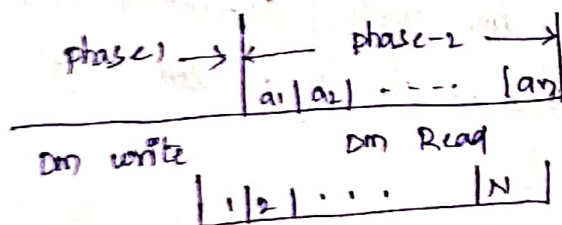
④ switching structure (Time Division time switch)

→ In the first two methods of control the inlets and outlets are scanned sequentially, but in the last method inlets and outlets scanned randomly and data memory accessed sequentially.

④④ → There are two modes in which a time division time switch may be operated under any one of the method of control

- phased operation.
- slotted operation.

phased operation:



(5)

- The phased operation of the time switches proceeds in two phases
- In the first phase, one memory write is involved per inlet where as in the second phase two memory reads, one at the data memory and other at the control memory involved / outlet.
- The time taken for the two phases operation t_s is given by

$$t_s = Nt_d + N(t_d + t_c) \quad \checkmark$$

where

t_d = Read/write time for data memory

t_c = read/write time for control mem

If $t_d = t_c = t_m$ we have

$$t_s = 3Nt_m \quad \checkmark$$

Since the entire operation is to be completed within 125 μ s, we have the expression for no. of subscribers

$$N = \frac{125}{3t_m} \quad \checkmark$$

for overlapped operations the

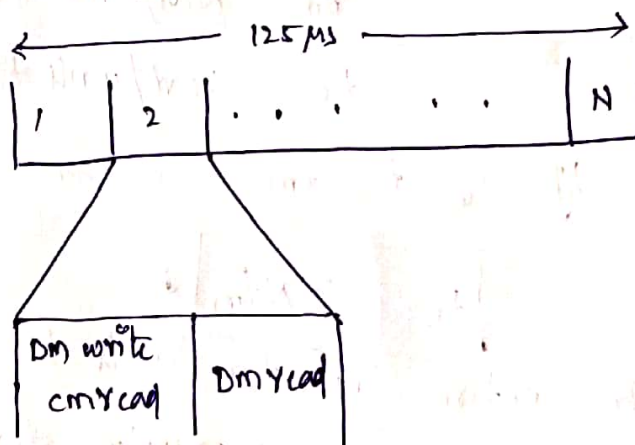
$$N = \frac{125}{2t_m} \quad \checkmark$$

⇒ slotted operation!

In the slotted operation the 125 μ s period is divided into N subperiods of duration $125/N$.

→ In each subperiod i , the following operations are performed.

- 1) Read Inlet i and store the data memory location i
- 2) Read the location i of the control memory which contains the value say J
- 3) Read the data memory location J and transfer the data to outlet i



- choosing between the two modes of operation of time switches is a matter of design choice
- The data transfer from inlets to the data memory can be organised using direct memory access facility in the phased mode, this is not possible in the slotted mode.

⇒ Time multiplexed space switching!

we deal with time division switches where an inlet or an outlet corresponded to a single subscriber line with one speech sample appearing for every 125μs on the line.

→ Here the inlets and outlets are trunks which carry time division multiplexed data streams. Each switch is called time division multiplexed switch.

→ A time multiplexed time division space switch, has N incoming trunks and N outgoing trunks, each carrying a time multiplexed stream of m samples per frame.

→ Each frame is 125μs time duration, in one frame time a total of mN speech samples have to be switched.

→ one sample duration is 125μs/ m . it is usually referred as 'timeslot'.

→ The control memory has mN words, if we view the control memory as m blocks of N words each, a location address may be specified in a two dimensional form (i, j) , where i is the block address and j is the word within the block.

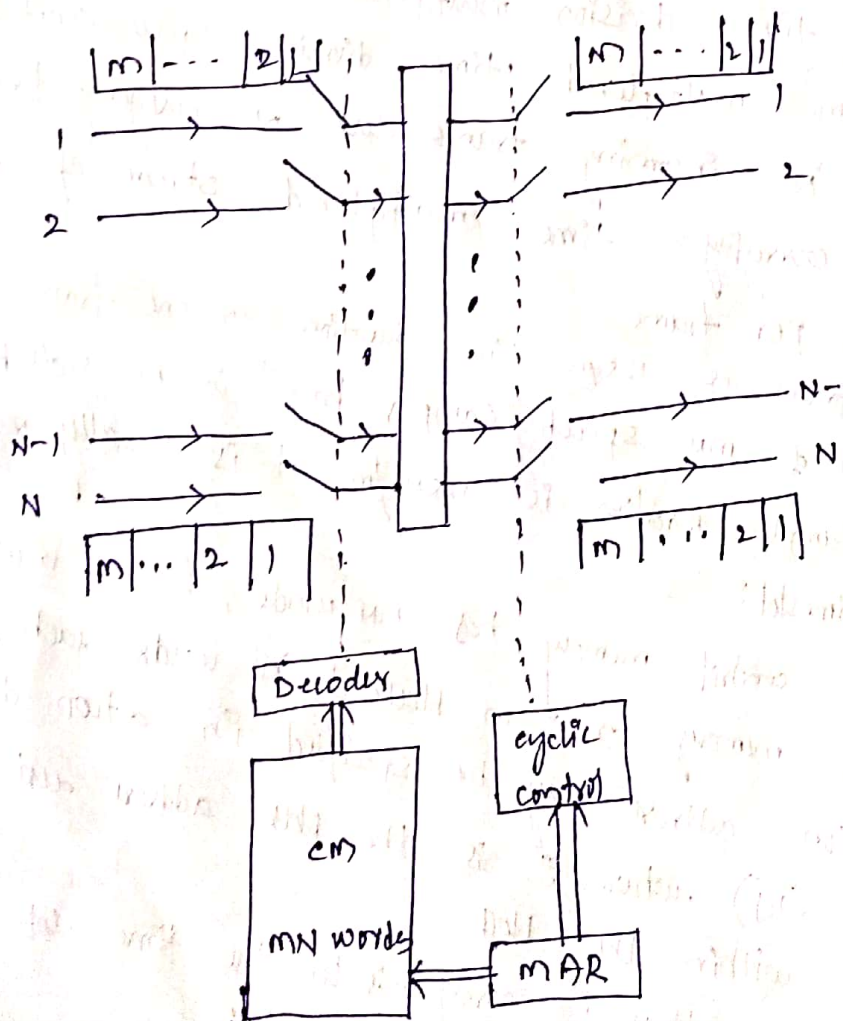
→ The block address i corresponds to the time slot i and the word address j to the outlet j .

⇒ The first N locations of the control memory correspond to the first time slot, the next N locations ... $i \in 1 \dots N$
 $N+1$ to $2N$

E → The number of trunks that can be supported on this switch is given by

$$N = \frac{125}{m \cdot t_s}$$

t_s = is the time including memory access time per inlet-outlet pair.



Time multiplexed space switch

→ The cost of the switch is estimated as

$$C = \text{no. of switches} + \text{no. of memory words}$$

$$= 2NT + MN$$

Example problem: calculate the number of trunks that can be supported on a time multiplexed space division,

- 32 channels are multiplexed in each stream
- control memory access time is 100ns
- ^{Bus} transfer time is 100ns per transfer

we know that $N = \frac{125}{mts}$.

$t_s = \text{Total switching time} =$

$$t_d + t_c = t_s$$

$$100 + 100 = 200ns = t_s$$

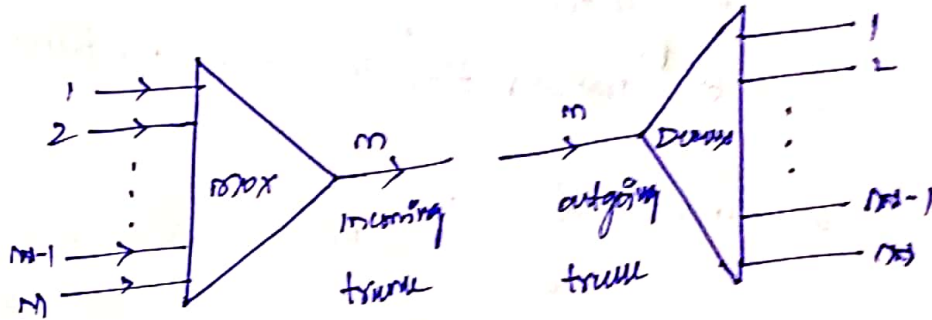
$$\therefore N = \frac{125}{mts} = \frac{125}{32 \times 200 \times 10^{-3}} = 20$$

The no of trunks $N = 20$ ✓

→ Internally the time multiplexed space switches do not provide fully availability. Each incoming trunk carries multiplexed samples from m different voice sources and each stream on the outgoing trunk is demultiplexed to its destinations.

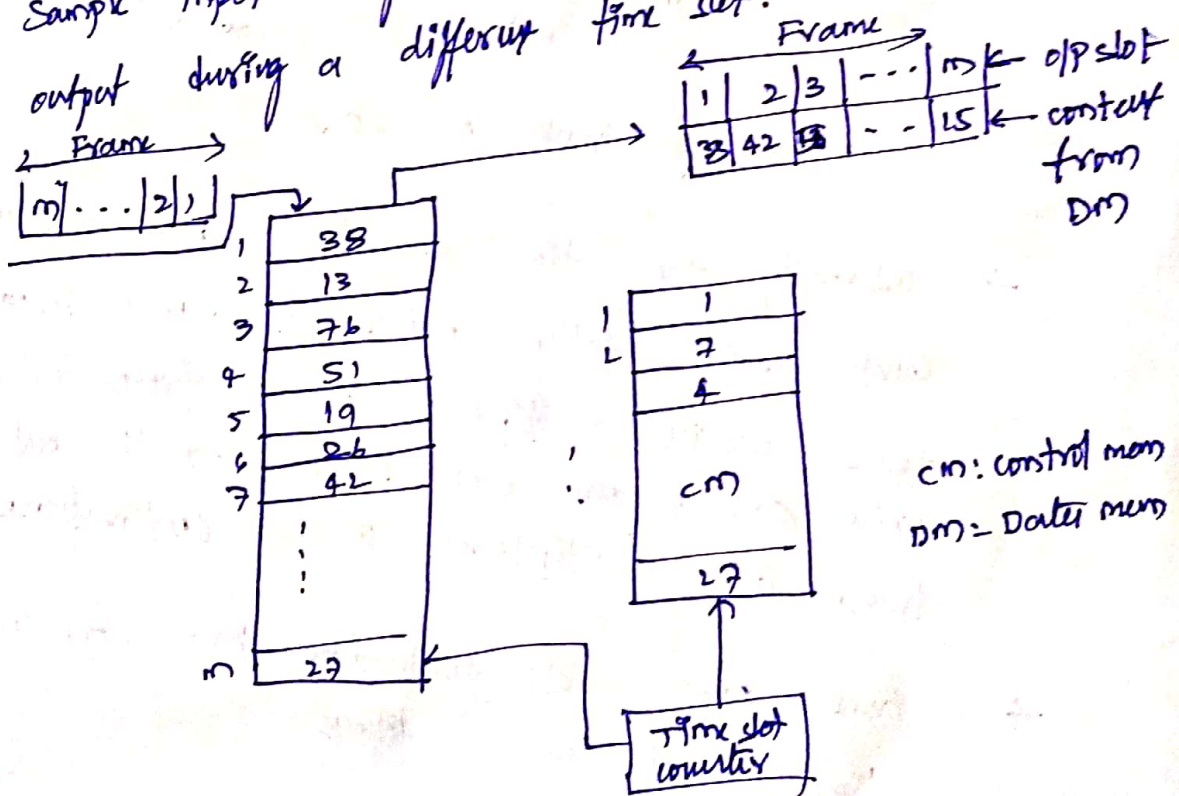
→ trunks, sources and destinations have one-to-one time relationship as follows

- 1) Sources and incoming trunks time slot
- 2) outgoing trunk time slot and the destinations
- 3) time slots of incoming and outgoing trunks.



⇒ Time multiplexed Time switching!

Time multiplexed time switch permit time slot interchange (TSI) of sample values. In TSI a speech sample input during one time slot may be sent to the output during a different time slot.



fig! principle of TSI (Time slot interchange)

→ The operations performed by a time multiplexing time division switch is in one time slot as follows.

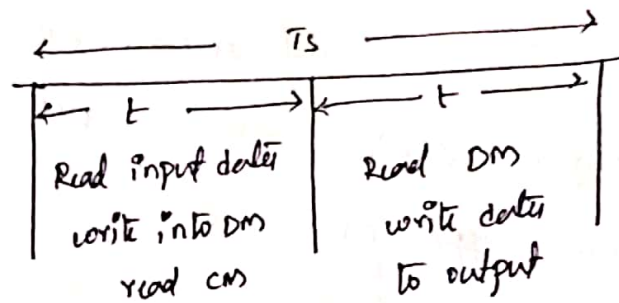
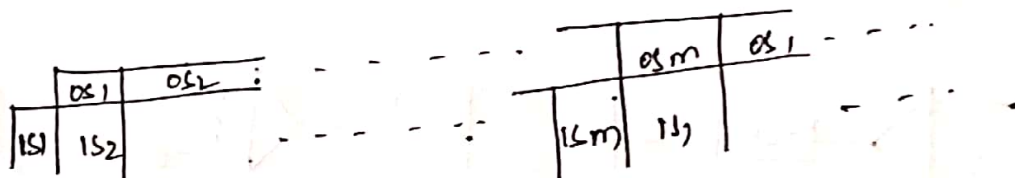


fig → operations in a time slot



⇒ Combination Switching

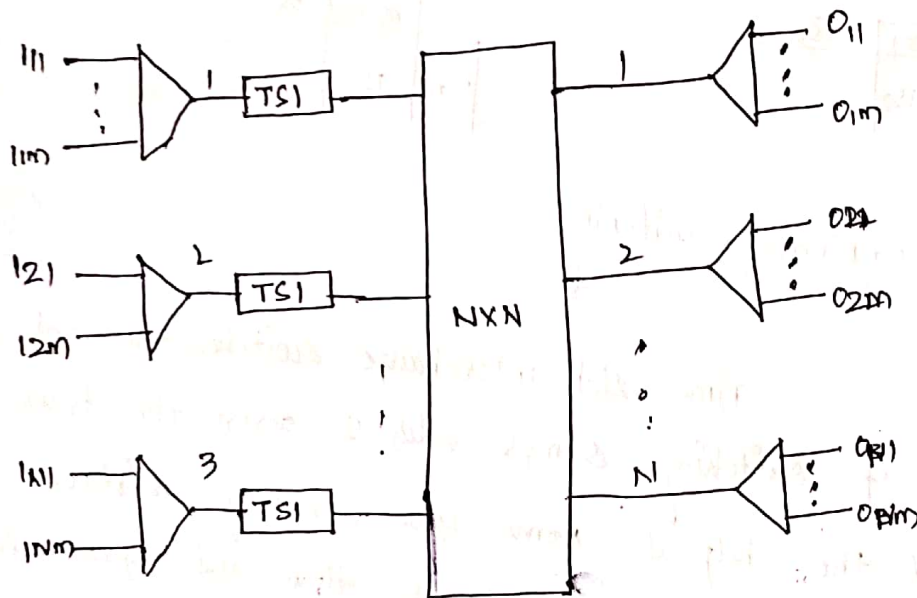
Time slot interchange switches are not capable of switching sample values if across the trunk without the help of some space switching matrices.

→ Therefore a combination of the time and space switches leads to configurations that achieve time slot interchange and sample switch across trunk.

→ A combination switch can be built by using a number of stages of time and space switches.

→ In different stages the combination switch is available i.e. two stage and three stage.

- A two stage combination switch may be organised with time switch in the first stage and the space switch in the second or vice versa.
- The two switch configurations are known as Time-space (TS) and Space-Time (ST)
- ⇒ Two stage Time-space (TS) switch.



→ Each time multiplexed input/output stream carries m channels

→ A subscriber on the input side assigned to one of the inlets and a time slot in that inlet.

→ An input subscriber assigned to line i at time slot j is identified by 147 . Similarly subscriber connected to the output and at time slots 1×0556 .

→ If these two are communicating $147 - 0556$ at defined time slot from input TS1.

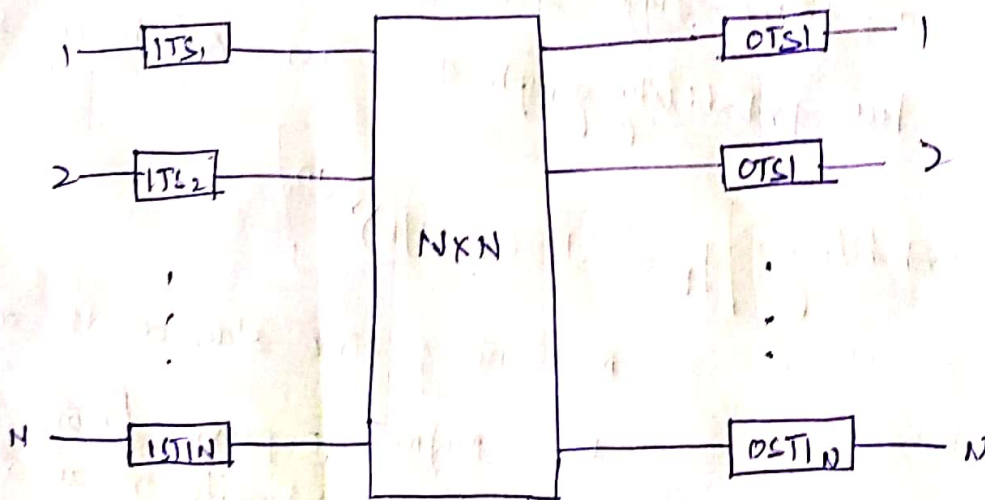
(7)

→ Three-stage combinations switching

Three-stage time and space combination switches are more flexible than their two stages counterparts; the most common three-stage configurations.

→ Those which place time stages on either side of a space stage giving rise to TST configurations.

→ Those which place space stages either side of a time stage giving rise to STS configurations.



Time - Space - Time

→ The first flexibility that becomes obvious in this arrangement is that there is no need to have a fixed space stage time slot for given input and output time slot.

→ For example 1547 is moved to 0656 via an intermediate slot 5.

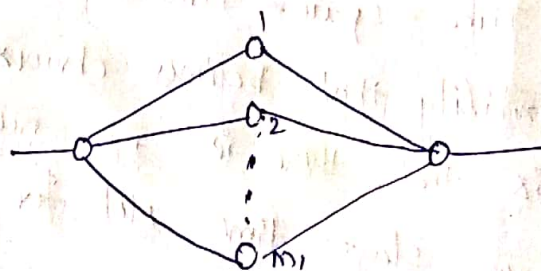
- A incoming channel time slot may be connected to an outgoing channel time slot using any possible space array time slot.
- There are many alternatives paths between a prescribed input and output unlike a two stage network which has only fixed path. This factor reduce the value of blocking probability of a three stage combination switch.
- In a functional sense a TST switch is identical to a three stage space division network. An equivalent Lee probability graph of a TST switch is shown.

Blocking probability :
$$P_B = \left(1 - (1 - \alpha/L)^r \right)^{m_1}$$

m_1 = no. of time slots on the output side

$L = m_1 m_2$ (Expansion factor)

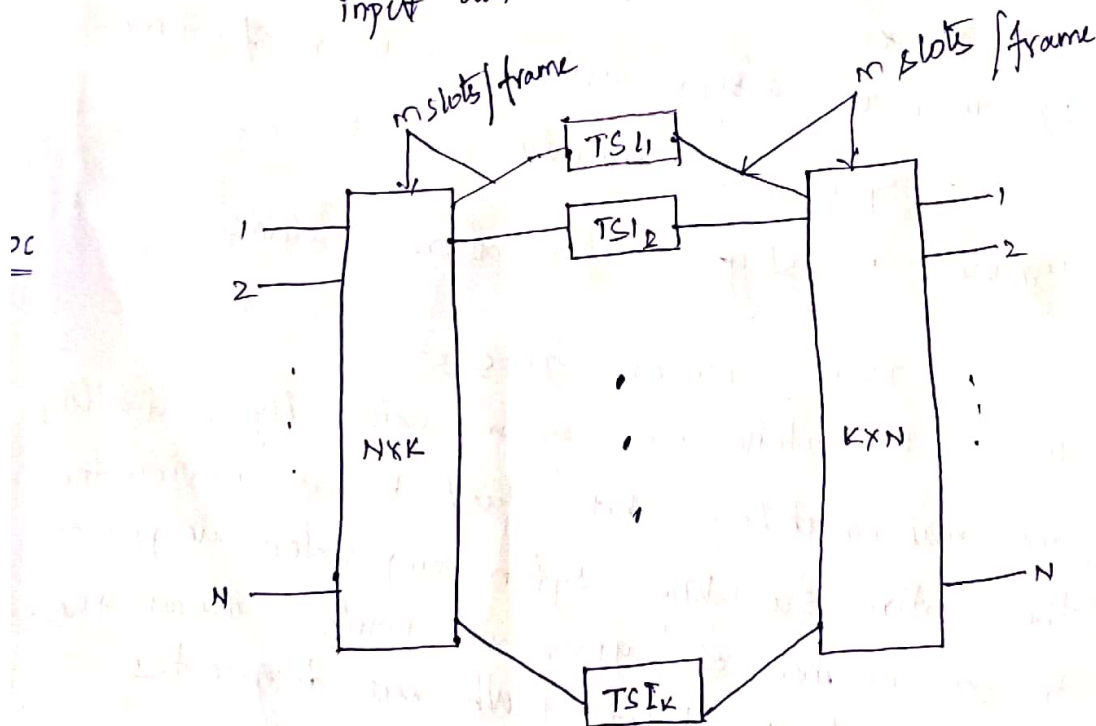
α = traffic intensity on an input.



3-stage Lee graph of TST switch

- The Lee graph shows that any input is having alternative paths in this 3-stage with different time slots.

- A space-time-space (STS) architecture consist of $N \times K$ space matrix at the input, an array of K TSI switches in middle and a $K \times N$ space matrix at the output.
- In this architecture the choice of input and output timeslot is fixed for a given connection. But the flexibility is provided by the ability to utilise any free TSI switch by space switching on the input and output side.



A STS switch

n-stage combination switch:

Very large time division switches, supporting 40,000 lines or more can be economically designed by using more than 3-stages of time and space combinator.

→ we call this N -stage switching where N is greater than 2-stage.

→ N -stage combination networks may also be designed to provide better flexibility and less blockage

→ Basically two approaches are seen in designing N -stage switches.

1) Expanding a TST switch with additional space

2) modular design using a number of time-space (TS) modules.

→ Typical N -stage configurations include

TSSS, TSSSST, TSTSTSTS.

→ In order to achieve high system availability, reliability and maintainability, hot stand-by is provided for the entire switching system. Comparators are provided in a number of appropriate points between the duplicate units to detect faults and diagnostics.

→ In designing n -stage combination systems a modular approach has been adopted, here the use of one type module containing both time and space switches for all stages. Advantage is wide range of availability and maintenance become easy.

→ Disadvantages of module based n -stage is delay due to more modules.

RLRLB↑