**R16**

**Code No: 135BX**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**
**B. Tech III Year I Semester Examinations, May/June - 2019**
**ANALOG AND DIGITAL IC APPLICATIONS**
**(Electrical and Electronics Engineering)**

**Time: 3 hours** **Max. Marks: 75**

**Note:** This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

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**PART - A**

**(25 Marks)**

| | | |
|---|---|---|
| 1.a) | What are the different linear IC packages? | [2] |
| b) | List ideal characteristics of op-amp. | [3] |
| c) | What is Hysteresis? | [2] |
| d) | List and explain the characteristics of three terminals IC regulators. | [3] |
| e) | Define duty cycle D. | [2] |
| f) | List the applications of PLL. | [3] |
| g) | Mention any two applications of multiplier IC. | [2] |
| h) | Explain noise margin and propagation delay with respect to CMOS logic. | [3] |
| i) | Give the applications of JK latch. | [2] |
| j) | Draw the block diagram of 3 - bit ring counter. | [3] |

**PART - B**

**(50 Marks)**

2.a) Design an op-amp differentiator to differentiate an input signal that varies in frequency from 10Hz to about 1 KHz.
b) What are the disadvantages of using zero crossing detector? How it can be overcome using Schmitt trigger? [5+5]

**OR**

3. Draw the circuit diagram of a two input non-inverting type summing amplifier and derive the expression for the output voltage. [10]

4.a) Draw and explain RC-phase shift oscillator.
b) Draw the functional diagram of 723 regulator. [5+5]

**OR**

5.a) How to get a notch filter from a band pass filter? Explain.
b) Explain how a non-symmetrical square wave can be obtained. [5+5]

6. With a neat diagram explain the working principle of R-2R ladder type DAC. Also give its advantages and disadvantages. [10]

**OR**

7.a) Discuss some applications of timer in monostable mode.
b) What is the major difference between digital and analog PLLs? [5+5]

8. With neat circuit diagram explain the working of a 4 - bit odd parity generator. [10]

**OR**

9.a) Explain sinking current and sourcing current of TTL output. Which of the above parameters decide the fan-out and how?

b) Design a full subtractor with NAND gates. [5+5]

10.a) Explain the functional behavior of Static RAM cell? Show the internal structure of 8×4 static RAM.

b) Design an 8-bit parallel-in and serial-out shift register. Explain the operation of the above shift register with the help of timing waveforms. [5+5]

**OR**

11.a) Explain with the help of timing diagram read and write operations of DRAM.

b) Name different type of memories, explain any two. [5+5]

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