Code No: R1622023 **R16** SET - 1

II B. Tech II Semester Regular/ Supplementary Examinations, April/May - 2019
SWITCHING THEORY AND LOGIC DESIGN
(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1. a) Explain the ones and twos complement representation of a binary number.
   b) What are advantages of tabulation method over k-map.
   c) List out the applications of multiplexers.
   d) Design a 4*2 PROM with AND-OR gates.
   e) Draw the circuit diagram of a shift register and list its types.
   f) What is Mealy state diagram?

PART -B

2. a) Convert $(AB6.13)_{16}$ into its octal equivalent and convert $(675.42)_8$ into base-16 number.
   b) Perform the following addition using excess-3 code.
   i) 386 + 756 ii) 1010 + 444.

3. a) State and prove the laws of Boolean algebra.
   b) Define k-map. Explain the implementation and simplification of 2-variable and 3-variable k-map.

4. a) Write a short note on i) Half adder. ii) Full adder.
   b) What is decoder? Construct 3*8 decoder using logic gates and truth tables.

5. a) Write a brief note on PLDs.
   b) Implement $f(A,B,C,D)=\Sigma(0,1,3,5,6,8,9,11,12,13)$ using PROM and explain its procedure.

6. a) Give the comparison between synchronous sequential and asynchronous sequential circuits.
   b) Explain synchronous and ripple counters. Compare their merits and demerits.

7. a) Define finite state machine? Explain about it.
   b) Draw a state diagram of a sequence detector which can detect 101.

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Code No: R1622023 **R16** SET - 2

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(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1. a) Convert $(2468)_{10}$ to $(\ )_{16}$.
   b) Write the advantages and disadvantages of k-map.
   c) What is an excess-3 adder circuit and draw its logic diagram?
   d) List the applications of PLA.
   e) Write the need for preset and clear inputs.
   f) Define state assignment.

PART -B

2. a) Discuss in detail about binary signed number.
   b) What are logic gates? Explain about different logic gates giving their graphic symbols and truth tables.

3. a) Obtain the dual of the following Boolean expressions.
   i) AB+A(B+C)+B´(B+D) ii) ABEF+ABE´F´ + A´B´EF.
   b) Simply the following expression using k-map,
   a) A´B+ABD+AB´CD´+BC
   b) ABC + A´B´C+A´BC+ABC´+A´B´C´

4. a) Give the NAND gate realization of full adder.
   b) What is encoder? Design octal to binary encoder.

5. a) Draw the logic diagram of programmable logic array. Explain its operation.
   b) Design a combinational circuit using PROM that accepts 3-bit binary number and generates its equivalent excess-3 code.

6. a) Differentiate between latch and flip-flop.
   b) Draw the circuit diagram of 4-bit Johnson counter using D-flip flop and explain its operation with the help of bit pattern.

7. a) Explain the analysis of clocked sequential circuits.
   b) Draw a state diagram of a sequence detector which can detect 110.

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Code No: R1622023 **R16** SET - 3

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(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1. a) Explain the importance of parity bit.
   b) Prove that $xy+\overline{x}z+x\overline{y} = xy + \overline{x}z$
   c) Define half subtractor and full subtractor.
   d) What is ROM? List the type of ROM.
   e) Draw NAND and NOR latch.
   f) Define state reduction.

PART -B

2. a) Explain the subtraction of binary number using 2`s complement method with examples.
   b) Explain the method to convert SOP and POS forms into their standards forms.

3. a) Explain the minimization of Boolean expression using theorems.
   b) Simplify the following expression using necessary minimization technique. $F=\Sigma m(0,1,2,8,9,15,17,21,24,25,27,31)$.

4. a) Discuss the functional principle of 4-bit ripple carry adder. What is its major disadvantage?
   b) Implement the following switching function $F(A,B,C,D)=\Sigma m(0,2,3,6,8,9,12,14)$ using the multiplexer.

5. a) Explain in detail about the programming table of PLDs.
   b) Implement $f(A,B,C,D)=\Sigma(0,1,4,5,6,9,10,12,13,15)$ using PLA and explain its procedure.

6. a) Draw the logic diagram of a JK flip-flop and using excitation table explain its operation.
   b) Draw and explain the working of shift left register.

7. a) Draw and explain the logic diagram of Moore model
   b) Draw a state diagram of a sequence detector which can detect 010.

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Code No: R1622023 **R16** SET - 4

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(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1. a) Convert the decimal number 250.5 to base 3, base 4.
   b) State duality theorem.
   c) What is combinational circuit? Give examples.
   d) What are PLDs?
   e) Write the difference between combinational and sequential circuits.
   f) Define state table.

PART -B

2. a) Explain the classification of binary codes.
   b) Realize the universal gates with basic logic gates. Draw the relevant logic diagrams.

3. a) Find the complement of the following Boolean function and reduce them to minimum number of literals.
   a) (bc´ + a´d)(ab´+cd´)
   b) (b´d+a´bc´+acd+a´bc)
   b) Design and draw the circuit diagram of BCD to binary code converter.

4. a) Explain the operation of carry look-a-head adder.
   b) Explain the operation of priority encoder with a neat diagram.

5. a) Give the comparison between PROM, PLA and PAL.
   b) Derive the PLA programming table for the combinational circuit that squares a 3-bit number.

6. a) Write the conversion procedure of the flip-flops. Convert T flip-flop to JK flip-flop.
   b) Draw and explain 4-bit universal shift register.

7. a) Explain the state reduction technique.
   b) Draw a state diagram of a sequence detector which can detect 011.

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