Code No: RT32042 **R13** SET - 1

III B. Tech II Semester Regular/Supplementary Examinations, April -2018

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	What are the elementary discrete time signals?	[3M]
	b)	Find the IDFT of Y (k) = (1, 1, 1, 0)	[4M]
	c)	State the properties of ROC.	[4M
	d)	Why IIR filters do not have linear phase?	[3M]
	e)	Explain how a multi-rate system is different from a single-rate system?	[4M]
	f)	Explain the basic architectural features of programmable DSP devices.	[4M]

PART -B

2	a)	Find the periodicity of the signal x(n) =sin $(2\pi n / 3)$+ cos $(\pi n / 2)$	[4M]
	b)	Explain the frequency response of discrete time system.	[8M]
	c)	What is the causality condition for an LTI system?	[4M]
3	a)	Find the DFT of $x[n] = a^n$ for $0 \le n \le 3$ = 0 otherwise.	[8M]
	b)	Find the linear convolution of the sequences x[n]={ 1,4,0,9,-1} and h[n]= {-3,-4,0,7}	[8M]
4	a)	State and prove any three properties of Z- Transform.	[8M]
	b)	Obtain direct form I, direct form II and cascade realizations of system described by the equation, y[n]=y[n-1]-(1/2)y[n-2]+x[n]-x[n-1]+x[n-2]	[8M]
5	a)	Determine the system function H(Z) of the lowest order Chebyshev digital filter that meets the following specifications. i) 3 db ripple in the passband $0 \le \|\omega\| \le 0.3\pi$ ii) At least 40 dB attenuation in the stopband $0.35\pi \le \|\omega\| \le \pi$. Use the bilinear transformation.	[8M]
	b)	Explain the need for the use of window sequence in the design of FIR filter. Describe the window sequence generally used and compare the properties.	[8M]
6	a)	What is Interpolation? Explain about the frequency domain description of an Interpolator.	[8M]
	b)	What do you mean by fractional sampling rate conversion? Explain with an example of converting 48 kHz signal to 44.1 kHz signal using multi-stage fractional sampling rate converter.	[8M]
7	a)	Discuss in detail the Basic Architectural features of programmable DSP devices,	[8M]
	b)	Discuss in detail the Pipeline Operation of TMS320C54XX Processors.	[8M]

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Code No: RT32042 **R13** SET - 2

III B. Tech II Semester Regular/Supplementary Examinations, April -2018

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	Define discrete time signal and give examples.	[3M]
	b)	What are the advantages FFT over DFT.	[4M]
	c)	What are the different methods of evaluating inverse z transform?	[3M]
	d)	Draw the indirect form realizations of FIR systems?	[4M]
	e)	Derive transfer function of an Interpolator.	[4M]
	f)	Discuss about the various sources of errors in the computation using DSP processor implementations.	[4M]

PART -B

2	a)	Discuss the frequency domain representation of linear time-invariant systems.	[8M]
	b)	Determine the frequency response for the system given by y(n)-3/4y(n-1)+1/8 y(n-2) = x(n)- x(n-1)	[8M]
3	a)	Find the DFT of the sequence x[n]={1,2,1,2,1,2,1,2} using decimation in time algorithm.	[8M]
	b)	State and prove any four Properties of discrete Fourier series.	[8M]
4	a)	With respect to Z transforms define the properties of ROC.	[8M]
	b)	Obtain the parallel form realization for the IIR system described by the transfer function $H(z)=\frac{3+3.6z^{-1}+0.6z^{-2}}{1+0.1z^{-1}-0.2z^{-2}}$.	[8M]
5	a)	Convert the following analog transfer function in to digital using bilinear transform and IIT methods with T=1sec $H(s)=\frac{s}{(s+3)(s+9)}$	[8M]
	b)	Design a HPF of length 7 with cut off frequency of 2 rad/sec using Hamming window..	[8M]
6	a)	With necessary derivations explain the operation of sampling rate conversion by a factor of I/D in both frequency and time domains.	[8M]
	b)	What are the applications of multirate digital signal processing?	[8M]
7	a)	Explain the various pipeline programming models that are adapted in DSP processors.	[8M]
	b)	Explain the Bus Architecture of DSP Processor.	[8M]

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Code No: RT32042 **R13** SET - 3

III B. Tech II Semester Regular/Supplementary Examinations, April -2018

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	Determine whether the following system given by y(n) = log10[{x(n)}] is Casual or not.	[3M]
	b)	What are the properties of convolution sum?	[4M]
	c)	List the applications of Z – transforms.	[3M]
	d)	Compare Chebyshev Filter and Butterworth Filter.	[4M]
	e)	Derive transfer function of Decimator.	[4M]
	f)	What are the functional units present in the TMS320C54XX processor?	[4M]

PART -B

2	a)	Consider a signal $x[n]=(-a)^{-n}\,u[n]$ determine the spectrum X(w).	[8M]
	b)	Determine the response of Second order Discrete Time system governed by the difference equation y(n)-2y(n-1)-3y(n-2)= x(n)+4x(n-1), n≥0,when the input signal is x(n)= 2^nu(n), with initial conditions y(-2)=0,y(-1)=5.	[8M]
3	a)	Explain the significance of FFT algorithms. Draw the basic butterfly diagram for radix - 2 DIT-FFT.	[8M]
	b)	Find the DFT of x[n]={0.5,0.5,0.5,0.5,-1,-1,-1,-1} using decimation in time algorithm.	[8M]
4	a)	Find the Z-Transform $x[n]=(\frac{1}{3})^n Sin[\frac{\pi}{4}n]\,u[n].$	[8M
	b)	Realize $H(z)=\frac{1+0.6z^{-2}+0.2z^{-1}}{3+5z^{-1}+4^{-2}}$ using Direct form I and Direct form II structures	[8M
5	a)	Distinguish between ”maximally flat magnitude response” and “equiripple magnitude response” filters.	[8M
	b)	Explain the impulse invariance method of IIR filter design.	[8M
6	a)	Explain the concept of multi rate signal processing along with two applications of it	[8M
	b)	Explain how sampling rate conversion of band pass signals can be achieved.	[8M
7	a)	Explain in detail the circular addressing mode and bit-reversed addressing mode.	[8M
	b)	Explain Memory Access schemes in DSPs.	[8M

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Code No: RT32042 **R13** SET - 4

III B. Tech II Semester Regular/Supplementary Examinations, April -2018

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	Determine whether the system defined by $y(n) = x(-n^2-2)$ is time invariant or not.	[3M]
	b)	What is FFT? How many multiplications and additions are required to compute N point DFT using redix-2 FFT?	[4M]
	c)	State and prove Parsvel's theorem.	[4M]
	d)	Why FIR filters are always stable?	[4M]
	e)	What is Down sampling?	[3M]
	f)	Explain the role of on-chip peripherals for programmable digital signal processors.	[4M]

PART -B

2	a)	For each case determine the system is stable or causal i) $h(n)= \sin(\pi n / 2)$ ii) $h(n) = \delta(n) + \sin \pi n$ iii) $h(n) = 2^n u(-n)$	[10M]
	b)	Show that an LTI system can be described by its unit sample response.	[6M]
3	a)	State and prove convolution Properties of DFT.	[8M]
	b)	Compute the DFT for the sequence (0.5,0.5,0.5,0.5,1,1,1,1) using DIF-FFT	[8M]
4	a)	Find the Inverse Z-Transform of $X(z) = \frac{1-\frac{1}{3}z^{-1}}{(1-z^{-1})(1+2z^{-1})}, \lvert z \rvert > 2$ using partial fractions method.	[8M
	b)	Obtain the cascade form realization for the recursive IIR system described by the transfer function $H(z) = \frac{3+3.6z^{-1}+0.6z^{-2}}{1+0.1z^{-1}-0.2z^{-2}}$.	[8M
5	a)	Explain the design procedure for IIR filters using Butterworth approximations.	[8M
	b)	A low pass filter is to be designed with the following desired frequency response.	[8M

$H_d(e^{jw}) = e^{-j2w}, \quad -\pi/4 \le \omega \le \pi/4$

$0, \quad \pi/4 \le |\omega| \le \pi$

Determine the filter coefficients $h_d(n)$ if the window function is defined as

$\omega(n) = 1, \quad 0 \le n \le 4$

$0, \quad$ otherwise

Also determine the frequency response $H(e^{jw})$ of the designed filter.

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6 a) With the help of an example define Decimation and Interpolation operations in DSP. [8M]

b) A signal, x(n), at a sampling frequency of 2.048 kHz is to be decimated by a factor of 32 to yield a signal at a sampling frequency of 64 Hz. The signal band of interest extends from 0 to 30 Hz. The anti-aliasing digital filter should satisfy the following specifications: [8M]

Pass band deviation	0.01 dB
Stop band deviation	80dB
Pass band	0-30Hz
Stop band	32-64 Hz

The signal components in the range from 30 to 32 Hz should be protected from aliasing. Design a suitable two stage decimator.

7 a) What is the difference between internal and external modes of clocking of TMS320C54XX Processor? [8M]

b) Explain different pipeline programming models that are adapted in DSP processors? [8M]

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